DATA SHEET

74HC/HCT03

Quad 2-input NAND gate

Product specification

File under Integrated Circuits, IC06

December 1990

Philips
Semiconductors

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Quad 2-input NAND gate   74HC/HCT03

FEATURES

- Level shift capability
- Output capability: standard (open drain)
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT03 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT03 provide the 2-input NAND function.

The 74HC/HCT03 have open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is LOW, the output may be pulled to any voltage between GND and V_{Omax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PZL}/ t_{PLZ}	propagation delay	C_L = 15 pF; R_L = 1 kΩ; V_{CC} = 5 V	8	10	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1, 2 and 3	4.0	4.0	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

    $$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) + \Sigma (V_O^2/R_L) \times \text{duty factor LOW, where:}$$

    f_i = input frequency in MHz
    f_o = output frequency in MHz
    V_O = output voltage in V
    C_L = output load capacitance in pF
    V_{CC} = supply voltage in V
    R_L = pull-up resistor in MΩ
    $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
    $\Sigma (V_O^2/R_L)$ = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

3. The given value of C_{PD} is obtained with:
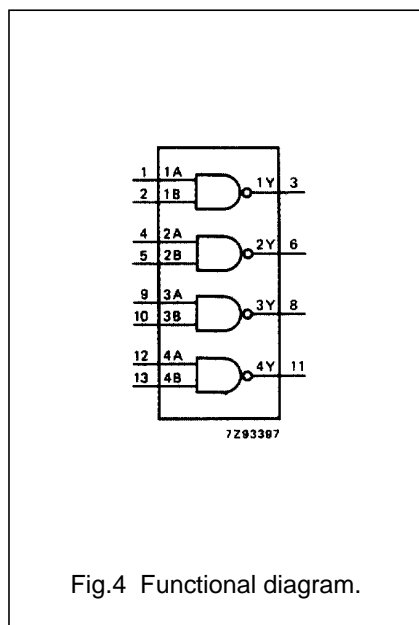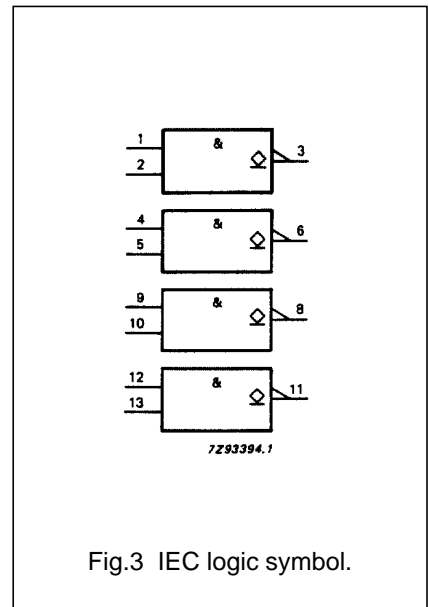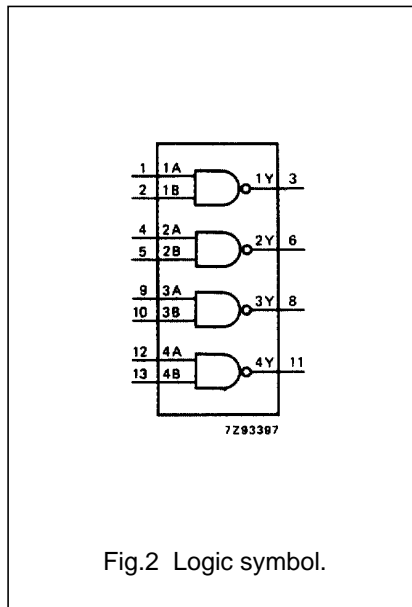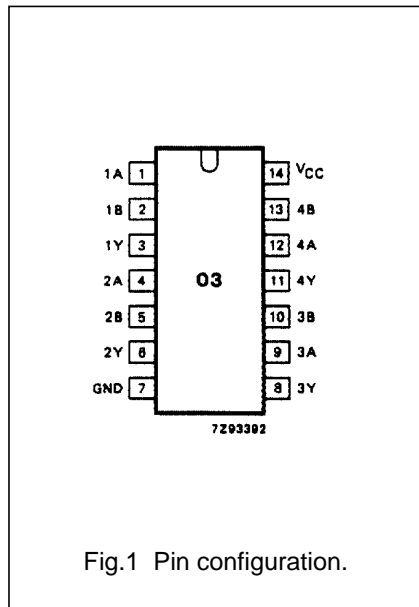 C_L = 0 pF and R_L = ∞

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

Quad 2-input NAND gate

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

Fig.1 Pin configuration.

Fig.2 Logic symbol.

Fig.3 IEC logic symbol.

Fig.4 Functional diagram.

Fig.5 Logic diagram (one gate).
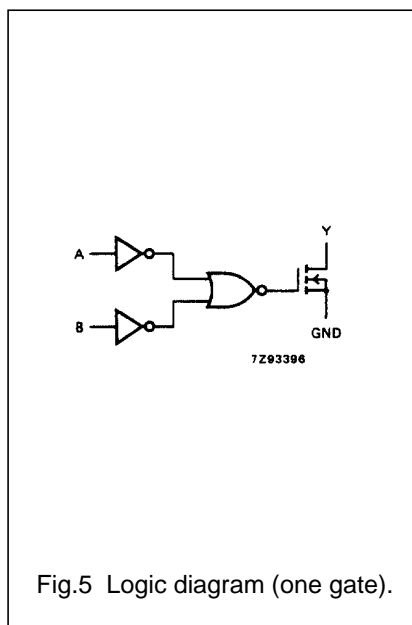
FUNCTION TABLE

INPUTS		OUTPUT
nA	nB	nY
L	L	Z
L	H	Z
H	L	Z
H	H	L

Note

1. H = HIGH voltage level
   L = LOW voltage level
   Z = high impedance OFF-state

Quad 2-input NAND gate

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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V_{CC}	DC supply voltage	−0.5	+7	V	
V_O	DC output voltage	−0.5	+7	V	
I_{IK}	DC input diode current		20	mA	for $V_I < −0.5$ V or $V_I > V_{CC} + 0.5$ V
$−I_{OK}$	DC output diode current		20	mA	for $V_O < −0.5$ V
$−I_O$	DC output sink current		25	mA	for $− 0.5$ V $< V_O$
$±I_{CC}$; $±I_{GND}$	DC VCC or GND current		50	mA	
T_{stg}	storage temperature range	−65	+150	°C	
P_{tot}	power dissipation per package				for temperature range; −40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

Quad 2-input NAND gate

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*, except that the V_{OH} values are not valid for open drain. They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting V_{OH}
I_{CC} category: SSI

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | T_{amb} (°C) 74HC | | | | | | UNIT | TEST CONDITIONS | | |
| | | +25 | | | −40 to +85 | | −40 to +125 | | V_{CC} (V) | V_I | OTHER |
		min.	typ.	max.	min.	max.	min.	max.				
I_{OZ}	HIGH level output leakage current			0.5		5.0		10.0	µA	2.0 to 6.0	V_{IL}	$V_O = V_{O(max)}$[1] or GND

Note

1. The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T_{amb} (°C) 74HC | | | | | | UNIT | TEST CONDITIONS | |
| | | +25 | | | −40 to +85 | | −40 to +125 | | V_{CC} (V) | WAVEFORMS |
		min.	typ.	max.	min.	max.	min.	max.			
t_{PZL}/ t_{PLZ}	propagation delay nA, nB to nY		28 10 8	95 19 16		120 24 20		145 29 25	ns	2.0 4.5 6.0	Fig.6
t_{THL}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

Quad 2-input NAND gate

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*, except that the V_{OH} values are not valid for open drain. They are replaced by I_{OZ} as given below.

Output capability: standard (open drain), excepting V_{OH}
I_{CC} category: SSI

Voltages are referenced to GND (ground = 0 V)

| SYMBOL | PARAMETER | T_{amb} (°C) 74HCT | | | | | | | UNIT | TEST CONDITIONS | | |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | V_{CC} (V) | V_I | OTHER |
		min.	typ.	max.	min.	max.	min.	max.				
I_{OZ}	HIGH level output leakage current			0.5		5.0		10.0	µA	4.5 to 5.5	V_{IL}	$V_O = V_{O(max)}$[1] or GND

Note

1. The maximum operating output voltage ($V_{O(max)}$) is 6.0 V.

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.0

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

| SYMBOL | PARAMETER | T_{amb} (°C) 74HCT | | | | | | | UNIT | TEST CONDITIONS | |
| | | +25 | | | −40 to +85 | | −40 to +125 | | | V_{CC} (V) | WAVEFORMS |
		min.	typ.	max.	min.	max.	min.	max.			
t_{PZL}/ t_{PLZ}	propagation delay nA, nB, to nY		12	24		30		36	ns	4.5	Fig.6
t_{THL}	output transition time		7	15		19		22	ns	4.5	Fig.6

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AC WAVEFORMS

HC: $V_M = 50\%$; $V_I = $ GND to V_{CC}
HCT: $V_M = 1.3$ V; $V_I = $ GND to 3 V.

Fig.6   Waveforms showing the input (nA, nB) to output (nY) propagation delays and the output transition times.
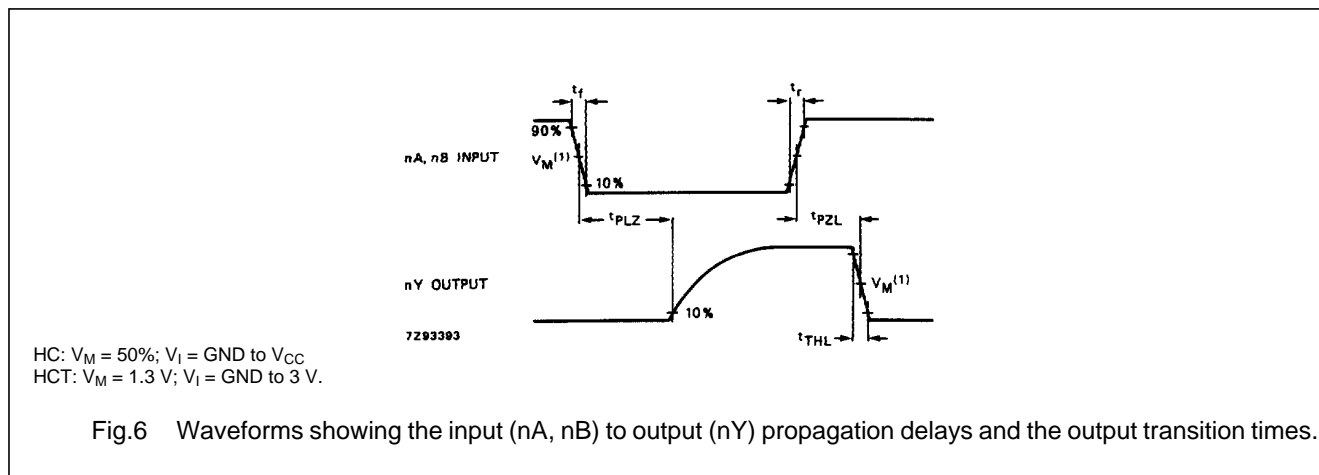
TEST CIRCUIT AND WAVEFORMS

Fig.7 Test circuit (open drain)

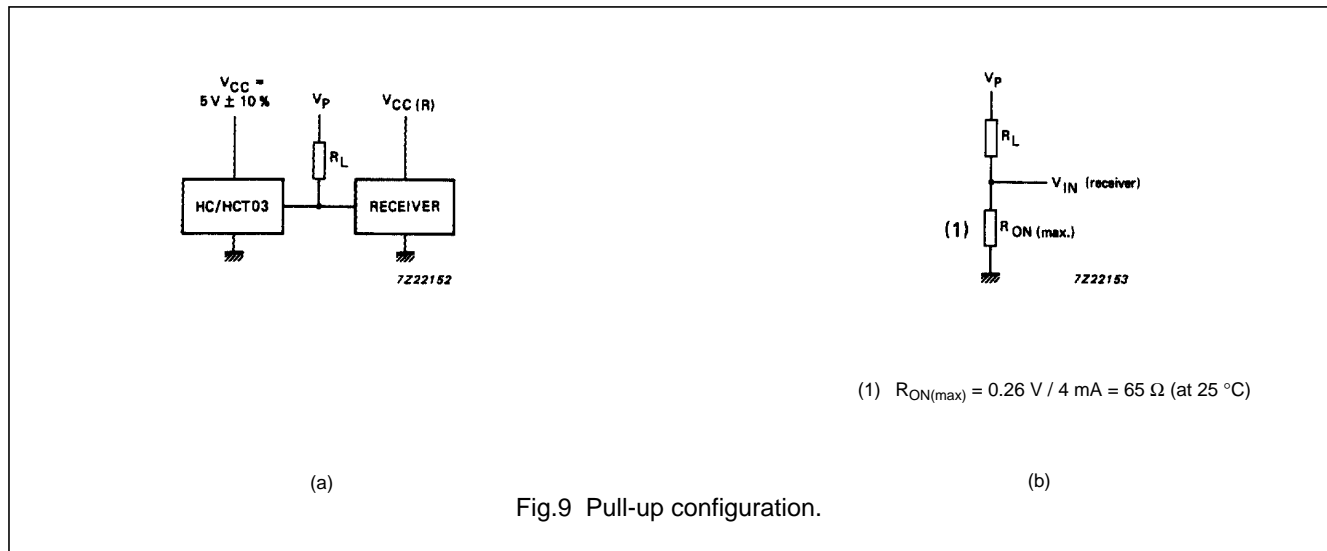Fig.8 Input pulse definitions.
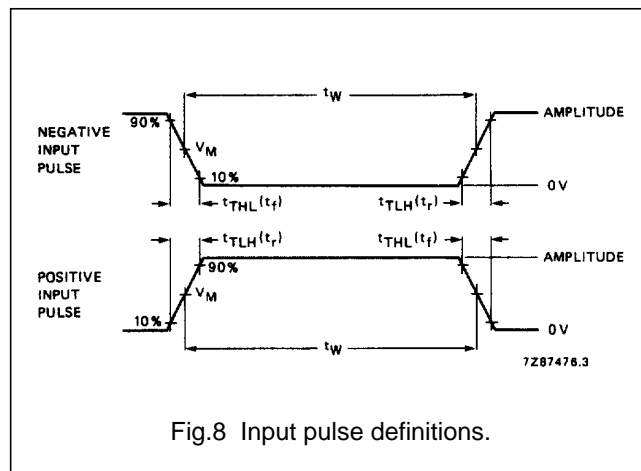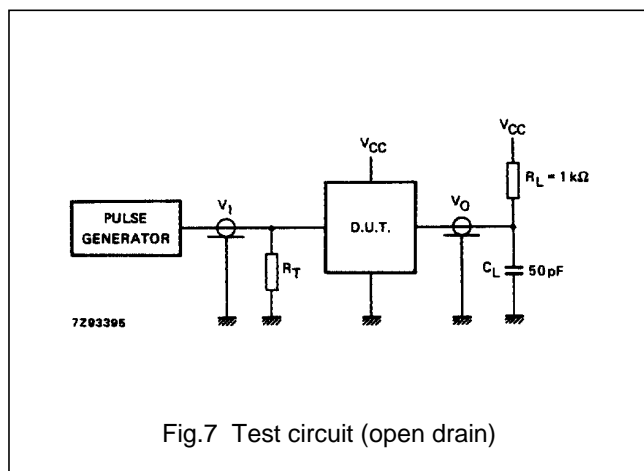
Definitions for Figs. 7, 8:

C_L = load capacitance including jig and probe capacitance
(see AC CHARACTERISTICS for values).

R_T = termination resistance should be equal to the output impedance Z_O of the pulse generator.

t_r = $t_f = 6$ ns; when measuring f_{max}, there is no constraint on t_r, t_f with 50% duty factor.

FAMILY	AMPLITUDE	V_M	t_r; t_f	
			f_{max}; PULSE WIDTH	OTHER
74HC	V_{CC}	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

Quad 2-input NAND gate

APPLICATION INFORMATION

(1) $R_{ON(max)} = 0.26$ V / 4 mA = 65 Ω (at 25 °C)

(a)

(b)

Fig.9 Pull-up configuration.

(1) V_{CC} (R) = 2.0 V; V_{IL} = 0.5 V.
(2) V_{CC} (R) = 5.0 V; V_{IL} = 0.8 V.
(3) V_{CC} (R) = 4.5 V; V_{IL} = 1.35 V.
(4) V_{CC} (R) = 6.0 V; V_{IL} = 1.8 V.

Fig.10 Minimum resistive load as a function of the pull-up voltage.
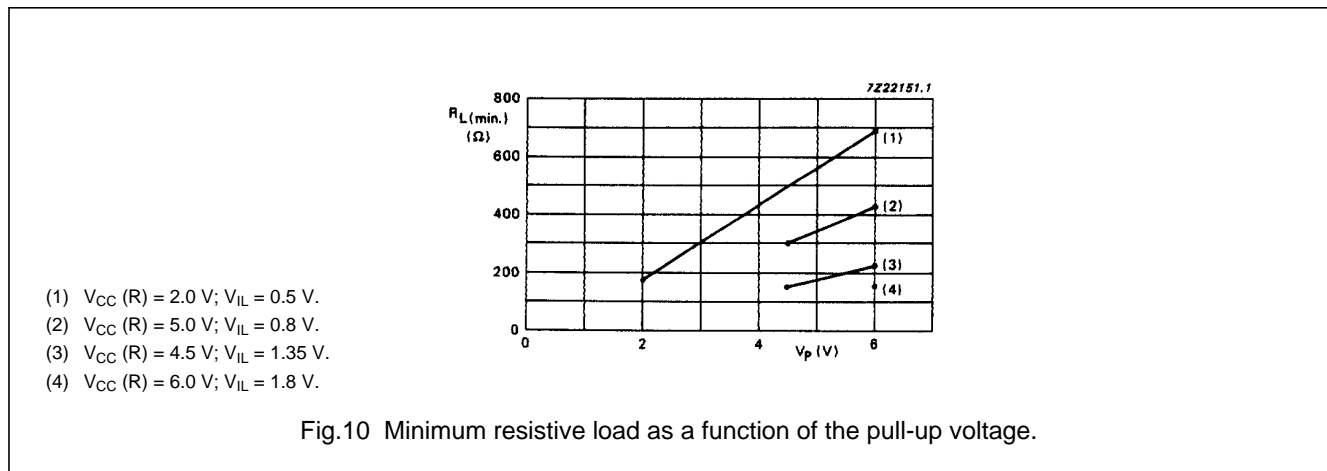
Notes to Figs 9 **and 10**

If $V_P - V_{CC}$ (R) > 0.5 V a positive current will flow into the receiver (as described in the *"USER GUIDE"*; input/output protection), this will not affect the receiver provided the current does not exceed 20 mA. At V_{CC} < 4.5 V, $R_{ON\ (max)}$ is not guaranteed; $R_{ON(max)}$ can be estimated using Figs 33 and 34 in the *"USER GUIDE"*.

Note to Application information

All values given are typical unless otherwise specified.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

74HC/HCT03; Quad 2-input NAND gate

Information as of 2003-04-22

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General description

The 74HC/HCT03 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

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Features

- Level shift capability
- Output capability: standard (open drain)
- I_{CC} category: SSI

Datasheet

Type number	Title	Publication release date	Datasheet status	Page count	File size (kB)	Datasheet
74HC/HCT03	Quad 2-input NAND gate	12/1/1990	Product specification	8	52	Download

Additional datasheet info

To complete the device datasheet with package and family information, also download the following PDF files. The "Logic Package Information" document is required to determine in which package(s) this device is available.

Document	Description
1 HCT_FAMILY_SPECIFICATIONS	HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications

Parametrics

Type number	Package	Description	Propagation Delay(ns)	Voltage	No. of Pins	Power Dissipation Considerations	Logic Switching Levels	Output Drive Capability
74HC03D	SOT108-1 (SO14)	Quad 2-Input NAND Gate with Level Shift Capability	15	5 Volts +	14	Low Power or Battery Applications	CMOS	Low
74HC03DB	SOT337-1 (SSOP14)	Quad 2-Input NAND Gate with Level Shift Capability	15	5 Volts +	14	Low Power or Battery Applications	CMOS	Low
74HC03N	SOT27-1 (DIP14)	Quad 2-Input NAND Gate with Level Shift Capability	15	5 Volts +	14	Low Power or Battery Applications	CMOS	Low
74HC03PW	SOT402-1 (TSSOP14)	Quad 2-Input NAND Gate with Level Shift Capability	15	5 Volts +	14	Low Power or Battery Applications	CMOS	Low
74HCT03D	SOT108-1 (SO14)	Quad 2-Input NAND Gate with Level Shift Capability; TTL Enabled	15	5 Volts +	14	Low Power or Battery Applications	TTL	Low
74HCT03DB	SOT337-1 (SSOP14)	Quad 2-Input NAND Gate with Level Shift Capability; TTL Enabled	15	5 Volts +	14	Low Power or Battery Applications	TTL	Low

Type number		Input NAND							
74HCT03N	SOT27-1 (DIP14)	Quad 2-Input NAND Gate with Level Shift Capability; TTL Enabled	15		5 Volts +	14	Low Power or Battery Applications	TTL	Low
74HCT03PW	SOT402-1 (TSSOP14)	Quad 2-Input NAND Gate with Level Shift Capability; TTL Enabled	15		5 Volts +	14	Low Power or Battery Applications	TTL	Low

◻ **Products, packages, availability and ordering**

Type number	North American type number	Ordering code (12NC)	Marking/Packing ☐ **Discretes packing info**	Package	Device status	Buy online
74HC03D	74HC03D	9337 486 60652	Standard Marking * Bulk Pack, CECC	SOT108-1 (SO14)	Full production	order this -
	74HC03D-T	9337 486 60653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT108-1 (SO14)	Full production	order this -
74HC03DB	74HC03DB	9351 737 70112	Standard Marking * Bulk Pack	SOT337-1 (SSOP14)	Full production	order this -
	74HC03DB-T	9351 737 70118	Standard Marking * Reel Pack, SMD, 13"	SOT337-1 (SSOP14)	Full production	order this -
74HC03N	74HC03N	9337 486 50652	Standard Marking * Bulk Pack, CECC	SOT27-1 (DIP14)	Full production	order this -
74HC03PW	74HC03PW	9351 741 80112	Standard Marking * Bulk Pack	SOT402-1 (TSSOP14)	Full production	order this -
	74HC03PW-T	9351 741 80118	Standard Marking * Reel Pack, SMD, 13"	SOT402-1 (TSSOP14)	Full production	order this -
74HCT03D	74HCT03D	9337 486 40652	Standard Marking * Bulk Pack, CECC	SOT108-1 (SO14)	Full production	order this -
	74HCT03D-T	9337 486 40653	Standard Marking * Reel Pack, SMD, 13", CECC	SOT108-1 (SO14)	Full production	order this -
74HCT03DB	74HCT03DB	9351 737 60112	Standard Marking * Bulk Pack	SOT337-1 (SSOP14)	Full production	order this -
	74HCT03DB-T	9351 737 60118	Standard Marking * Reel Pack, SMD, 13"	SOT337-1 (SSOP14)	Full production	order this -

74HCT03N	74HCT03N	9337 486 30652	Standard Marking * Bulk Pack, CECC	SOT27-1 (DIP14)	Full production	order this	-
74HCT03PW	74HCT03PW	9351 862 50112	Standard Marking * Bulk Pack	SOT402-1 (TSSOP14)	Full production	order this	-
	74HCT03PW-T	9351 862 50118	Standard Marking * Reel Pack, SMD, 13"	SOT402-1 (TSSOP14)	Full production	order this	-

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❑ Support & tools

❑ HC/T Family Specifications, The IC06 74HC/HCT/HCMOS Logic Family Specifications(date 01-Mar-98)
❑ HC/T User Guide(date 01-Nov-97)

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