

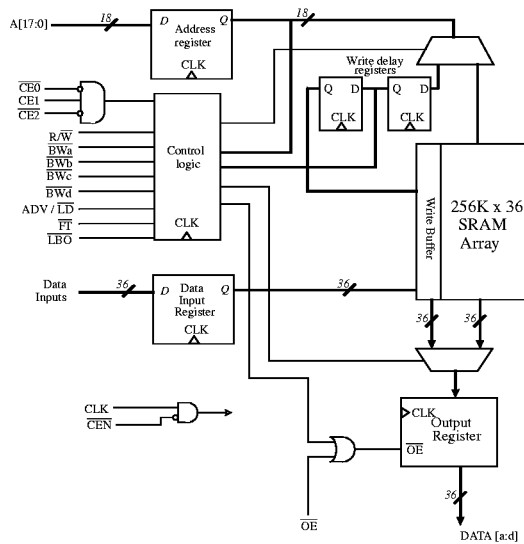
3.3V 256K×32/36 synchronous burst SRAM with NTD™

SRAM

Features

- Organization: 262,144 words × 32 or 36 bits
- NTD™ architecture for efficient bus operation
- Fast clock speeds to 150 MHz in LVTTTL/LVCMOS
- Fast clock to data access: 3.8/4/5 ns
- Fast OE access time: 3.5/3.8/4 ns
- Fully synchronous operation
- “Flow-through” mode
- Asynchronous output enable control
- Multiple packaging options
  - Economical 100-pin TQFP package
  - Chip-scale fBGA package for smallest footprint
- Byte write enables
- Clock enable for operation hold
- Multiple chip enables for easy expansion
- 3.3 core power supply
- 2.5V or 3.3V I/O operation with separate V<sub>DDQ</sub>
- 10 mW typical standby power

Logic block diagram



Pin arrangement

For information on the pin arrangement for the TQFP package, refer to the section entitled “Pin arrangement for TQFP (top view)” on page 3.

For information on the pin arrangement for the chip-scale fBGA package, refer to the section entitled “Pin arrangement for chip-scale fBGA (top view)” on page 3.

Selection guide

	7C3256K36-3.8	7C3256K36-4	7C3256K36-5	Units
Minimum cycle time	6.7	7.5	10	ns
Maximum pipelined clock frequency	150	133.3	100	MHz
Maximum pipelined clock access time	3.8	4	5	ns
Maximum operating current	325	300	250	mA
Maximum standby current	60	60	60	mA
Maximum CMOS standby current (DC)	5	5	5	mA

NTD™ is a trademark of Alliance Semiconductor Corporation.



## Functional description

The AS7C3256K36Z family is a high performance CMOS 8 Mbit synchronous Static Random Access Memory (SRAM) organized as 262,144 words  $\times$  32 or 36 bits and incorporates a LATE LATE Write.

This variation of the 8Mb synchronous SRAM uses the No Turnaround Delay (NTD™) architecture, featuring an enhanced write operation that improves bandwidth over pipeline burst devices. In a normal pipeline burst device, the write data, command, and address are all applied to the device on the same clock edge. If a read command follows this write information, the system must wait for two 'dead' cycles for valid data to become available. These dead cycles can significantly reduce overall bandwidth for applications requiring random access or read-modify-write operations.

NTD™ devices use the memory bus more efficiently by introducing a write 'latency' which matches the two cycle read latency. Write data is applied two cycles after the write command and address, allowing the read pipeline to clear. With NTD™, write and read operations can be used in any order without producing dead bus cycles.

The single register flow-through mode of the AS7C3256K36Z and AS7C3256K32Z can disable output circuit registers. This allows the device to operate in 2-1-1-1 mode rather than 3-1-1-1 found in two-stage pipeline architecture timing. The single register flow-through mode sacrifices access and cycle times for lower latency. Consult AC timing parameters for more details.

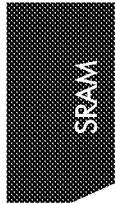
Assert  $R/\overline{W}$  low to perform write cycles. Byte write enable controls write access to specific bytes, or can be tied low for full 32/36 bit writes. Write enable signals, along with the write address, are registered on a rising edge of the clock. Write data is applied to the device two clock cycles later. Unlike some asynchronous SRAMs, output enable  $\overline{OE}$  does not need to be toggled for write operations; it can be tied low for normal operations. Outputs go to a high impedance state when the device is de-selected by any of the three chip enable inputs. In pipeline mode, a two cycle deselect latency allows pending read or write operations to be completed.

Use the ADV (burst advance) input to perform burst read and write operations. When ADV is high, external addresses are ignored, and internal address counters increment in the count sequence specified by the  $\overline{LBO}$  control. Any device operations, including burst, can be stalled using the  $\overline{CEN}$  clock enable input. If  $\overline{CEN}$  is high at the rising edge of clock, all operations are effectively stalled.

The AS7C3256K36Z and AS7C3256K32Z operate with a  $3.3V \pm 5\%$  power supply for the device core ( $V_{DD}$ ). DQ circuits use a separate power supply ( $V_{DDQ}$ ) that operates across 3.3V or 2.5V ranges. These devices are available in a 100-pin  $14 \times 20$  mm TQFP and 119 ball fine-pitch Ball-Grid-Array (fBGA) packaging.

## Capacitance <sup>1</sup>

Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	$C_{IN}$	Address and control pins	$V_{in} = 0V$	5	pF
I/O capacitance	$C_{I/O}$	I/O pins	$V_{in} = V_{out} = 0V$	7	pF







Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	$V_{DD}, V_{DDQ}$	-0.5	+4.6	V
Input voltage relative to GND (input pins)	$V_{IN}$	-0.5	+4.6	V
Input voltage relative to GND (I/O pins)	$V_{IN}$	-0.5	$V_{DDQ} + 0.5$	V
Power dissipation	$P_D$	-	1.2	W
DC output current	$I_{OUT}$	-	30	mA
Storage temperature (plastic)	$T_{stg}$	-65	+150	°C
Temperature under bias	$T_{bias}$	-65	+135	°C

Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Synchronous truth table

CE0	CE1	CEZ	ADV/ED	R/W	BW[a:d]	OE	Address source	CLK	Operation
H	X	X	(1)	X	X	X	NA	L to H	Deselect, high-Z
X	L	X	(1)	X	X	X	NA	L to H	Deselect, high-Z
X	X	H	(1)	X	X	X	NA	L to H	Deselect, high-Z
L	H	L	L	H	X	X	External	L to H	Begin read
L	H	L	H	H	X	X	External	L to H	Begin burst read
L	H	L	L	L	L(2)	X	External	L to H	Begin write
L	H	L	H	L	L(2)	X	External	L to H	Begin burst write

Key: X = Don't Care, L = Low, H = High.



Recommended operating conditions

Parameter	Symbol	Min	Nominal	Max	Unit	
Supply voltage	V <sub>DD</sub>	3.0	3.3	3.6	V	
	GND	0.0	0.0	0.0	V	
3.3V I/O supply voltage	V <sub>DDQ</sub>	3.135	3.3	3.465	V	
	GND <sub>Q</sub>	0.0	0.0	0.0	V	
2.5V I/O supply voltage	V <sub>DDQ</sub>	2.35	2.5	2.65	V	
	GND <sub>Q</sub>	0.0	0.0	0.0	V	
Input voltages <sup>†</sup>	Address and control pins	V <sub>IH</sub>	2.0	-	4.5	V
		V <sub>IL</sub>	-0.5*	-	0.8	V
	I/O pins	V <sub>IH</sub>	2.0	-	V <sub>DDQ</sub> + 0.5	V
		V <sub>IL</sub>	-0.5*	-	0.8	V
Ambient operating temperature	T <sub>A</sub>	0	-	70	°C	

\* V<sub>IL</sub> min = -2.0V for pulse width less than 0.2 x t<sub>RC</sub>.

<sup>†</sup> Input voltage ranges apply to 3.3V I/O operation. For 2.5V operation, contact factory for input specifications.

DC electrical characteristics

Parameter	Symbol	Test conditions	-3.8		-4		-5		Unit
			Min	Max	Min	Max	Min	Max	
Input leakage current	I <sub>II</sub>	V <sub>DD</sub> = Max, V <sub>in</sub> = GND to V <sub>DD</sub>	-	2	-	2	-	2	µA
Output leakage current	I <sub>LO</sub>	OE ≥ V <sub>IH</sub> , V <sub>DD</sub> = Max, V <sub>out</sub> = GND to V <sub>DD</sub>	-	2	-	2	-	2	µA
Operating power supply current	I <sub>CC</sub>	CE = V <sub>IL</sub> , CE = V <sub>IH</sub> , CE = V <sub>IL</sub> , f = f <sub>max</sub> , I <sub>out</sub> = 0 mA	-	325	-	300	-	250	mA
Standby power supply current	I <sub>SB</sub>	Deselected, f = f <sub>max</sub>	-	60	-	60	-	60	mA
	I <sub>SB1</sub>	Deselected, f = 0, all V <sub>IN</sub> ≤ 0.2V or ≥ V <sub>DD</sub> - 0.2V	-	5	-	5	-	5	mA
Output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 8 mA, V <sub>DDQ</sub> = 3.6V	-	0.4	-	0.4	-	0.4	V
	V <sub>OH</sub>	I <sub>OH</sub> = -4 mA, V <sub>DDQ</sub> = 3.0V	2.4	-	2.4	-	2.4	-	V

DC electrical characteristics for 2.5V I/O operation

Parameter	Symbol	Test conditions	-166		-150		-133		-100		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Output leakage current	I <sub>LO</sub>	OE ≥ V <sub>IH</sub> , V <sub>DD</sub> = Max, V <sub>out</sub> = GND to V <sub>DD</sub>	-1	1	-1	1	-1	1	-1	1	µA
Output voltage	V <sub>OL</sub>	I <sub>OL</sub> = 2 mA, V <sub>DDQ</sub> = 2.65V	-	0.7	-	0.7	-	0.7	-	0.7	V
	V <sub>OH</sub>	I <sub>OH</sub> = -2 mA, V <sub>DDQ</sub> = 2.35V	1.7	-	1.7	-	1.7	-	1.7	-	








Timing characteristics over operating range

Parameter	Symbol	-3.8		-4		-5		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock frequency	F <sub>MAX</sub>	-	150	-	133	-	100	MHz	1
Cycle time (pipelined mode)	t <sub>CYC</sub>	6.6	-	7.5	-	10	-	ns	
Cycle time (flow-through mode)	t <sub>CYCF</sub>	10	-	12	-	15	-	ns	
Clock access time (pipelined mode)	t <sub>CD</sub>	-	3.8	-	4	-	5	ns	
Clock access time (flow-through mode)	t <sub>CDF</sub>	-	6.6	-	7.5	-	10	ns	
Output enable Low to data valid	t <sub>OE</sub>	-	3.5	-	3.8	-	4	ns	
Clock High to output Low Z	t <sub>LZC</sub>	0	-	0	-	0	-	ns	8
Data output hold from clock High	t <sub>OH</sub>	1.5	-	1.5	-	2	-	ns	8
Output enable Low to output Low Z	t <sub>LZOE</sub>	1	-	1.5	-	2	-	ns	8
Output enable High to output High Z	t <sub>HZOE</sub>	-	3.5	-	4	-	4	ns	8
Clock High to output High Z	t <sub>HZC</sub>	-	3	-	3.5	-	3.5	ns	8
Clock High to output High Z	t <sub>HZCN</sub>	-	1.5	-	2	-	2.5	ns	1,9
Clock High pulse width	t <sub>CH</sub>	2.6	-	2.8	-	3	-	ns	
Clock Low pulse width	t <sub>CL</sub>	2.6	-	2.8	-	3	-	ns	
Address and Control setup to clock High	t <sub>AS</sub>	1.3	-	1.5	-	1.5	-	ns	
Data setup to clock High	t <sub>DS</sub>	1.3	-	1.5	-	1.5	-	ns	
Write setup to clock High	t <sub>WS</sub>	1.3	-	1.5	-	1.5	-	ns	
Chip select setup to clock High	t <sub>CSS</sub>	1.3	-	1.5	-	1.5	-	ns	
Address hold from clock High	t <sub>AH</sub>	0.5	-	0.5	-	0.5	-	ns	
Data hold from clock High	t <sub>DH</sub>	0.5	-	0.5	-	0.5	-	ns	
Write hold from clock High	t <sub>WH</sub>	0.5	-	0.5	-	0.5	-	ns	
Chip select hold from clock High	t <sub>CSH</sub>	0.5	-	0.5	-	0.5	-	ns	
Output rise time (0 pF load)	t <sub>R</sub>	1.5	-	1.5	-	1.5	-	V/ns	1
Output fall time (0 pF load)	t <sub>F</sub>	1.5	-	1.5	-	1.5	-	V/ns	1

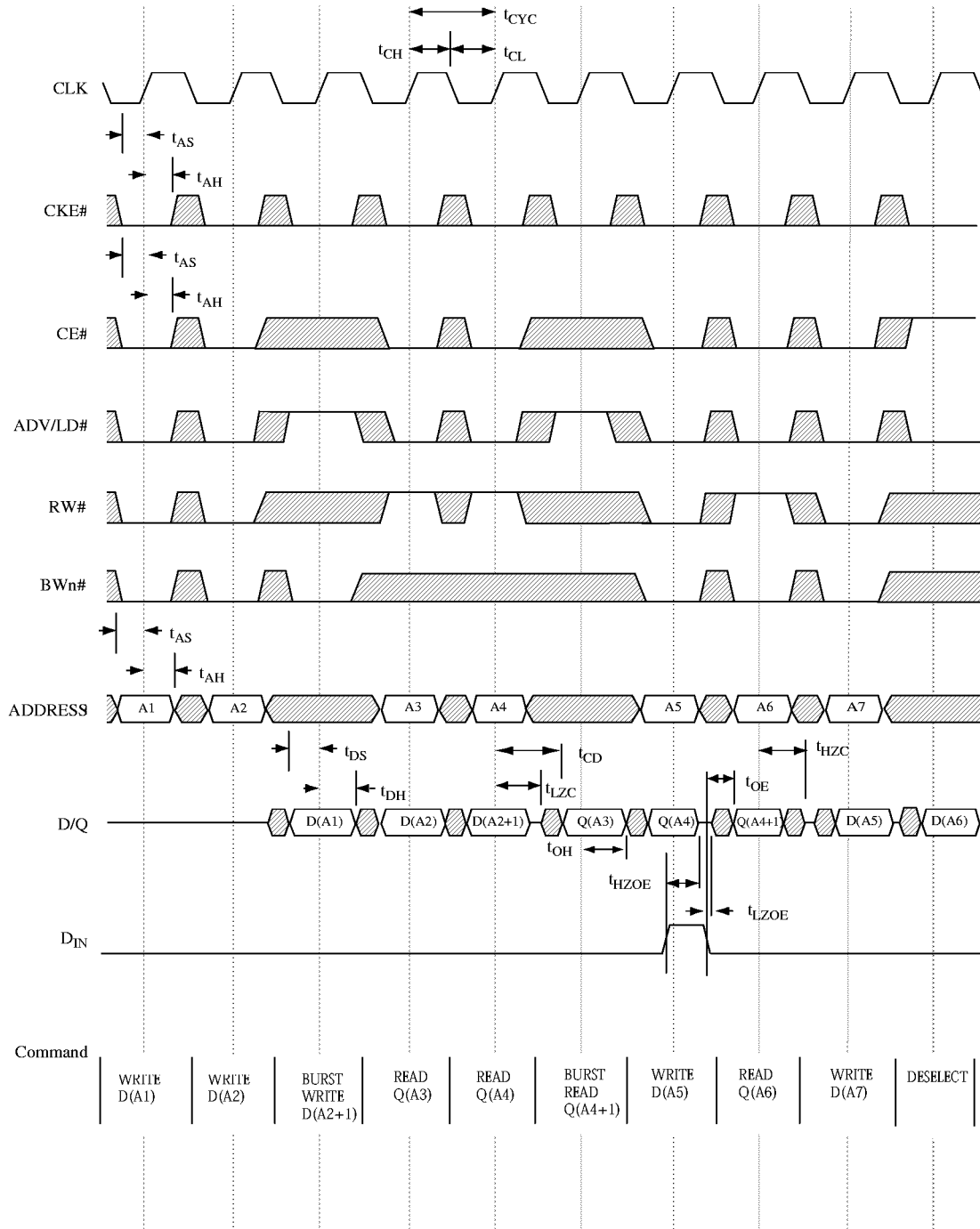
See "Notes" on page 9.

Key to switching waveforms

 Rising input     
  Falling input     
  Undefined output/don't care



Timing waveform of read/write cycle



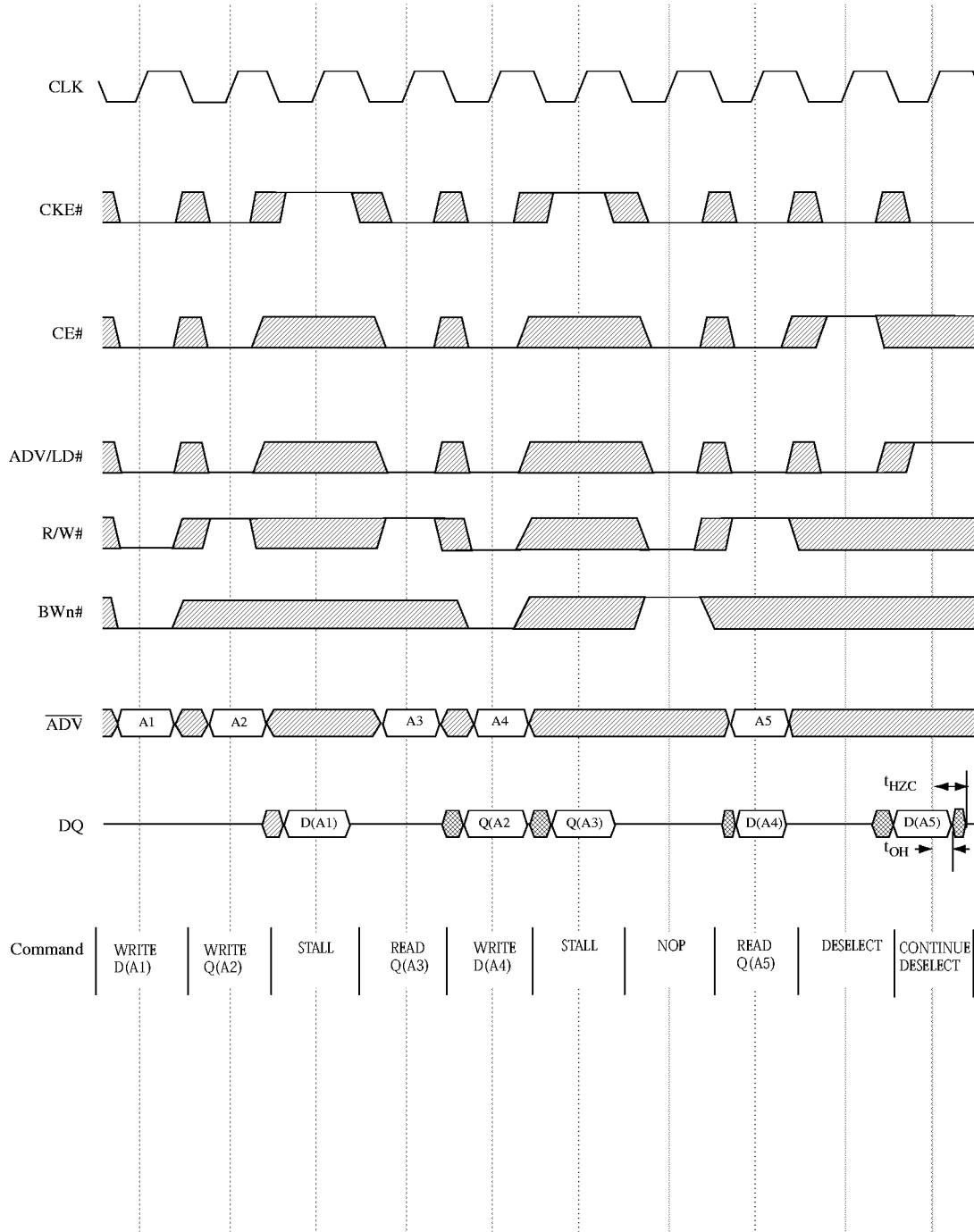
SRAM

Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low.  
WE[0:3] is don't care.



NOP, stall and deselect cycles

SRAM



Note:  $\oplus$  = XOR when MODE = High/No Connect;  $\oplus$  = ADD when MODE = Low.  
 Note:  $\oplus$  = XOR when MODE = High/No Connect;  $\oplus$  = ADD when MODE = Low.  
 Note:  $\overline{OE}$  is Low.





Notes

- 1 This parameter is guaranteed but not tested.
- 2 For test conditions, see AC Test Conditions, Figures A, B, C.
- 3 This parameter is sampled and not 100% tested.
- 4 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK when chip is enabled.
- 5 Typical values measured at 3.3V, 25 °C and 10 ns cycle time.
- 6  $I_{CC}$  given with no output loading.  $I_{CC}$  increases with faster cycle times and greater output loading.
- 7 Transitions are measured  $\pm 500$  mV from steady state voltage. Output loading specified with  $C_L = 5$  pF as in Figure C.
- 8  $t_{HZOE}$  is less than  $t_{LZOE}$ ; and  $t_{HZC}$  is less than  $t_{LZC}$  at any given temperature and voltage.
- 9  $t_{HZCN}$  is a 'no load' parameter to indicate exactly when SRAM outputs have stopped driving.

AC test conditions

- Output Load: see Figure B, except for  $t_{LZC}$ ,  $t_{LZOE}$ ,  $t_{HZOE}$ ,  $t_{HZC}$  see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (Measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

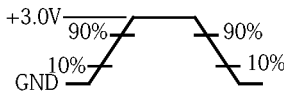


Figure A: Input waveform

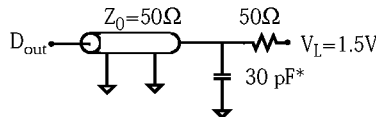


Figure B: Output load (A)

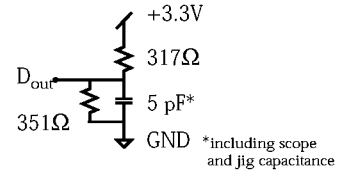


Figure C: Output load (B)

AS7C3256K32Z and AS7C3256K36Z ordering information

Package	Width	150 MHz	133 MHz	100 MHz
TQFP	$\times 32$	AS7C3256K32Z-3.8TQC	AS7C3256K32Z-4TQC	AS7C3256K32Z-5TQC
TQFP	$\times 36$	AS7C3256K36Z-3.8TQC	AS7C3256K36Z-4TQC	AS7C3256K36Z-5TQC
fBGA	$\times 32$	AS7C3256K32Z-3.8BC	AS7C3256K32Z-4BC	AS7C3256K32Z-5BC
fBGA	$\times 36$	AS7C3256K36Z-3.8BC	AS7C3256K36Z-4BC	AS7C3256K36Z-5BC

AS7C3256K32Z and AS7C3256K36Z part numbering system

AS7C	3	256K36	P	--XX	XX	C
SRAM prefix	Operating voltage	Part number, organization	Timing Z=NTD™ timing P=PBSRAM	Access time (ns)	Package: TQ = TQFP B = fBGA	Commercial temperature, 0 °C to 70 °C

