AMD

Am29DL400B

4 Megabit (512 K x 8-Bit/256 K x 16-Bit) CMOS 3.0 Volt-only, Simultaneous Operation Flash Memory

DISTINCTIVE CHARACTERISTICS

- **Simultaneous Read/Write operations**
  - — Host system can program or erase in one bank, then immediately and simultaneously read from the other bank
  - — Zero latency between read and write operations
  - — Read-while-erase
  - — Read-while-program
- **Single power supply operation**
  - — Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
  - — Regulated voltage range: 3.0 to 3.6 volt read and write operations and for compatibility with high performance 3.3 volt microprocessors
- **Manufactured on 0.35 µm process technology**
- **High performance**
  - — Access times as fast as 70 ns
- **Low current consumption (typical values at 5 MHz)**
  - — 7 mA active read current
  - — 21 mA active read-while-program or read-while-erase current
  - — 17 mA active program-while-erase-suspended current
  - — 200 nA in standby mode
  - — 200 nA in automatic sleep mode
  - — Standard t_{CE} chip enable access time applies to transition from automatic sleep mode to active mode
- **Flexible sector architecture**
  - — Two 16 Kword, two 8 Kword, four 4 Kword, and six 32 Kword sectors in word mode
  - — Two 32 Kbyte, two 16 Kbyte, four 8 Kbyte, and six 64 Kbyte sectors in byte mode
  - — Any combination of sectors can be erased
  - — Supports full chip erase
- **Unlock Bypass Program Command**
  - — Reduces overall programming time when issuing multiple program command sequences
- **Sector protection**
  - — Hardware method of locking a sector to prevent any program or erase operation within that sector
  - — Sectors can be locked in-system or via programming equipment
  - — Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically pre-programs and erases sectors or entire chip
  - — Embedded Program algorithm automatically programs and verifies data at specified address
- **Minimum 1,000,000 program/erase cycles guaranteed per sector**
- **Package options**
  - — 44-pin SO
  - — 48-pin TSOP
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply flash standard
  - — Superior inadvertent write protection
- **Data# Polling and Toggle Bits**
  - — Provides a software method of detecting program or erase cycle completion
- **Ready/Busy# output (RY/BY#)**
  - — Hardware method for detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends or resumes erasing sectors to allow reading and programming in other sectors
  - — No need to suspend if sector is in the other bank
- **Hardware reset pin (RESET#)**
  - — Hardware method of resetting the device to reading array data

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GENERAL DESCRIPTION

The Am29DL400B is an 4 Mbit, 3.0 volt-only flash memory device, organized as 262,144 words or 524,288 bytes. The device is offered in 44-pin SO and 48-pin TSOP packages. The word-wide (x16) data appears on DQ0–DQ15; the byte-wide (x8) data appears on DQ0–DQ7. This device requires only a single 3.0 volt V_{CC} supply to perform read, program, and erase operations. A standard EPROM programmer can also be used to program and erase the device.

The standard device offers access times of 70, 80, 90, and 120 ns, allowing high-speed microprocessors to operate without wait states. Standard control pins—chip enable (CE#), write enable (WE#), and output enable (OE#)—control read and write operations, and avoid bus contention issues.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into two banks. Bank 1 contains eight boot/parameter sectors, and Bank 2 consists of fourteen larger, code sectors of uniform size. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with **zero latency.** This releases the system from waiting for the completion of program or erase operations.

Am29DL400B Features

The device offers complete compatibility with the **JEDEC single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programrning times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device automatically returns to reading array data.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector within that bank that is not selected for erasure. True background erase can thus be achieved. There is no need to suspend the erase operation if the read data is in the other bank.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device to reading array data, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

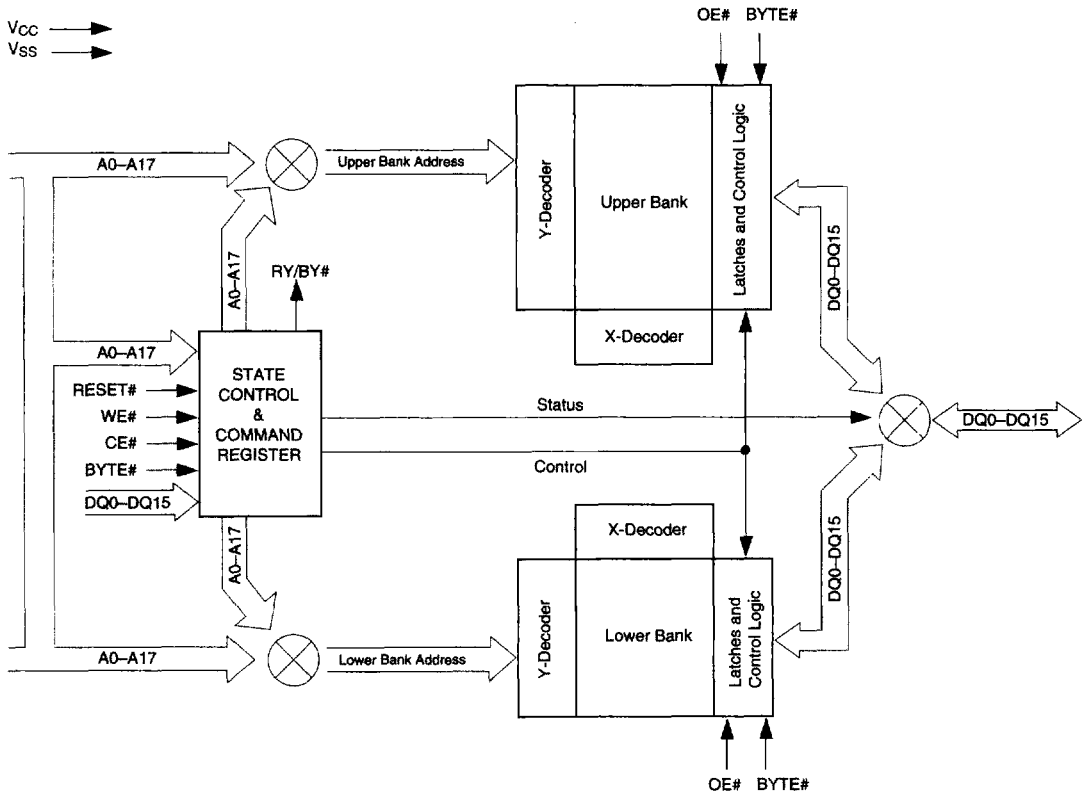
AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability, and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The bytes are programmed one byte or word at a time using hot electron injection.

PRODUCT SELECTOR GUIDE

Family Part Number		Am29DL400B			
Speed Options	Regulated Voltage Range: V_{CC} = 3.0 – 3.6 V	**70R**			
	Full Voltage Range: V_{CC} = 2.7 – 3.6 V		**80**	**90**	**120**
Max Access Time (ns)		70	80	90	120
CE# Access (ns)		70	80	90	120
OE# Access (ns)		30	30	35	50

Note: *See "AC Characteristics" for full specifications.*

BLOCK DIAGRAM



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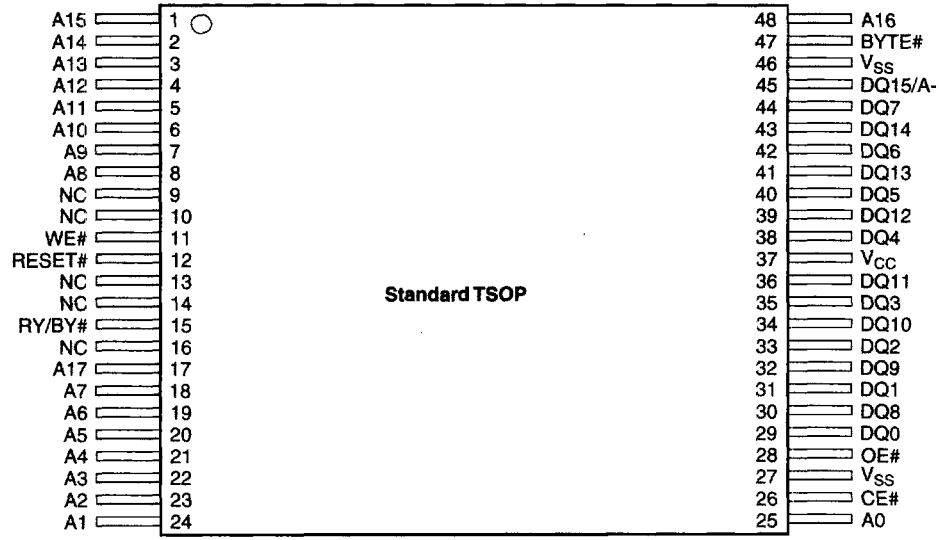
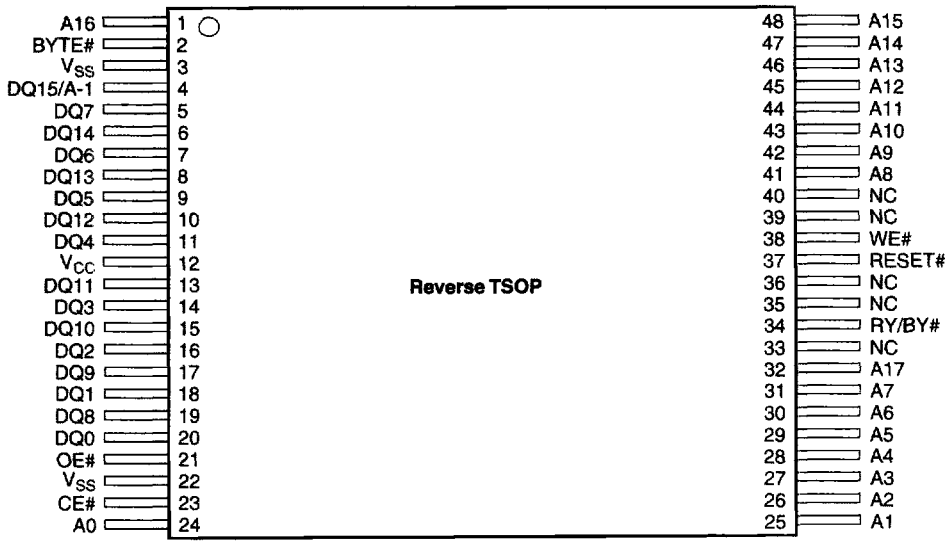
CONNECTION DIAGRAMS





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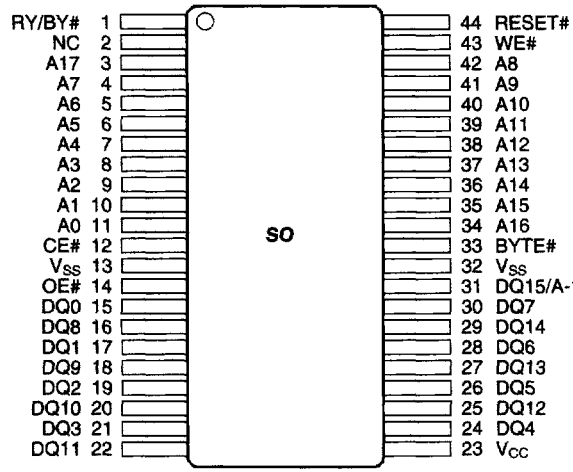
CONNECTION DIAGRAMS



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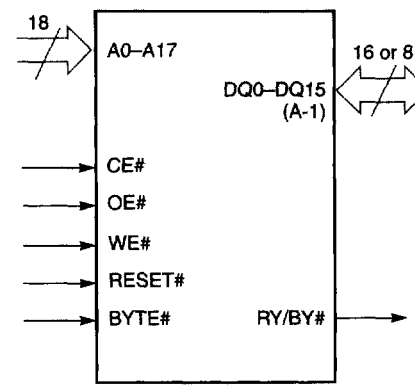
PIN DESCRIPTION

A0–A17 = 18 Addresses
DQ0–DQ14= 15 Data Inputs/Outputs
DQ15/A-1 = DQ15 (Data Input/Output, word mode), A-1 (LSB Address Input, byte mode)
CE# = Chip Enable
OE# = Output Enable
WE# = Write Enable
BYTE# = Selects 8-bit or 16-bit mode
RESET# = Hardware Reset Pin, Active Low
RY/BY# = Ready/Busy Output
V_{CC} = 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{SS} = Device Ground
NC = Pin Not Connected Internally

LOGIC SYMBOL



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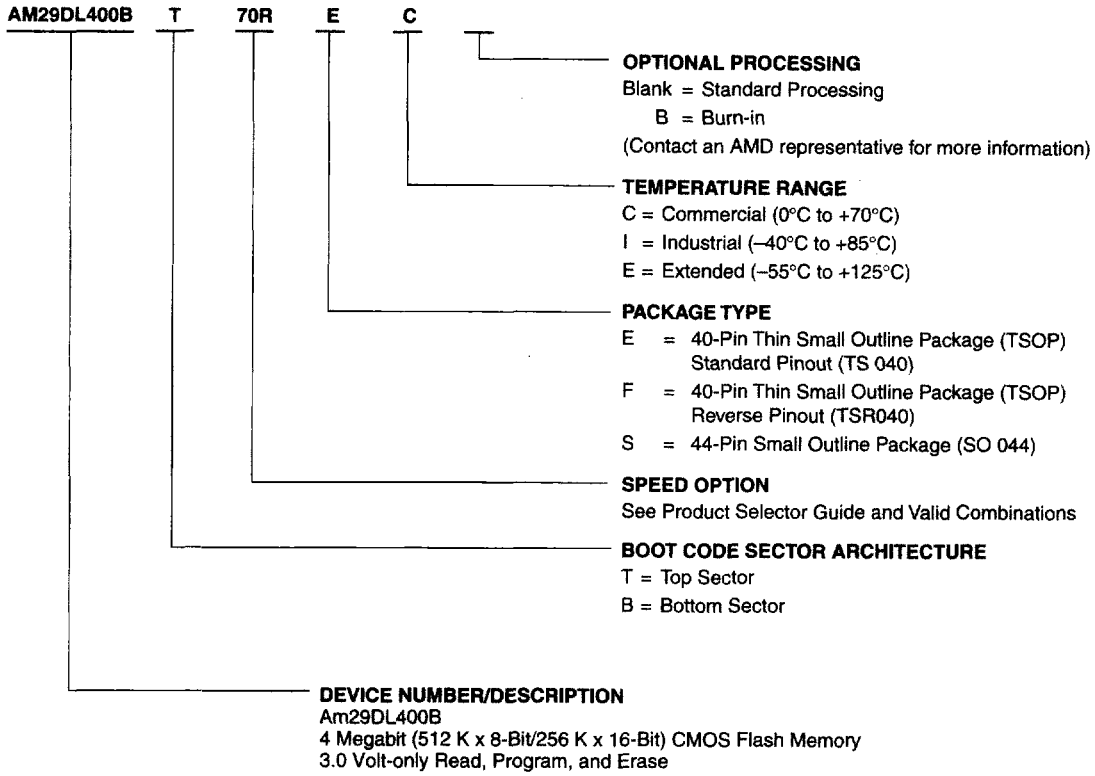
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
AM29DL400BT70R AM29DL400BB70R	EC, EI, FC, FI, SC, SI
AM29DL400BT80 AM29DL400BB80	EC, EI, EE, FC, FI, FE, SC, SI, SE
AM29DL400BT90 AM29DL400BB90	
AM29DL400BT120 AM29DL400BB120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.