

DP8212/DP8212M 8-Bit Input/Output Port

General Description

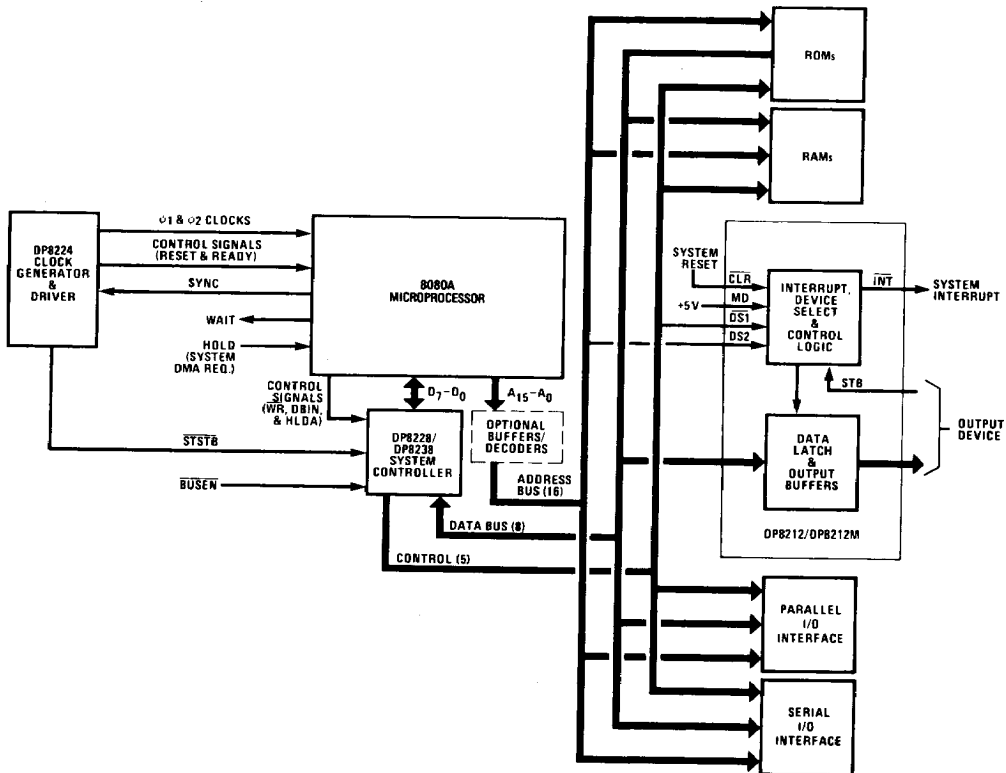
The DP8212/DP8212M is an 8-bit input/output port contained in a standard 24-pin dual-in-line package. The device, which is fabricated using Schottky Bipolar technology, is part of National Semiconductor's 8080A support family. The DP8212/DP8212M can be used to implement latches, gated buffers, or multiplexers. Thus, all of the major peripheral and input/output functions of a microcomputer system can be implemented with this device.

The DP8212/DP8212M includes an 8-bit latch with TRI-STATE® output buffers, and device selection and control logic. Also included is a service request flip-flop for the generation and control of interrupts to the microprocessor.

Features

- 8-Bit data latch and buffer
- Service request flip-flop for generation and control of interrupts
- 0.25 mA input load current
- TRI-STATE TTL output drive capability
- Outputs sink 15 mA
- Asynchronous latch clear
- 3.65V output for direct interface to INS8080A
- Reduces system package count by replacing buffers, latches, and multiplexers in microcomputer systems

8080A Microcomputer Family Block Diagram



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Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +160°C
All Output or Supply Voltages	-0.5V to +7V
All Input Voltages	-1.0V to 5.5V
Output Currents	125 mA
Maximum Power Dissipation* at 25°C	
Cavity Package	1903 mW
Molded Package	2005 mW

*Derate cavity package 12.7 mW/°C above 25°C; derate molded package 16.0 mW/°C above 25°C.

Operating Conditions

	Min	Max	Units
Supply Voltage (V _{CC})			
DP8212M	4.50	5.50	V _{DC}
DP8212	4.75	5.25	V _{DC}
Operating Temperature (T _A)			
DP8212M	-55	+125	°C
DP8212	0	+75	°C

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC electrical characteristics.

Electrical Characteristics Min ≤ T_A ≤ Max, Min ≤ V_{CC} ≤ Max, unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I _F	Input Load Current, STB, DS2, $\overline{\text{CLR}}$, DI ₁ -DI ₈ Inputs	V _F = 0.45V			-0.25	mA
I _F	Input Load Current, MD Input	V _F = 0.45V			-0.75	mA
I _F	Input Load Current, $\overline{\text{DS1}}$ Input	V _F = 0.45V			-1.0	mA
I _R	Input Leakage Current STB, DS2, $\overline{\text{CLR}}$, DI ₁ -DI ₈ Inputs	V _R = V _{CC} Max			10	μA
I _R	Input Leakage Current, MD Input	V _R = V _{CC} Max			30	μA
I _R	Input Leakage Current, $\overline{\text{DS1}}$ Input	V _R = V _{CC} Max			40	μA
V _C	Input Forward Voltage Clamp	I _C = -5 mA			-1	V
V _{IL}	Input "Low" Voltage	DP8212M			0.08	V
		DP8212			0.85	V
V _{IH}	Input "High" Voltage		2.0			V
V _{OL}	Output "Low" Voltage	I _{OL} = 10 mA	DP8212M		0.45	V
		I _{OL} = 15 mA	DP8212		0.45	V
V _{OH}	Output "High" Voltage	I _{OH} = 0.5 mA	DP8212M	3.40	4.0	V
		I _{OH} = 1.0 mA	DP8212	3.65	4.0	V
I _{SC}	Short-Circuit Output Current	V _O = 0V, V _{CC} = 5V	-15		-75	mA
I _O	Output Leakage Current, High Impedance State	V _O = 0.45V/V _{CC} Max			20	μA
I _{CC}	Power Supply Current	DP8212M		90	145	mA
		DP8212		90	130	mA

Capacitance* F = 1 MHz, V_{BIAS} = 2.5V, V_{CC} = 5V, T_A = 25°C

Symbol	Parameter	Min	Typ	Max	Units
C _{IN}	DS1, MD Input Capacitance		9	12	pF
C _{IN}	DS2, $\overline{\text{CLR}}$, STB, DI ₁ -DI ₈ Input Capacitance		5	9	pF
C _{OUT}	DO1-DO8 Output Capacitance		8	12	pF

*This parameter is sampled and not 100% tested.

Switching Characteristics $\text{Min} \leq T_A \leq \text{Max}, \text{Min} \leq V_{CC} \leq \text{Max}$

Symbol	Parameter	Conditions	DP8212M		DP8212		Units
			Min	Max	Min	Max	
t_{PW}	Pulse Width		40		30		ns
t_{PD}	Data to Output Delay	(Note 1)		30		30	ns
t_{WE}	Write Enable to Output Delay	(Note 1)		50		40	ns
t_{SET}	Data Set-Up Time		20		15		ns
t_H	Data Hold Time		30		20		ns
t_R	Reset to Output Delay	(Note 1)		55		40	ns
t_S	Set to Output Delay	(Note 1)		35		30	ns
t_E	Output Enable/Disable Time	(Note 2)		50		45	ns
t_C	Clear to Output Delay	(Note 1)		65		55	ns

Note 1: $C_L = 30 \text{ pF}$

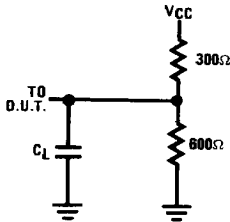
Note 2: $C_L = 30 \text{ pF}$ except for DP8212M

$t_E \text{ (DISABLE) } C_L = 5 \text{ pF}$

Switching Conditions

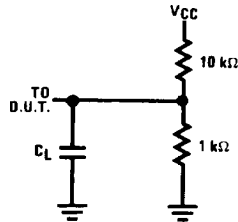
1. Input Pulse Amplitude = 2.5V.
2. Input Rise and Fall Times = 5 ns.
3. Between 1V and 2V Measurements made at 1.5V with 15 mA & 30 pF Test Load.
4. C_L includes jig and probe capacitance.
5. $C_L = 30 \text{ pF}$.
6. $C_L = 30 \text{ pF}$ except for DP8212M $t_E \text{ (DISABLE) } C_L = 5 \text{ pF}$

Test Load



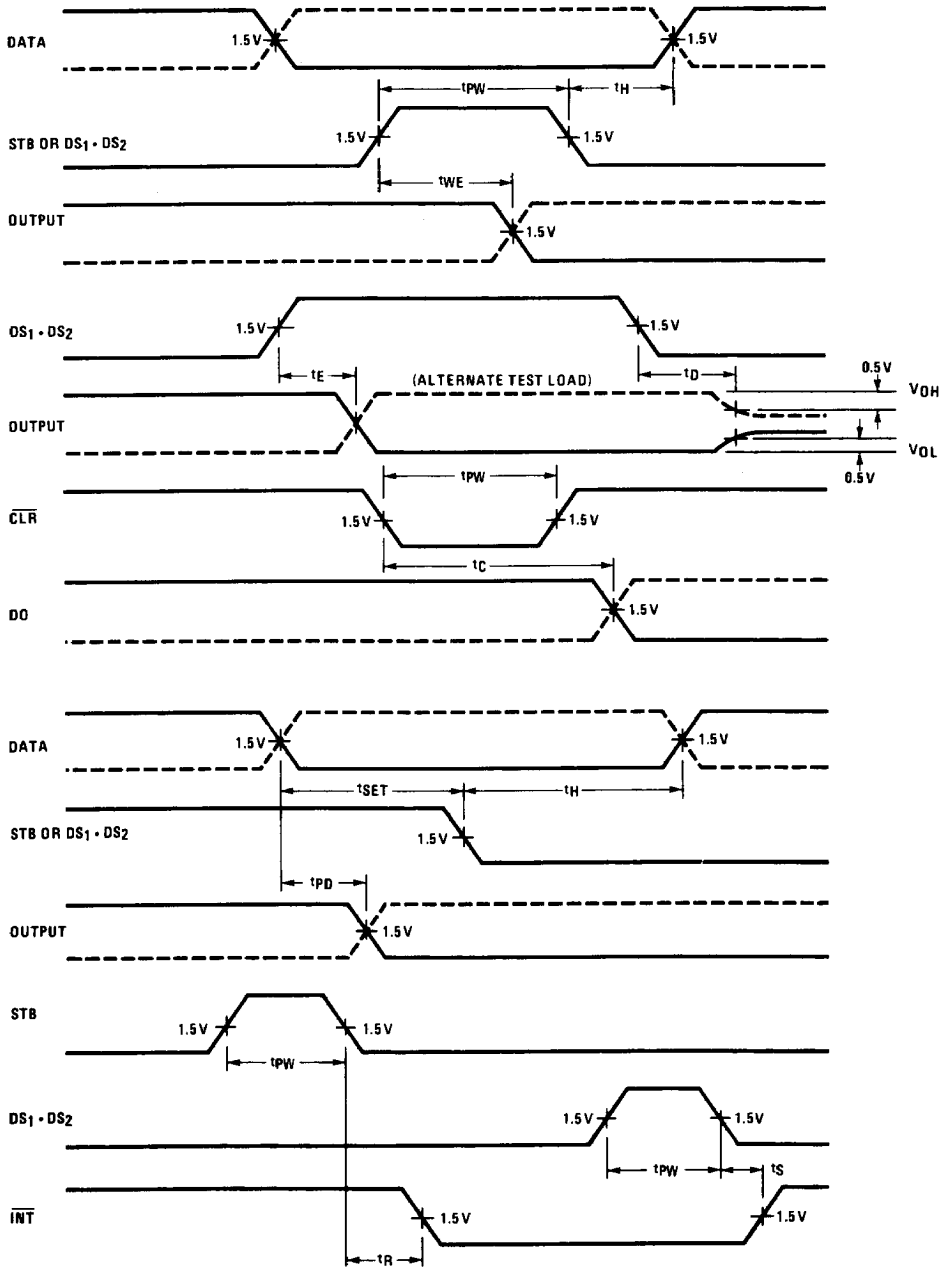
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**Alternate Test Load
(Refer to Timing Diagram)**



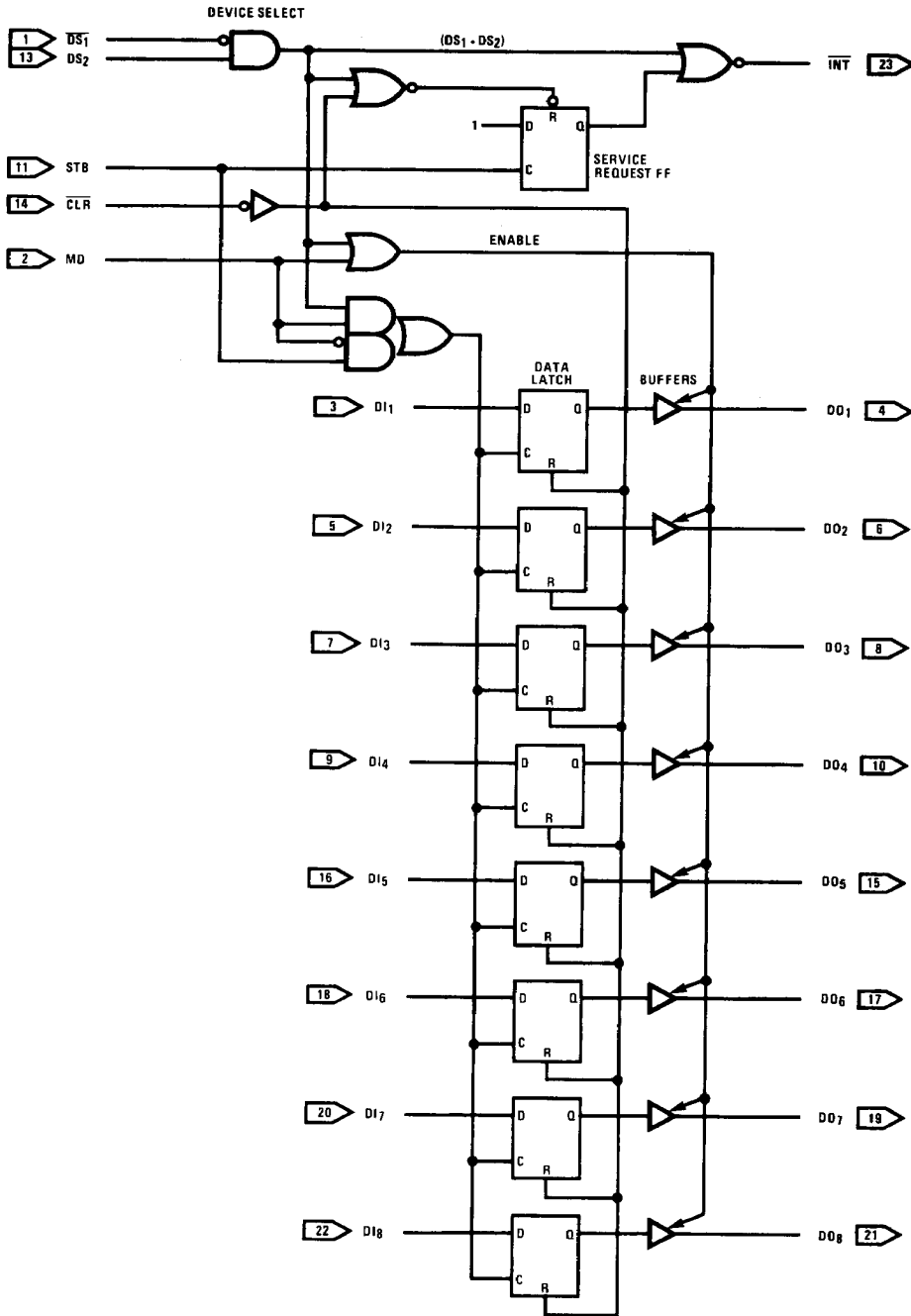
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Timing Diagram



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Logic Diagram



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Logic Tables

Logic Table A

STB	MD	(DS ₁ •DS ₂)	Data Out Equals
0	0	0	TRI-STATE
1	0	0	TRI-STATE
0	1	0	DATA LATCH
1	1	0	DATA LATCH
0	0	1	DATA LATCH
1	0	1	DATA IN
0	1	1	DATA IN
1	1	1	DATA IN

CLR \sim resets data latch to the output low state.

The data latch clock is level sensitive, a low level clock latches the data.

Logic Table B

CLR	(DS ₁ •DS ₂)	STB	Q*	INT
0 RESET	0	0	0	1
1	0	0	0	1
1	0	\sim	1	0
1	1 RESET	0	0	0
1	0	0	0	1

*Internal Service Request flip-flop.

Functional Pin Definitions

The following describes the function of all the DP8212/DP8212M input/output pins. Some of these descriptions reference internal circuits.

INPUT SIGNALS

Device Select (DS₁, DS₂): When $\overline{DS_1}$ is low and DS₂ is high, the device is selected. The output buffers are enabled and the service request flip-flop is asynchronously reset (cleared) when the device is selected.

Mode (MD): When high (output mode), the output buffers are enabled and the source of the data latch clock input is the device selection logic (DS₁ • DS₂). When low (input mode), the state of the output buffers is determined by the device selection logic (DS₁ • DS₂) and the source of the data latch clock input is the strobe (STB) input.

Strobe (STB): Used as data latch clock input when the mode (MD) input is low (input mode). Also used to synchronously set the service request flip-flop, which is negative edge triggered.

Data In (DI₁–DI₈): Eight-bit data input to the data latch, which consists of eight D-type flip-flops. Incorporating a level sensitive clock while the data latch clock input is high, the Q output of each flip-flop follows the data input. When the clock input returns low, the data latch stores the data input. The clock input high overrides the clear (CLR) input data latch reset.

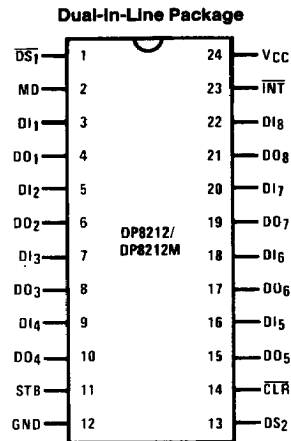
Clear (CLR): When low, asynchronously resets (clears) the data latch and the service request flip-flop. The service request flip-flop is in the non-interrupting state when reset.

OUTPUT SIGNALS

Interrupt (INT): Goes low (interrupting state) when either the service request flip-flop is synchronously set by the strobe (STB) input or the device is selected.

Data Out (DO₁–DO₈): Eight-bit data output of data buffers, which are TRI-STATE, non-inverting stages. These buffers have a common control line that either enables the buffers to transmit the data from the data latch outputs or disables the buffers by placing them in the high-impedance state.

Connection Diagram



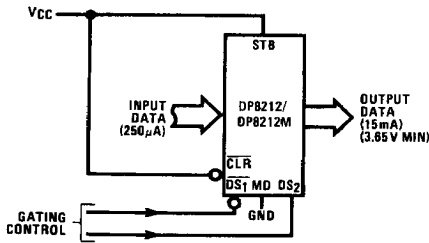
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Top View

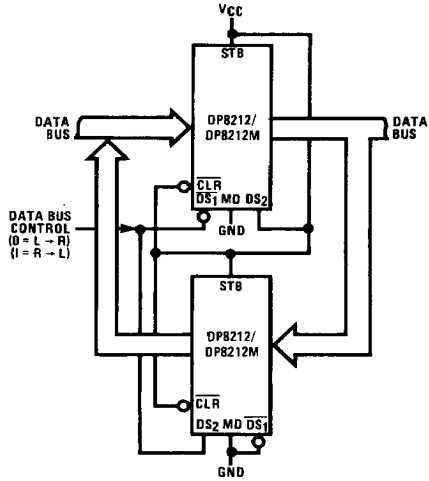
Order Number DP8212J, DP8212N
or DP8212MJ
See NS Package Number J24A or N24A

Applications in Microcomputer Systems

Gated Buffer (TRI-STATE)

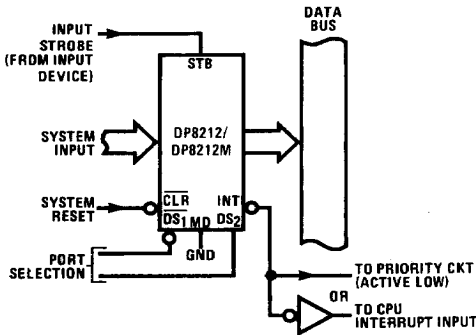


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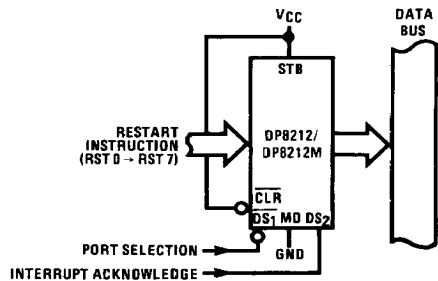
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Interrupting Input Port



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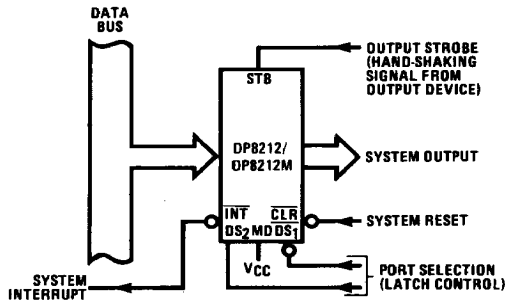
Interrupt Instruction Port



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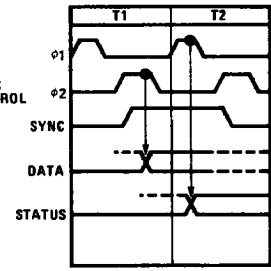
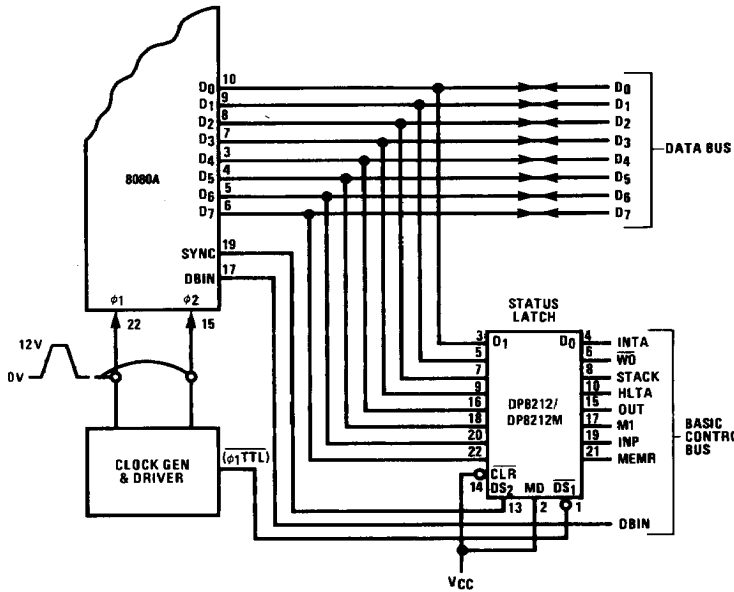
Applications In Microcomputer Systems (Continued)

Output Port (with Hand-Shaking)



TL/F/6824-11

INS8080A Status Latch



TL/F/6824-12