UC1524A
UC2524A
UC3524A

LINEAR INTEGRATED CIRCUITS

PRELIMINARY DATA

ADVANCED REGULATING PULSE WIDTH MODULATORS

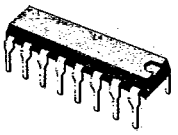
- FULLY INTERCHANGEABLE WITH SG1524
- PRECISION REFERENCE (± 1%)
- HIGH-PERFORMANCE CURRENT LIMITER
- UNDER-VOLTAGE LOCKOUT WITH HYSTERETIC TURN-ON
- START-UP SUPPLY CURRENT LESS THAN 4mA
- OUTPUT CURRENT TO 200mA
- 60V OUTPUT CAPABILITY
- WIDE COMMON-MODE INPUT RANGE FOR BOTH ERROR AND CURRENT LIMIT AMPLIFIERS
- PWM LATCH INSURES SINGLE PULSE PER PERIOD
- 200ns SHUTDOWN THROUGH PWM LATCH
- GUARANTEED FREQUENCY ACCURACY
- THERMAL SHUTDOWN PROTECTION

The UC1524A family of regulating PWM ICs has been designed to retain the same highly versatile architecture of the industry standard SG1524 while offering substantial improvements to many of its limitations. The UC1524A is pin compatible with "non-A" models and in most existing applications can be directly interchanged with no effect on power supply performance. Using the UC1524A, however, frees the designer from many concerns which typically had required additional circuitry to solve.

The UC1524A includes a precise 5V reference trimmed to ± 1% accuracy, eliminating the need for potentiometer adjustments, an error amplifier with an input range which includes 5V, eliminating the need for a reference divider; a current sense amplifier useful in either the ground or power supply output lines; and a pair of 60V, 200mA uncommited transistor switches which greatly enhance output versatility.

An additional feature of the UC1524A is an under-voltage lockout circuit which disables all the internal circuitry, except the reference, until the input voltage has risen to 8V. This holds standby current low until turn-on, greatly simplifying the design of low power, off-line supplies. The turn-on circuit has approximately 600mV of hysteresis for jitter free activation.

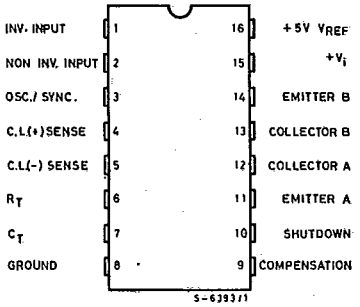
Other product enhancements included in the UC1524A's design include a PWM latch which insures freedom from multiple pulsing within a period even in noisy enviromments and a shutdown circuit feeding directly to the latch which will disable the outputs within 200ns. The oscillator circuit of the UC1524A is usable beyond 500KHz and is now easier to synchronize with an external clock pulse.



DIP-16
(Plastic and Ceramic)

CONNECTION DIAGRAM AND ORDERING NUMBERS

(top view)



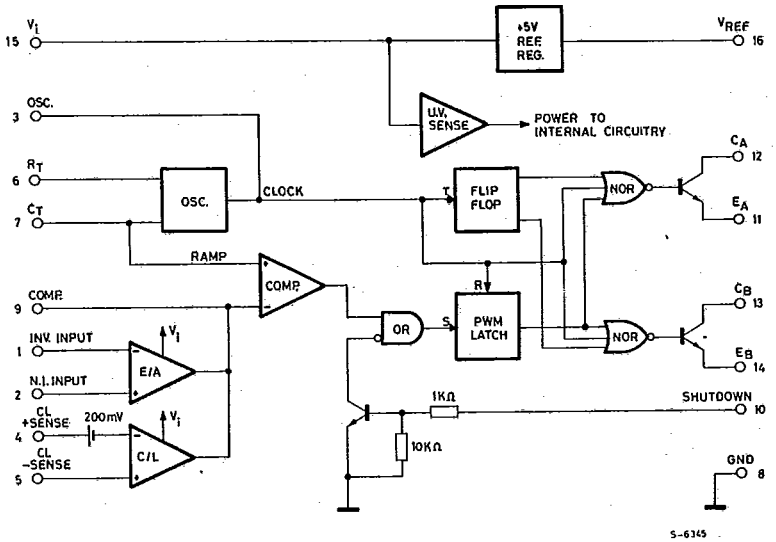
Type	Plastic	Ceramic
UC1524A	—	UC1524AJ
UC2524A	UC2524AN	UC2524AJ
UC3524A	UC3524AN	UC3524AJ

UC1524A
UC2524A
UC3524A

ABSOLUTE MAXIMUM RATINGS

V_i	Supply voltage		40	V
V_C	Collector supply voltage:	**UC1524A, UC2524A**	60	V
		UC3524A	50	V
I_C	Collector output current (each output)		200	mA
I_R	Reference output current		50	mA
I_T	Current through C_T terminal		-5	mA
P_{tot}	Total power dissipation at $T_{amb} = 70°C$		1000	mW
T_j	Junction temperature range		-55 to 125	°C
T_{stg}	Storage temperature range		-65 to 150	°C
T_{op}	Operating ambient temperature range	**UC1524A**	-55 to 125	°C
		UC2524A	-25 to 85	°C
		UC3524A	0 to 70	°C

BLOCK DIAGRAM



THERMAL DATA

$R_{th\,j\text{-}amb}$	Thermal resistance junction-ambient	max.	80	°C/W

UC1524A
UC2524A
UC3524A

ELECTRICAL CHARACTERISTICS (Unless otherwise stated, these specifications apply from T_{amb} = -55 to 125°C for the UC1524A, -25 to 85°C for the UC2524A, and 0 to 70°C for the UC3524A; $V_i = V_C = 20V$

Parameter		Test conditions	UC1524A UC2524A			UC3524A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
TURN-ON CHARACTERISTICS									
V_I	Input voltage	Operating range after Turn-on	8		40	8		40	V
	Turn-on threshold		5.5	7.5	8.5	5.5	7.5	8.5	V
	Turn-on current	V_I = 6V		2.5	4		2.5	4	mA
I_q	Operating current	V_I = 8 to 40V		5	10		5	10	mA
*	Turn-on hysteresis			0.6			0.6		V
REFERENCE SECTION									
V_{REF}	Output voltage	T_j = 25°C	4.95	5	5.05	4.9	5	5.1	V
ΔV_{REF}	Line regulation	V_I = 10 to 40V		10	20		10	30	mV
ΔV_{REF}	Load regulation	I_L = 0 to 20mA		20	50		20	50	mV
$\Delta V_{REF}/\Delta T$*	Temperature stability	Over operating range		20	50		20	50	mV
	Short circuit current	V_{REF} = 0 T_j = 25°C		80	100		80	100	mA
*	Output noise voltage	10Hz ≤ f ≤ 10KHz, T_j = 25°C		40			40		μV_{rms}
ΔV_{REF}*	Long term stability	T_j = 125°C 1000Hrs		20	50		20	50	mV
OSCILLATOR SECTION (Unless otherwise specified, R_T = 2700Ω, C_T = 0.01μF									
	Initial accuracy	T_j = 25°C	41	43	45	39	43	47	KHz
$\Delta f/\Delta T$*	Temperature stability	Over op. temp. range		1	2		1	2	%
f_{min}	Minimum frequency	R_T = 150KΩ, C_T = 0.1μF			140			120	Hz
f_{max}	Maximum frequency	R_T = 2KΩ, C_T = 470pF	500			500			KHz
*	Output amplitude	T_j = 25°C		3.5			3.5		V
*	Output pulse width	T_j = 25°C		0.5			0.5		μs
	Ramp peak		3.3	3.5	3.7	3.3	3.5	3.7	V
	Ramp valley	T_j = 25°C	0.7	0.8	0.9	0.7	0.8	0.9	V
ERROR AMPLIFIER SECTION (unless otherwise specified, V_{CM} = 2.5V)									
V_{OS}	Input offset voltage			0.5	5		2	10	mV
I_b	Input bias current			1	5		1	10	μA
I_{OS}	Input offset current			0.05	1		0.5	1	μA
CMR	Common mode rejection	V_{CM} = 1.5 to 5.5V	60	75		60	75		dB
PSR	Power supply rejection	V_I = 10 to 40V	50	60		50	60		dB

UC1524A
UC2524A
UC3524A

ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions	UC1524A UC2524A			UC3524A			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_O	Output swing	Minimum total range	0.5		5	0.5		5	V
G_V	Open loop voltage gain	ΔV_O= 1 to 4V $R_L \geq$ 10MΩ	72	80		60	80		dB
B *	Gain-bandwidth	T_j = 25°C G_V = 0dB	1	3		1	3		MHz
	DC Transconduct *†	T_j = 25°C, 30kΩ ≤ R_L ≤ 1MΩ	1.7	2.3		1.7	2.3		mS
CURRENT LIMIT AMPLIFIER (Unless otherwise specified, pin 5 = 0V)									
V_{OS}	Input offset voltage	T_j=25°C, E/A set for Max. Out.	190	200	210	180	200	220	mV
V_{OS}	Input offset voltage	over op. temp. range	180		220	170		230	mV
I_b	Input bias current			-1	-10		-1	-10	μA
CMR	Common mode rejection	$V_{(pin\ 5)}$ = -0.3 to 5.5V	50	60		50	60		dB
PSR	Power supply rejection	V_I = 10 to 40V	50	60		50	60		dB
V_O	Output swing	Minimum total range	0.5		5	0.5		5	V
G_V	Open loop volt. gain	ΔV_O= 1 to 4V, $R_L \geq$ 10MΩ	70	80		70	80		dB
t_d *	Delay time	pin 4 to pin 9, ΔV_I=300mV		300			300		ns
OUTPUT SECTION (Each output)									
V_{CE}	Collector-emitter voltage	I_C = 100μA	60	80		50	80		V
I_C	Collector leakage current	V_{CE} = 50V		0.1	20		0.1	20	μA
V_{sat}	Saturation voltage	I_C = 20mA I_C = 200mA		0.2 1	0.4 2.2		0.2 1	0.4 2.2	V V
V_{EO}	Emitter output voltage	I_E = 50mA	17	18		17	18		V
t_r*	Rise time	T_j = 25°C R = 2KΩ		200			200		ns
t_f *	Fall time	Tj = 25°C R = 2KΩ		100			100		ns
*	Comparator delay	T_j = 25°C, pin 9 to output		300			300		ns
*	Shutdown delay	T_j = 25°C, pin 10 to output		200			200		ns
	Shutdown threshold	T_j= 25°C R_C = 2KΩ	0.5	0.7	1	0.5	0.7	1	V
	Thermal shutdown			165			165		°C

* These parameters are guaranteed by design but not 100% tested in production
† DC transconductance (g_M) relates to DC open-loop voltage gain according to the following equation $G_V = g_M R_L$ where R_L in the resistance from pin 9 to ground.
The minimum g_M specification is used to calculate minimum G_V when the error amplifier output is loaded.

UC1524A
UC2524A
UC3524A

Fig. 1 - Supply current vs. input voltage

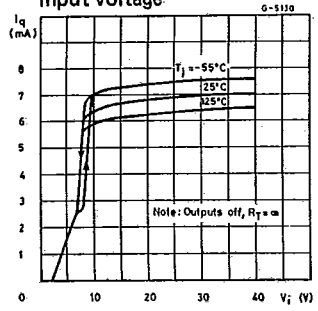


Fig. 2 - Error amplifier voltage gain vs. frequency

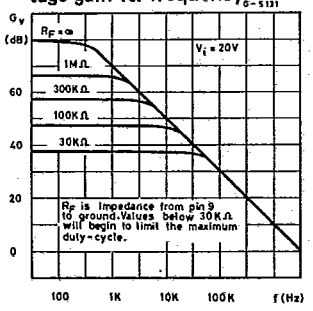


Fig. 3 - PWM duty cycle vs. V_g (one output)

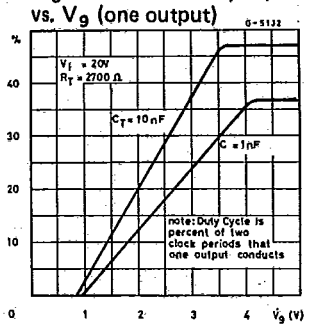


Fig. 4 - Oscillator frequency vs. timing components

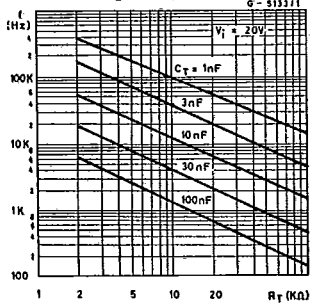


Fig. 5 - Output dead time vs. timing capacitor value

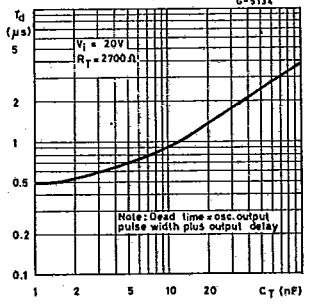


Fig. 6 - Output saturation voltage

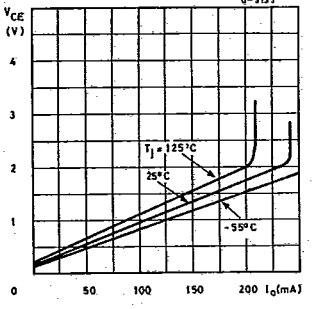


Fig. 7 - Current limit amplifier delay

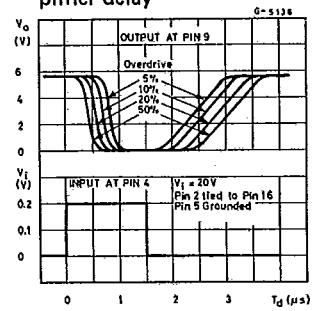


Fig. 8 - Shutdown delay from PWM comparator - pin 9

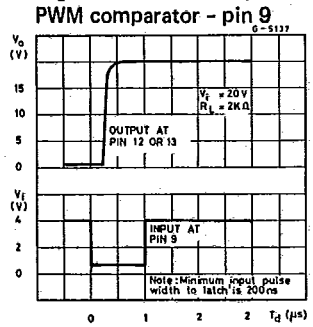
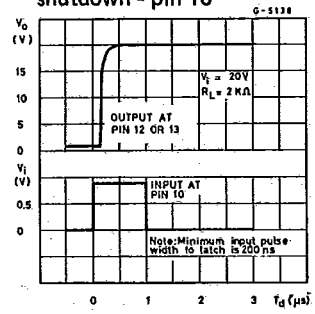


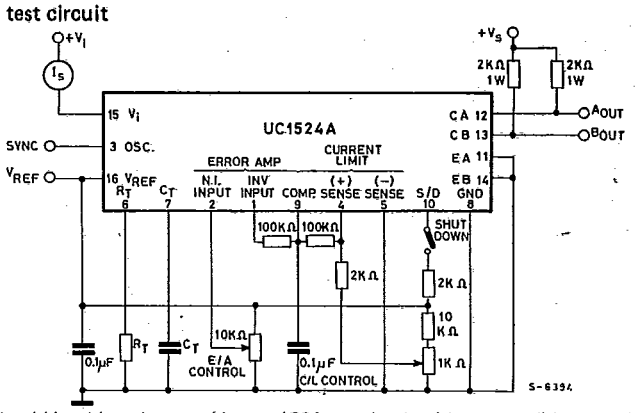
Fig. 9 - Turn-off delay from shutdown - pin 10



UC1524A
UC2524A
UC3524A

APPLICATION INFORMATION

Fig. 10 - Open-loop test circuit



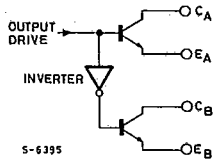
Note : The UC1524A should be able to be tested in any 1524 test circuit with two possible exceptions:

1. The higher gain-bandwidth of the current limit amplifier in the UC1524A may cause oscillations in an uncompensated 1524 test circuit.
2. The effect of the shutdown, pin 10, cannot be seen at the compensation terminal, pin 9, but must be observed at the outputs

OUTPUT STAGES

The outputs are NPN transistors, capable of a maximum current of 200mA. These transistors are driven 180° out of phase and have non-committed open collectors and emitters as shown in figure 11

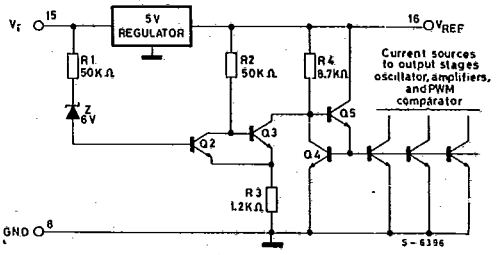
Fig. 11



Internal power turn-on circuit

The under-voltage lockout and turn-on hysteresis circuit is shown in Fig. 12. This circuit requires approximately 2V for activation; and, since nothing else will turn on without at least 3V of supply voltage, lockout is assured. When V_I rises above 2V, R2 begins to conduct saturating Q_3 and holding the base of Q_5 too low to allow any of the current sources to conduct. The current through R_4 flows through Q3 and R_3 developing a 600mV drop across R_3 when V_{REF} reaches 5V. At this level, the only current flowing is that used by the reference regulator and R_2 and R_4, a total of approximately 2.5mA at turn-on threshold. When the input reaches approximately 8V, diode, Z begins to conduct turning on Q_2 which turns off Q_3 and allows the current sources to activate. Since the current through Q_2 is much less than through Q_3, the voltage across R_3 drops providing positive feedback. **This gives about 600mV of hysteresis.** This circuit, of course, works in reverse at turn off, ensuring that the outputs can only operate when the supply is adequate for fully predictable operation. Figure 1 shows the relation-ship between quiescent current and input voltage. Designers should find this low current start-up characteristic quite advantageous for off-line, primary-side control with bootstrapped operation after turn on.

Fig. 12



UC1524A
UC2524A
UC3524A

APPLICATION INFORMATION (continued)

Fig. 13 - Single 5V-10A regulator

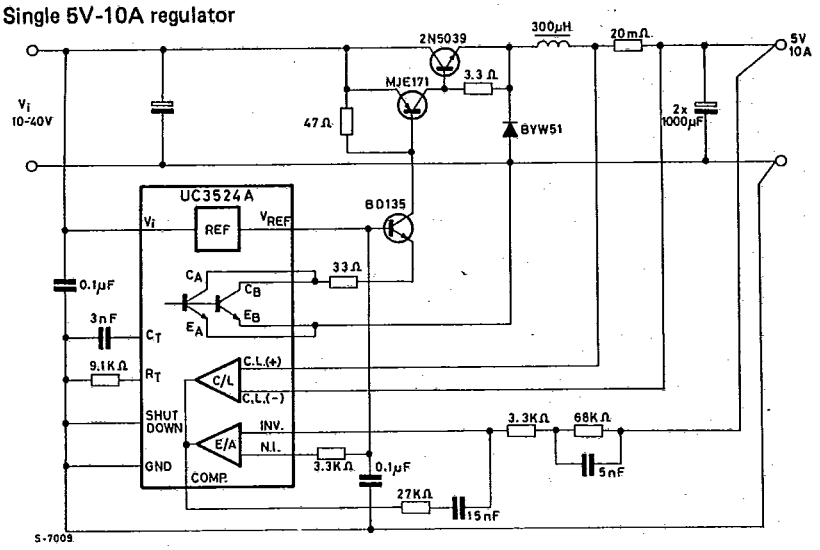
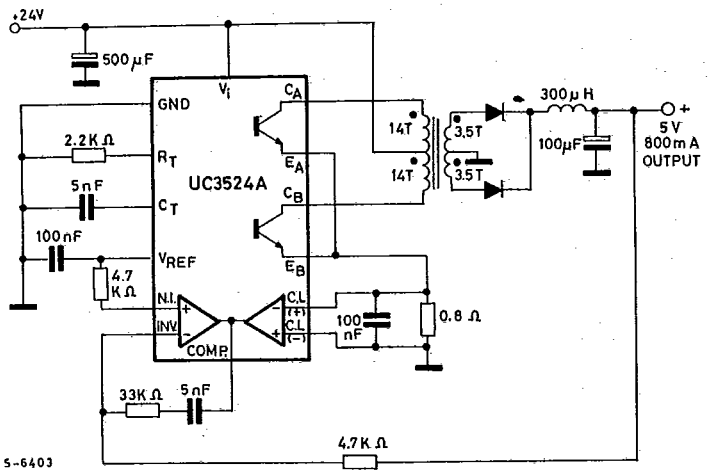


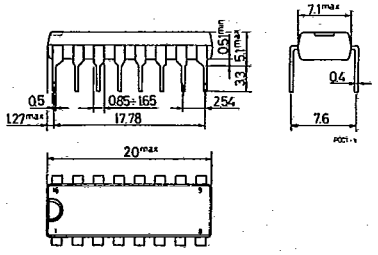
Fig. 14 - 4W DC-DC converter. With higher output voltage and current capability the UC3524A can implement a complete converter with no external transistors.



UC1524A
UC2524A
UC3524A

MECHANICAL DATA (Dimensions in mm)

DIP-16 (Plastic)



DIP-16 (Ceramic)