DS36277

DS36277 Dominant Mode Multipoint Transceiver

Literature Number: SNLS086D

National Semiconductor

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DS36277
Dominant Mode Multipoint Transceiver

General Description

The DS36277 Dominant Mode Multipoint Transceiver is designed for use on bi-directional differential busses. It is optimal for use on Interfaces that utilize Society of Automotive Engineers (SAE) J1708 Electrical Standard.

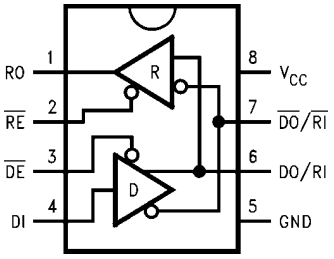
The device is similar to standard TIA/EIA-485 transceivers, but differs in enabling scheme. The Driver's Input is normally externally tied LOW, thus providing only two states: Active (LOW), or Disabled (OFF). When the driver is active, the dominant mode is LOW, conversely, when the driver is disabled, the bus is pulled HIGH by external bias resistors.

The receiver provides a FAILSAFE feature that guarantees a known output state when the Interface is in the following conditions: Floating Line, Idle Line (no active drivers), and Line Fault Conditions (open or short). The receiver output is HIGH for the following conditions: Open Inputs, Terminated Inputs (50Ω), or Shorted Inputs. FAILSAFE is a highly desirable feature when the transceivers are used with Asynchronous Controllers such as UARTs.

Features

- FAILSAFE receiver, RO = HIGH for:
  - OPEN inputs
  - Terminated inputs
  - SHORTED inputs
- Optimal for use in SAE J1708 Interfaces
- Compatible with popular interface standards:
  - TIA/EIA-485 and TIA/EIA-422-A
  - CCITT recommendation V.11
- Bi-directional transceiver
  - Designed for multipoint transmission
- Wide bus common mode range
  - (−7V to +12V)
- Available in plastic DIP and SOIC packages

Connection and Logic Diagram



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Order Number DS36277TM or DS36277TN
See NS Package Number M08A or N08E

Truth Table

Driver

Inputs		Outputs	
$\overline{DE}$	DI	DO/RI	$\overline{DO}$ /$\overline{RI}$
L	L	L	H
L	H	H	L
H	X	Z	Z

Receiver

Inputs		Output
$\overline{RE}$	DO/RI–$\overline{DO}$ /$\overline{RI}$	RO
L	≥ 0 mV	H
L	≤ −500 mV	L
L	SHORTED	H
L	OPEN	H
H	X	Z

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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	7V
Input Voltage ($\overline{DE}$, $\overline{RE}$, and DI)	5.5V
Driver Output Voltage/ Receiver Input Voltage	−10V to +15V
Receiver Output Voltage (RO)	5.5V
Maximum Package Power Dissipation @ +25°C	
N Package (derate 9.3 mW/°C above +25°C)	1168 mW
M Package (derate 5.8 mW/°C above +25°C)	726 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 4 sec.)	260°C
ESD Rating (HBM, 1.5 kΩ, 100 pF)	7.0 kV

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Voltage	−7	+12	V
Operating Temperature (T_A)			
DS36277T	−40	+85	°C

Electrical Characteristics (Notes 2, 4)

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions			Min	Typ	Max	Units
DRIVER CHARACTERISTICS								
V_{OD}	Differential Output Voltage	I_O = 0 mA (No Load)			1.5	3.6	6	V
V_{oDO}	Output Voltage	I_O = 0 mA (Output to GND)			0		6	V
$V_{o\overline{DO}}$	Output Voltage				0		6	V
V_{T1}	Differential Output Voltage (Termination Load)	R_L = 54Ω (485)	(*Figure 1*)		1.3	2.2	5.0	V
		R_L = 100Ω (422)			1.7	2.6	5.0	V
ΔV_{T1}	Balance of V_{T1}	R_L = 54Ω	(Note 3)		−0.2		0.2	V
	$\lvert V_{T1} - \overline{V_{T1}} \rvert$	R_L = 100Ω			−0.2		0.2	V
V_{OS}	Driver Common Mode Output Voltage	R_L = 54Ω	(*Figure 1*)		0	2.5	3.0	V
		R_L = 100Ω			0	2.5	3.0	V
ΔV_{OS}	Balance of V_{OS}	R_L = 54Ω	(Note 3)		−0.2		0.2	V
	$\lvert V_{OS} - \overline{V_{OS}} \rvert$	R_L = 100Ω			−0.2		0.2	V
V_{OH}	Output Voltage High	I_{OH} = −22 mA	(*Figure 2*)		2.7	3.7		V
V_{OL}	Output Voltage Low	I_{OL} = +22 mA				1.3	2	V
I_{OSD}	Driver Short-Circuit Output Current	V_O = +12V	(*Figure 3*)			92	290	mA
		V_O = −7V				−187	−290	mA
RECEIVER CHARACTERISTICS								
V_{TH}	Differential Input High Threshold Voltage (Note 5)	$V_O = V_{OH}$, I_O = −0.4 mA −7V ≤ V_{CM} ≤ +12V				−0.150	0	V
V_{TL}	Differential Input Low Threshold Voltage (Note 5)	$V_O = V_{OL}$, I_O = 8.0 mA −7V ≤ V_{CM} ≤ +12V			−0.5	−0.230		V
V_{HST}	Hysteresis (Note 6)	V_{CM} = 0V				80		mV
I_{IN}	Line Input Current (V_{CC} = 4.75V, 5.25V, 0V)	Other Input = 0V	V_I = +12V			0.5	1.5	mA
		$\overline{DE}$ = V_{IH} (Note 7)	V_I = −7V			−0.5	−1.5	mA
I_{OSR}	Short Circuit Current	V_O = 0V		RO	−15	−32	−85	mA
I_{OZ}	TRI-STATE® Leakage Current	V_O = 0.4 to 2.4V			−20	1.4	+20	µA
V_{OH}	Output High Voltage (*Figure 12*)	V_{ID} = 0V, I_{OH} = −0.4 mA			2.3	3.7		V
		V_{ID} = OPEN, I_{OH} = −0.4 mA			2.3	3.7		V
V_{OL}	Output Low Voltage (*Figure 12*)	V_{ID} = −0.5V, I_{OL} = +8 mA				0.3	0.7	V
		V_{ID} = −0.5V, I_{OL} = +16 mA				0.3	0.8	V
R_{IN}	Input Resistance				10	20		kΩ

Symbol	Parameter	Conditions		Min	Typ	Max	Units
DEVICE CHARACTERISTICS							
V_{IH}	High Level Input Voltage		$\overline{DE}$, $\overline{RE}$, or DI	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IH}	High Level Input Current	V_{IH} = 2.4V				20	µA
I_{IL}	Low Level Input Current	V_{IL} = 0.4V				−100	µA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA			−0.7	−1.5	V
I_{CC}	Output Low Voltage	$\overline{DE}$ = 0V, $\overline{RE}$ = 0V, DI = 0V			39	60	mA
I_{CCR}	Supply Current	$\overline{DE}$ = 3V, $\overline{RE}$ = 0V, DI = 0V			24	50	mA
I_{CCD}	(No Load)	$\overline{DE}$ = 0V, $\overline{RE}$ = 3V, DI = 0V			40	75	mA
I_{CCX}		$\overline{DE}$ = 3V, $\overline{RE}$ = 3V, DI = 0V			27	45	mA

Switching Characteristics (Note 4)

Over recommended Supply Voltage and Operating Temperature ranges, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DRIVER CHARACTERISTICS						
t_{PLHD}	Diff. Prop. Delay Low to High	R_L = 54Ω	8	17	60	ns
t_{PHLD}	Diff. Prop. Delay High to Low	C_L = 50 pF	8	19	60	ns
t_{SKD}	Diff. Skew ($\lvert t_{PLHD} - t_{PHLD} \rvert$)	C_D = 50 pF		2	10	ns
t_r	Diff. Rise Time	(*Figures 4*, *5*)		11	60	ns
t_f	Diff. Fall Time			11	60	ns
t_{PLH}	Prop. Delay Low to High	R_L = 27Ω, C_L = 15 pF		22	85	ns
t_{PHL}	Prop. Delay High to Low	(*Figures 6*, *7*)		25	85	ns
t_{PZH}	Enable Time Z to High	R_L = 110Ω		25	60	ns
t_{PZL}	Enable Time Z to Low	C_L = 50 pF		30	60	ns
t_{PHZ}	Disable Time High to Z	(*Figure 8 – Figure 11*)		16	60	ns
t_{PLZ}	Disable Time Low to Z			11	60	ns
RECEIVER CHARACTERISTICS						
t_{PLH}	Prop. Delay Low to High	V_{ID} = −1.5V to +1.5V	15	37	90	ns
t_{PHL}	Prop. Delay High to Low	C_L = 15 pF	15	43	90	ns
t_{SK}	Skew ($\lvert t_{PLH} - t_{PHL} \rvert$)	(*Figures 13*, *14*)		6	15	ns
t_{PZH}	Enable Time Z to High	C_L = 15 pF		12	60	ns
t_{PZL}	Enable Time Z to Low	(*Figures 15*, *16*)		28	60	ns
t_{PHZ}	Disable Time High to Z			20	60	ns
t_{PLZ}	Disable Time Low to Z			10	60	ns

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the devices should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground unless otherwise specified.

Note 3: $\Delta \lvert V_{T1} \rvert$ and $\Delta \lvert V_{OS} \rvert$ are changes in magnitude of V_{T1} and V_{OS}, respectively, that occur when the input changes state.

Note 4: All typicals are given for V_{CC} = 5.0V and T_A = +25°C.

Note 5: Threshold parameter limits specified as an algebraic value rather than by magnitude.

Note 6: Hysteresis defined as $V_{HST} = V_{TH} - V_{TL}$.

Note 7: I_{IN} includes the receiver input current and driver TRI-STATE leakage current.

Parameter Measurement Information

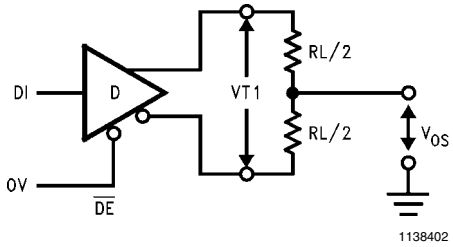


FIGURE 1. Driver V_{T1} and V_{OS} Test Circuit

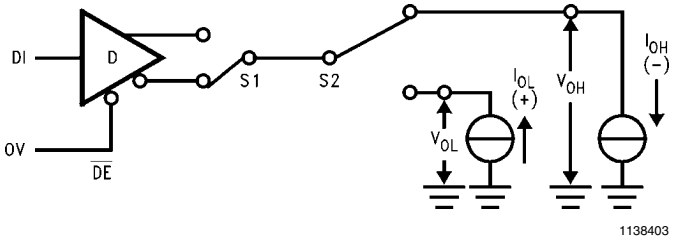


FIGURE 2. Driver V_{OH} and V_{OL} Test Circuit

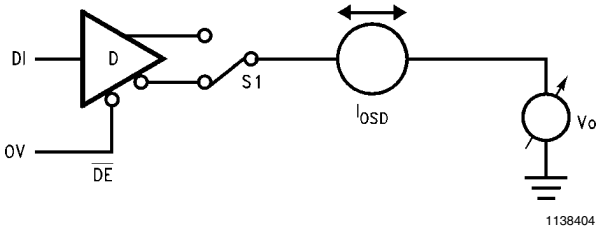


FIGURE 3. Driver Short Circuit Test Circuit

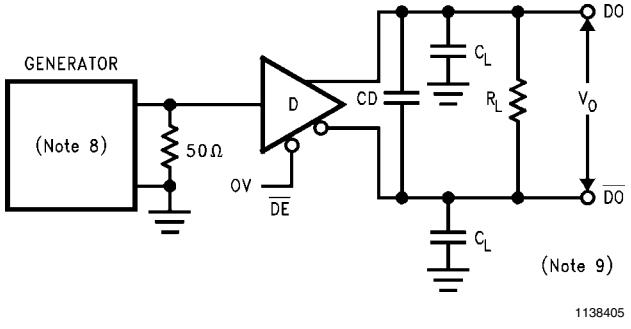


FIGURE 4. Driver Differential Propagation Delay and Transition Time Test Circuit

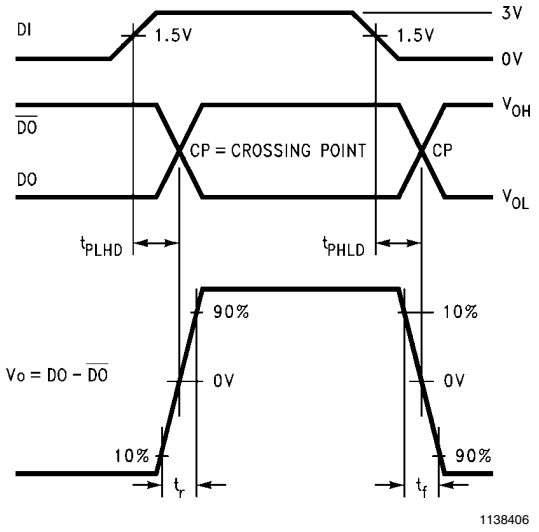


FIGURE 5. Driver Differential Propagation Delays and Transition Times

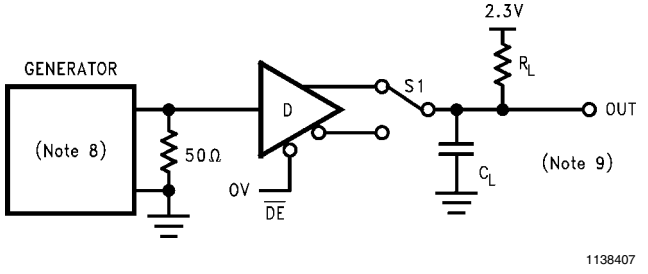


FIGURE 6. Driver Propagation Delay Test Circuit

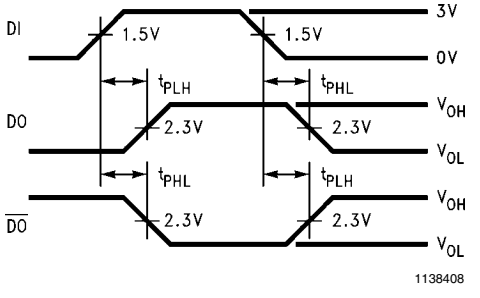
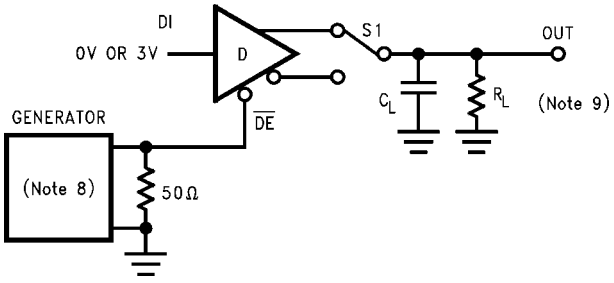


FIGURE 7. Driver Propagation Delays



S1 to DO for DI = 3V
S1 to $\overline{DO}$ for DI = 0V

FIGURE 8. Driver TRI-STATE Test Circuit (t_{PZH}, t_{PHZ})

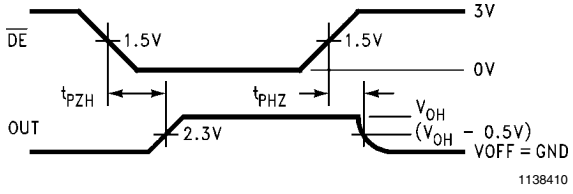
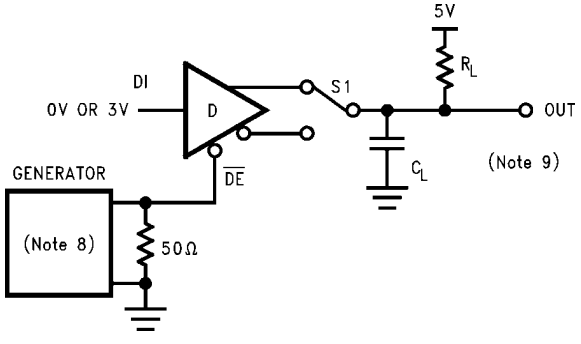


FIGURE 9. Driver TRI-STATE Delays (t_{PZH}, t_{PHZ})



S1 to DO for DI = 0V
S1 to $\overline{DO}$ for DI = 3V

FIGURE 10. Driver TRI-STATE Test Circuit (t_{PZL}, t_{PLZ})

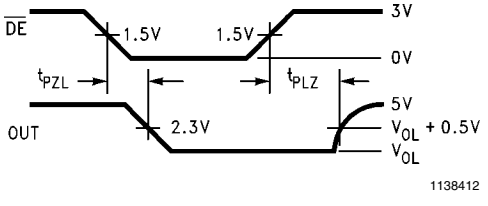


FIGURE 11. Driver TRI-STATE Delays (t_{PZL}, t_{PLZ})

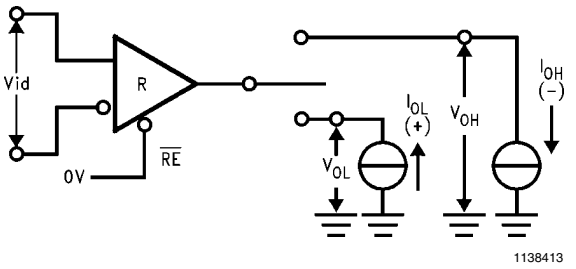


FIGURE 12. Receiver V_{OH} and V_{OL}

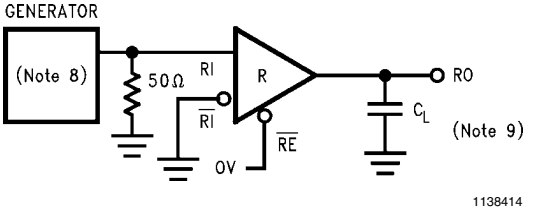


FIGURE 13. Receiver Propagation Delay Test Circuit

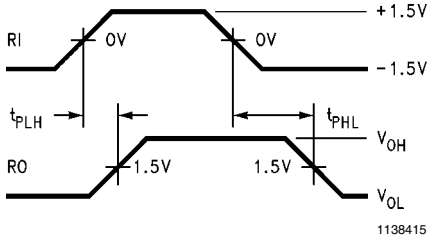


FIGURE 14. Receiver Propagation Delays

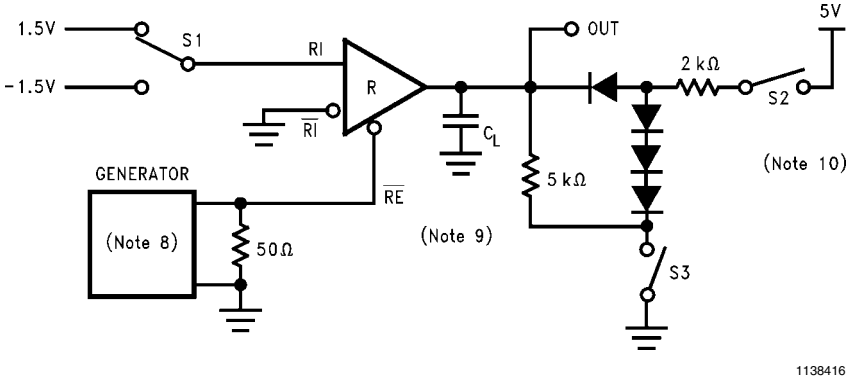
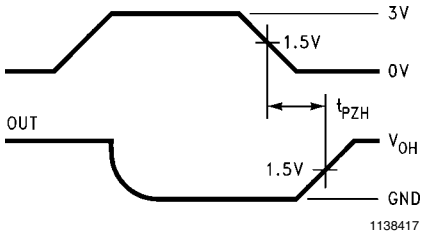
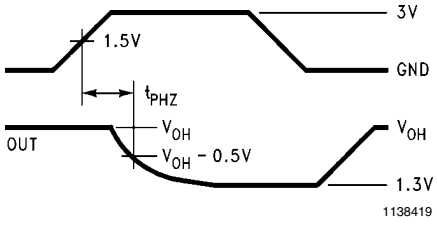


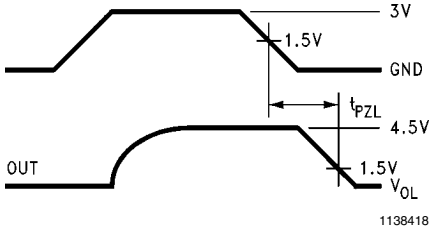
FIGURE 15. Receiver TRI-STATE Delay Test Circuit



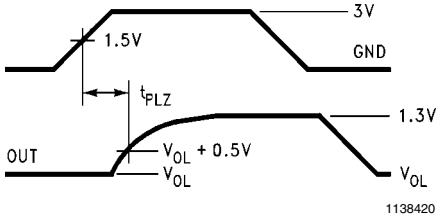
S1 1.5V
S2 OPEN
S3 CLOSED



S1 1.5V
S2 CLOSED
S3 CLOSED



S1 –1.5V
S2 CLOSED
S3 OPEN



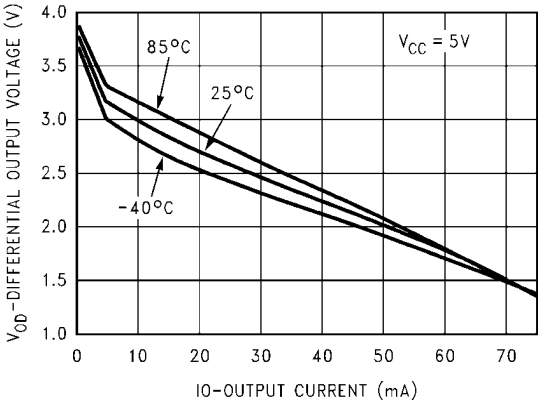
S1 –1.5V
S2 CLOSED
S3 CLOSED

FIGURE 16. Receiver Enable and Disable Timing

Note 8: The input pulse is supplied by a generator having the following characteristics: f = 1.0 MHz, 50% duty cycle, t_r and t_f < 6.0 ns, Z_O = 50Ω.
Note 9: C_L includes probe and stray capacitance.
Note 10: Diodes are 1N916 or equivalent.

Typical Performance Characteristics

Differential Output Voltage vs Output Current



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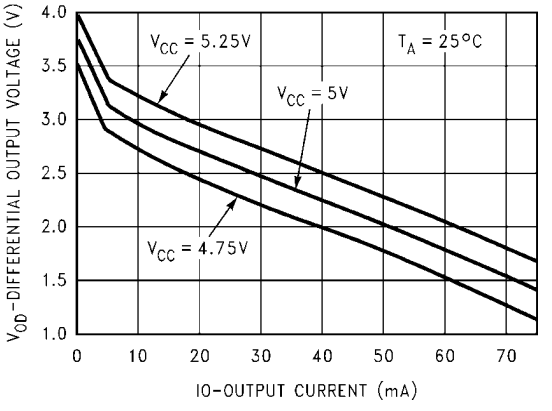
Differential Output Voltage vs Output Current



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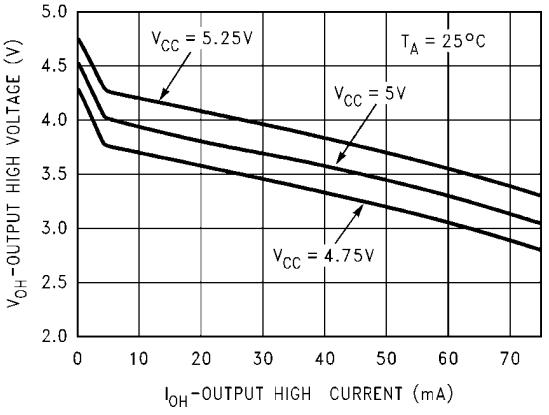
Driver V_{OH} vs I_{OH} vs V_{CC}



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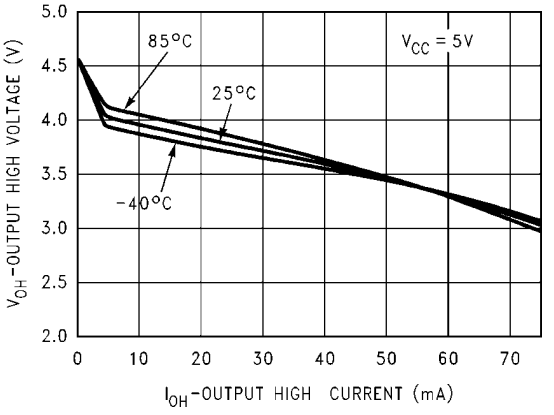
Driver V_{OH} vs I_{OH} vs Temperature



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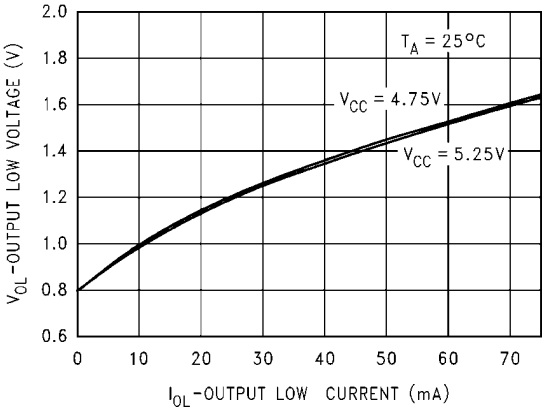
Driver V_{OL} vs I_{OL} vs V_{CC}



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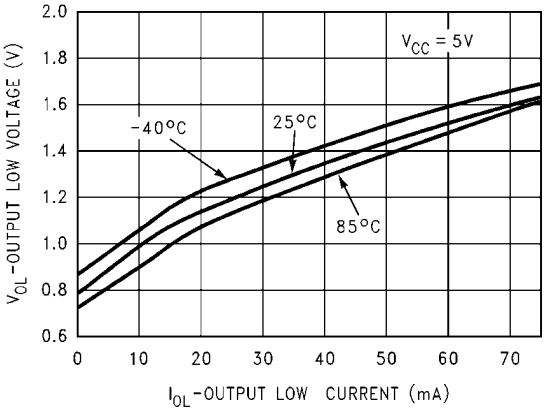
Driver V_{OL} vs I_{OL} vs Temperature



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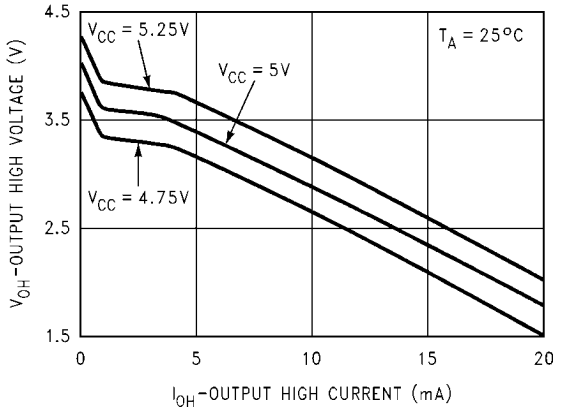
Receiver V_{OH} vs I_{OH} vs V_{CC}



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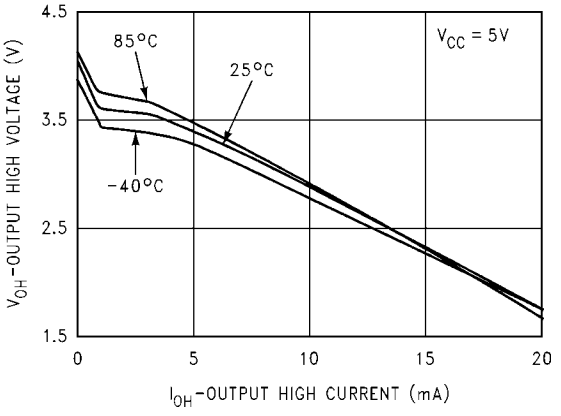
Receiver V_{OH} vs I_{OH} vs Temperature



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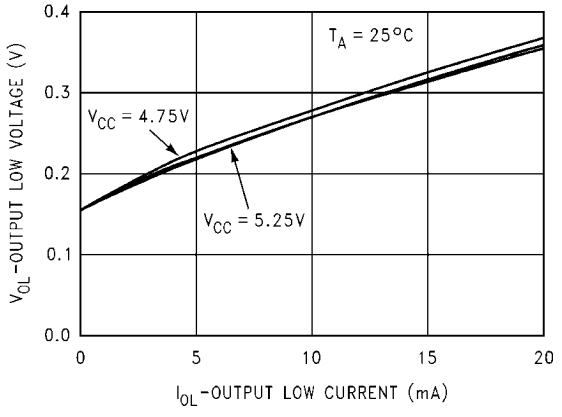
Receiver V_{OL} vs I_{OL} vs V_{CC}



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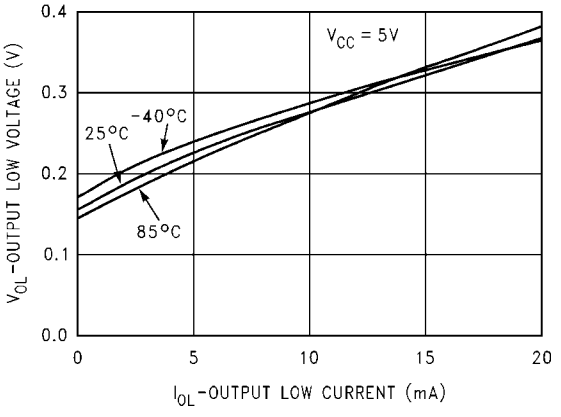
Receiver V_{OL} vs I_{OL} vs Temperature



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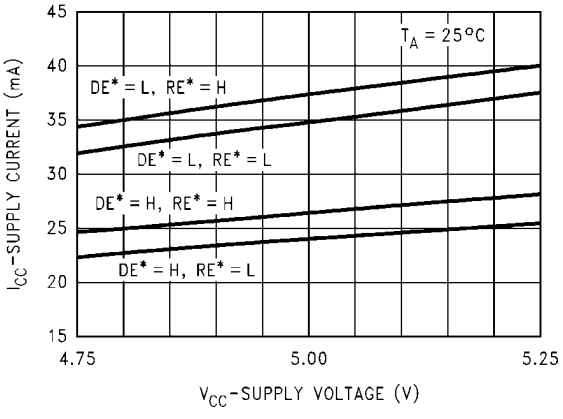
Supply Current vs Supply Voltage



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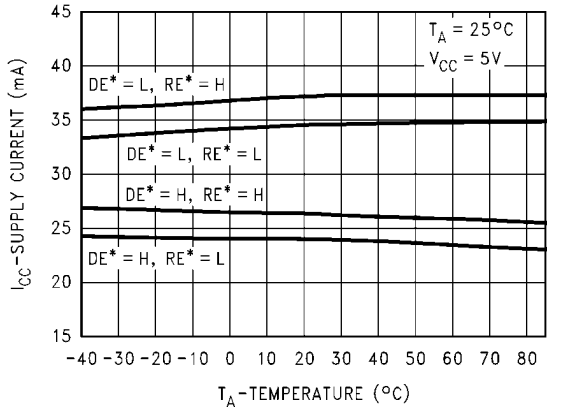
Supply Current vs Temperature



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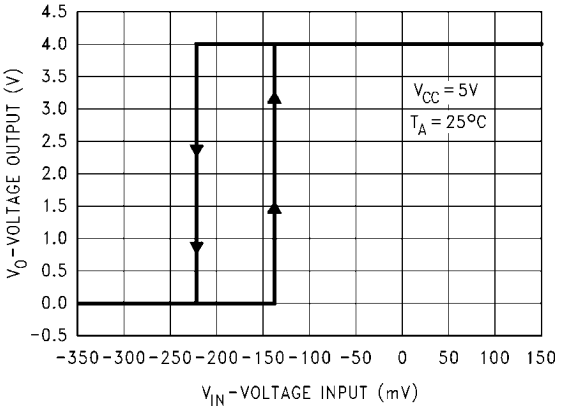
Voltage Output vs Voltage Input (Hysteresis)



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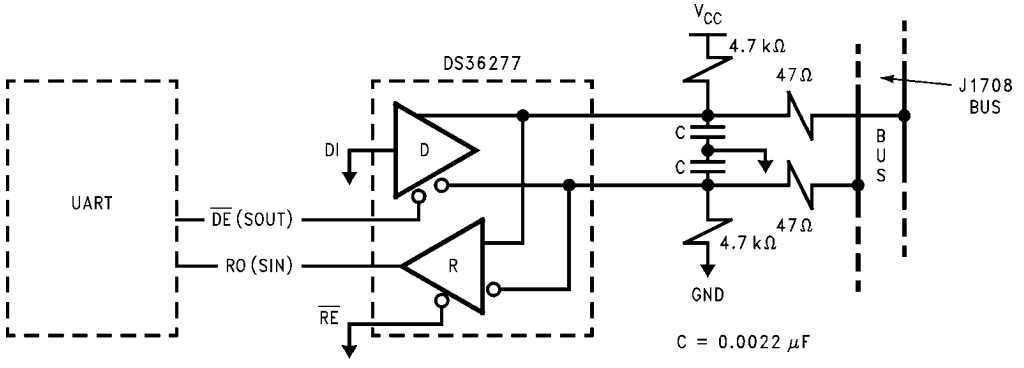
Typical Applications Information

SAE J1708 Node with External Bias Resistors and Filters



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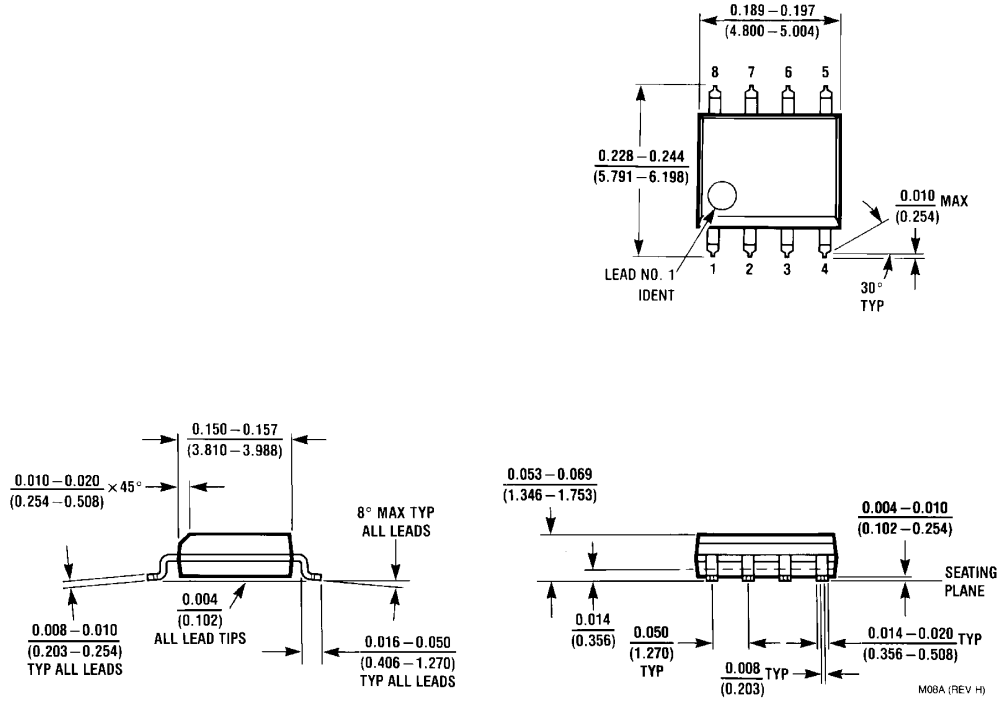
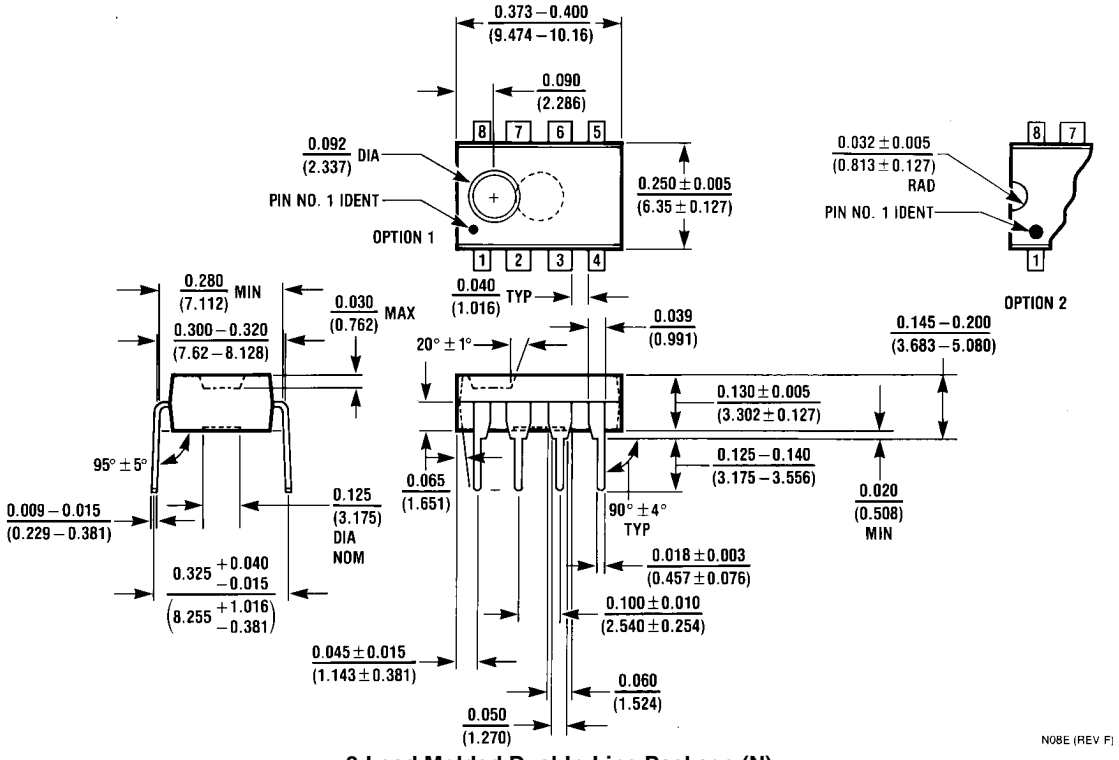
Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Molded Package (SO)
Order Number DS36277TM
NS Package Number M08A



8-Lead Molded Dual-In-Line Package (N)
Order Number DS36277TN
NS Package Number N08E

Notes

Notes

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