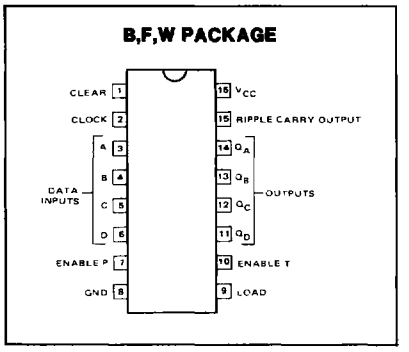
SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F

PIN CONFIGURATION



DESCRIPTION

This synchronous presettable decade counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function for the 54/74LS160 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

The 54/74LS160 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

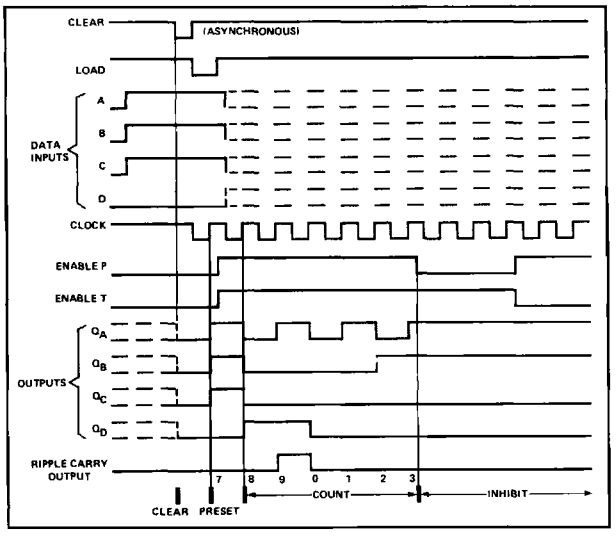
LOGIC

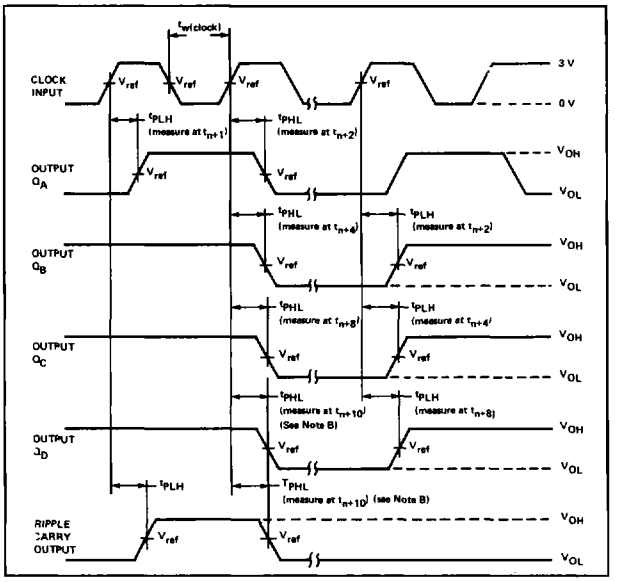
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit





VOLTAGE WAVEFORMS

NOTES:

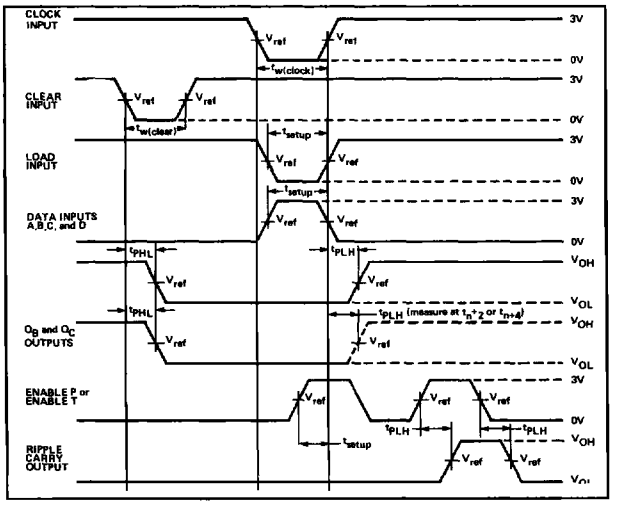
A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%. $Z_{out} \approx 50\Omega$ $t_r \leq 15$ns, $t_f \leq 6$ns.

B. Outputs Q_D and carry are tested at t_n+10, where t_n is the bit time when all outputs are low.

C. $V_{ref} = 1.3V$.

Load circuit is shown at front of section (totem pole outputs).

FIGURE 1—SWITCHING TIMES



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by generators having the following characteristics. PRR ≤ 1MHz, duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15$ns, $t_f \leq 6$ns.

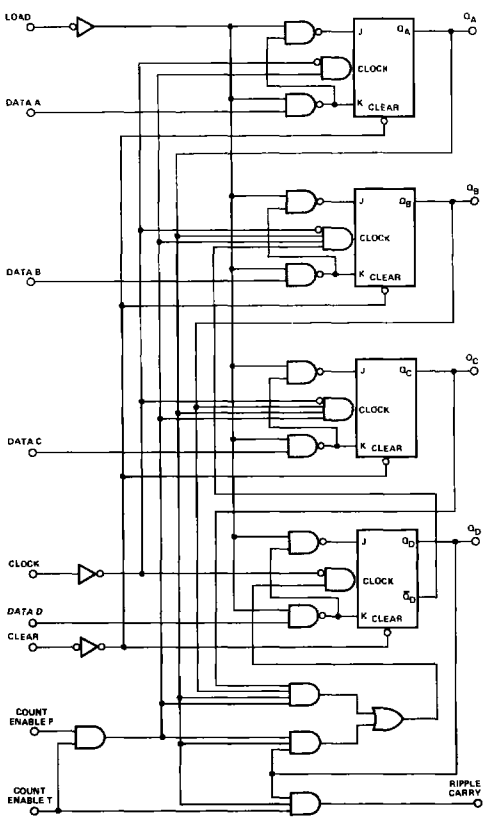
B. Enable P and enable T setup times are measured at $t_N + 0$

C. $V_{ref} = 1.3V$.

Load circuit is shown at front of book (totem pole outputs).

BLOCK DIAGRAMS

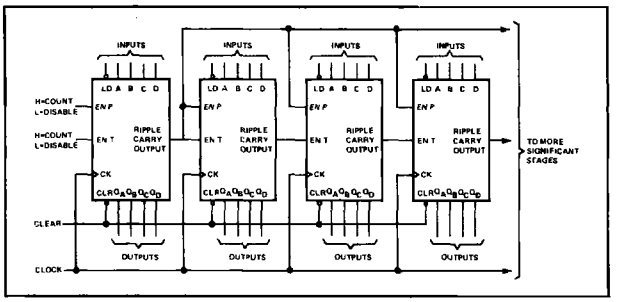
54/74



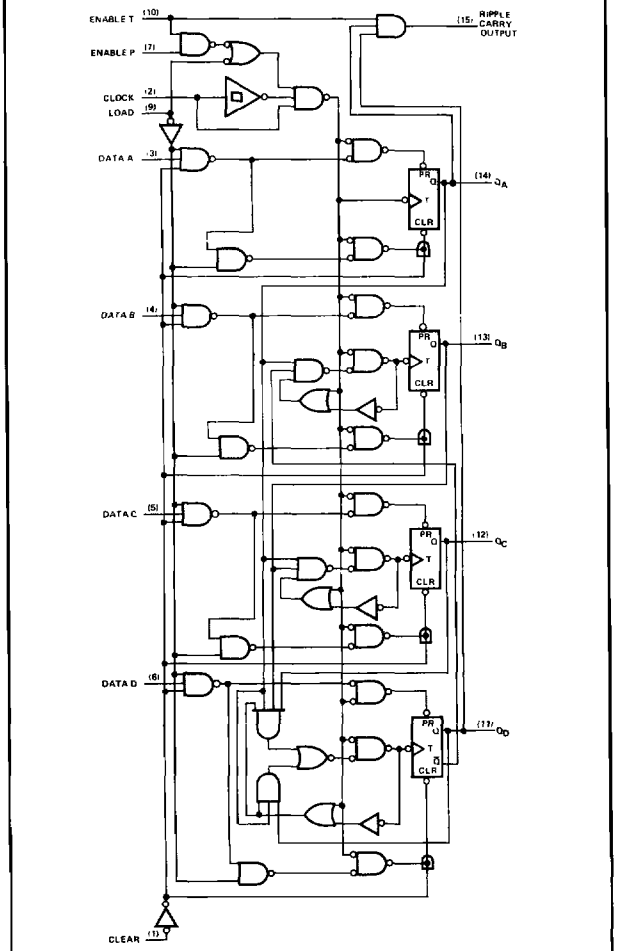
N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS160 will count in BCD. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.

TYPICAL APPLICATION DATA



54/74LS



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock}	Clock frequency			25	32		25	32		MHz
$t_{W(Clock)}$	Width of clock input pulse			25			25			ns
$t_{w(Clear)}$	Width of clear input pulse			20			20			ns
t_{Setup}	Input setup time	D_A-D_D		15						ns
		Enable P		20						
		Load		25						
		A,B,C,D	Q				0↑			
		Enable P, Enable T	Q				20↑			
		Load	Q				20↑			
t_{Hold}	Input hold time	Any		0						ns
		A,B,C,D					25↑			
		Others					10↑			
Propagation delay time										
t_{PLH}	Low-to-high	Clock	Carry		23	35		23	35	ns
t_{PHL}	High-to-low				23	35		23	35	
t_{PLH}	Low-to-high	Clock (load input high)	Q		13	20		16	24	
t_{PHL}	High-to-low				15	23		18	27	
t_{PLH}	Low-to-high	Clock (load input low)	Q		17	25		17	25	
t_{PHL}	High-to-low				19	29		19	29	
t_{PLH}	Low-to-high	Enable T	Carry		10	14		15	23	
t_{PHL}	High-to-low				10	14		15	23	
t_{PHL}	High-to-low	Clear	Q		20	30		26	38	

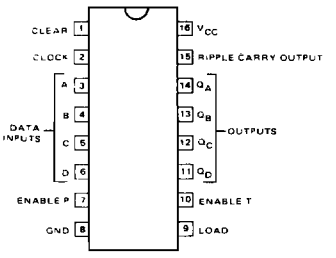
Load circuit and typical waveforms are shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54 F,W 74 B,F
54LS F,W 74LS B,F

PIN CONFIGURATION

B,F,W PACKAGE



DESCRIPTION

This synchronous presettable binary counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the

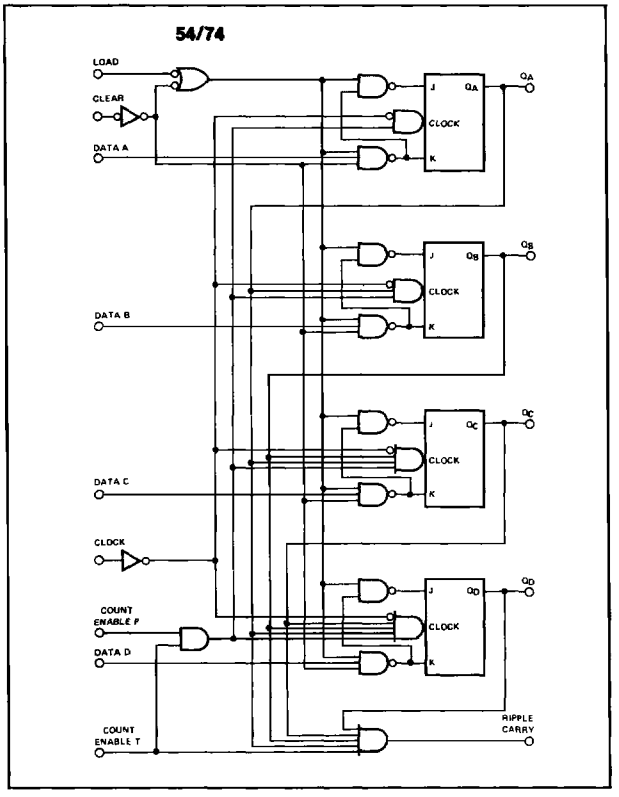
levels of the enable inputs. The clear function for the 54/74LS161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load or enable inputs.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

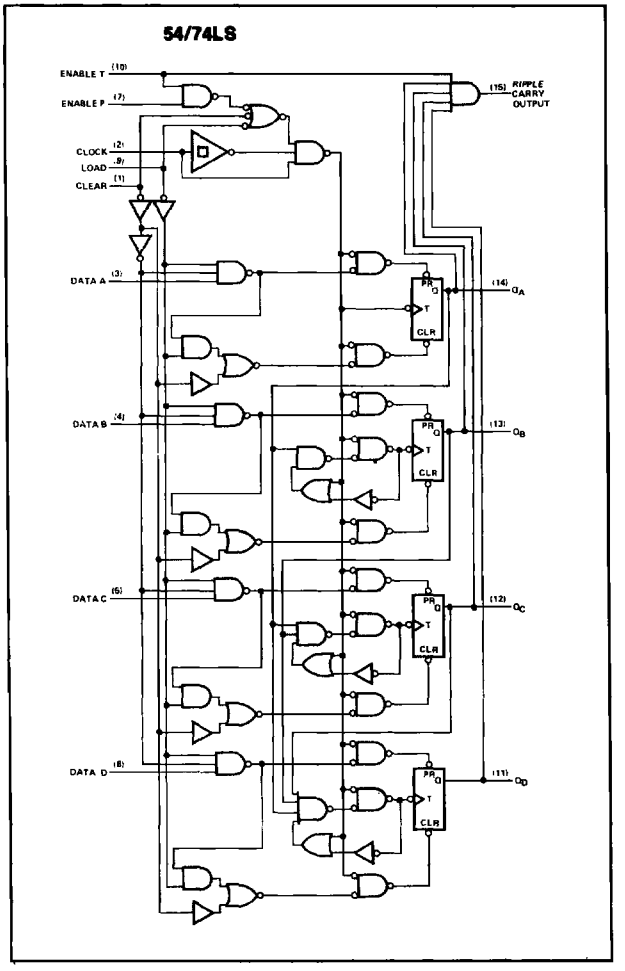
The 54/74LS161 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

BLOCK DIAGRAMS

54/74



54/74LS

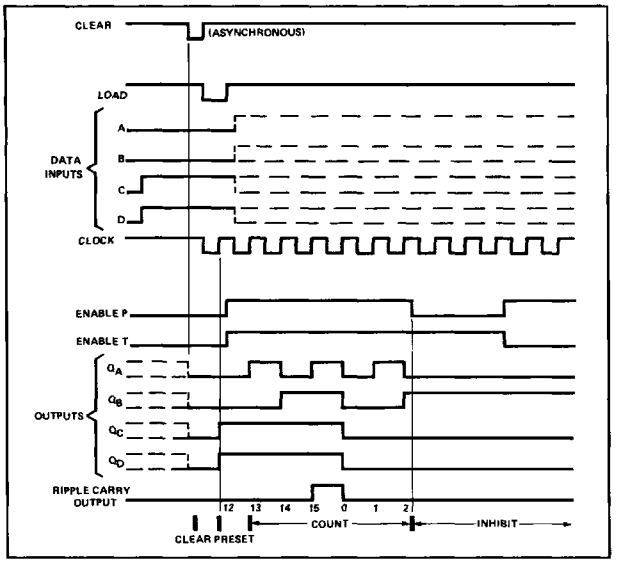


PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT, AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to binary twelve
3. Count to thirteen, fourteen, fifteen, zero, one, and two
4. Inhibit



NOTES

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, Duty Cycle ≤ 50%, $Z_{out} \approx 50\Omega$ $t_r \leq 15$ns, $t_f \leq 6$ns.
B. *Outputs Q_D and carry are tested at t_{n+16}, where t_n is the bit time when all outputs are low.*
C. $V_{ref} \approx 1.3V$.

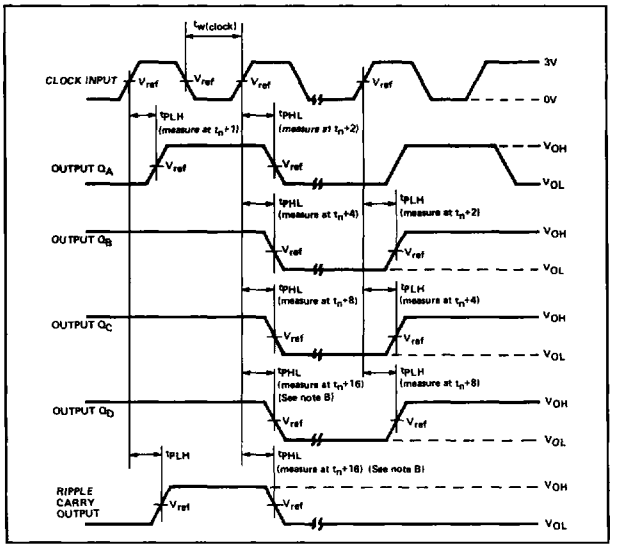


FIGURE 1—VOLTAGE WAVEFORMS

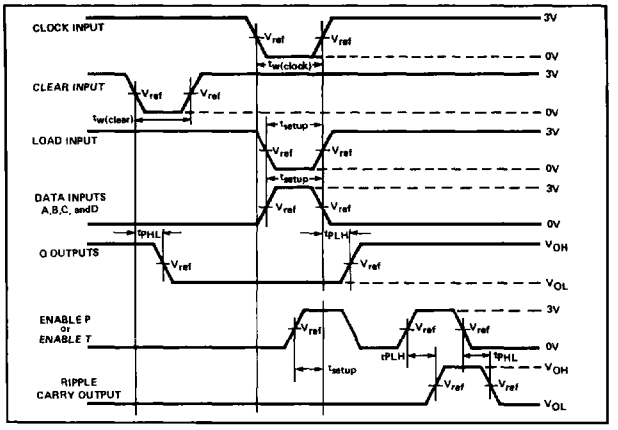


FIGURE 2—VOLTAGE WAVEFORMS

NOTES

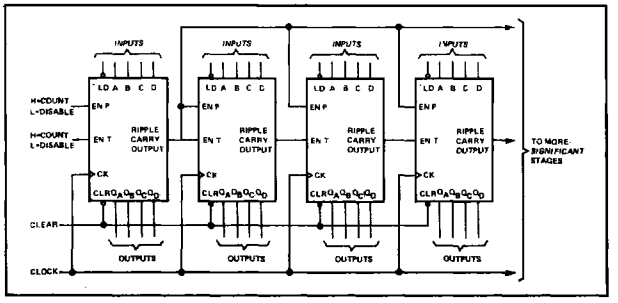
A. The input pulses are supplied by generators having the following characteristics: PRR≤1MHz, Duty cycle ≤ 50%, $Z_{out} \approx 50\Omega$, $t_r \leq 15$ns, $t_f \leq 6$ns.
B. Enable P and T setup times are measured at t_{n+0}.
C. $V_{ref} \approx 1.3V$.

Load circuit is shown at front of book (totem pole output).

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS161 will count in binary. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.



LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2kΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			25	32		25	32		MHz
t_w (Clock) Width of clock input pulse			25			25			ns
t_w (Clear) Width of clear input pulse			20			20			ns
t_{Setup} Input setup time	D_A-D_D		15						ns
	Enable P		26						
	Load		25						
	A,B,C,D	Q				0↑			
	Enable P, Enable T	Q				20↑			
	Load	Q				20↑			
t_{Hold} Input hold time	Any		0						ns
	A,B,C,D					25↑			
	Others					10↑			
Propagation delay time									
t_{PLH} Low-to-high	Clock	Carry		23	35		23	35	ns
t_{PHL} High-to-low				23	35		23	35	
t_{PLH} Low-to-high	Clock (load input high)	Q		13	20		16	24	
t_{PHL} High-to-low				15	23		18	27	
t_{PLH} Low-to-high	Clock (load input low)	Q		17	25		17	25	
t_{PHL} High-to-low				19	29		19	29	
t_{PLH} Low-to-high	Enable T	Carry		10	14		15	23	
t_{PHL} High-to-low				10	14		15	23	
t_{PHL} High-to-low	Clear	Q		20	30		26	38	

Load circuit and typical waveforms shown at the front of section.

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F

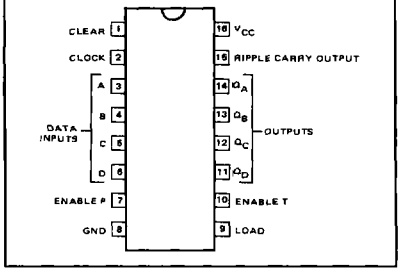
DESCRIPTION

This synchronous presettable decade counter features an internal carry look-ahead for applications in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveforms.

This counter is fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of

PIN CONFIGURATION

B,F,W PACKAGE



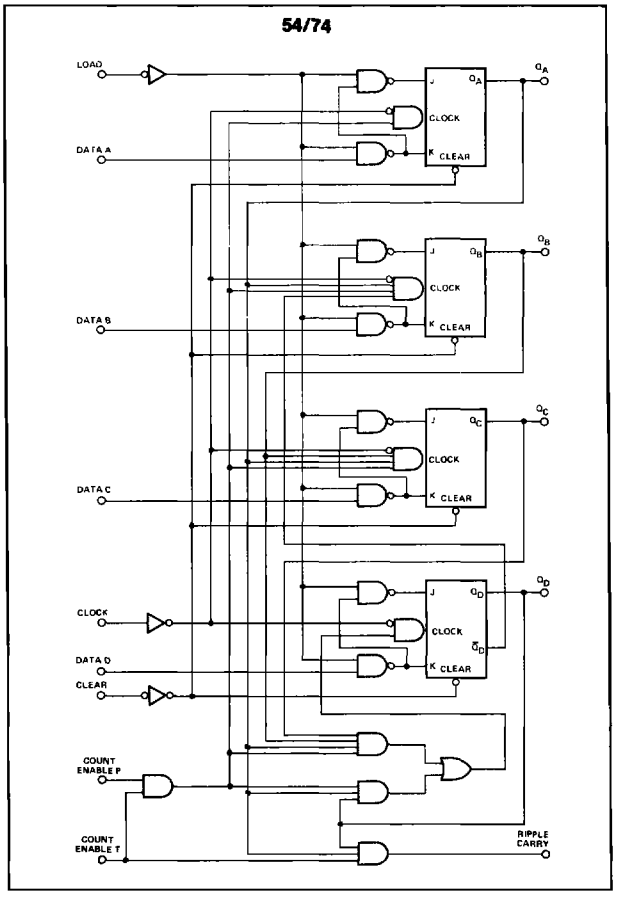
the levels of the enable inputs. The clear function for the 54/74LS162 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. Transitions at the enable P or T inputs are allowed regardless of the level of the clock input.

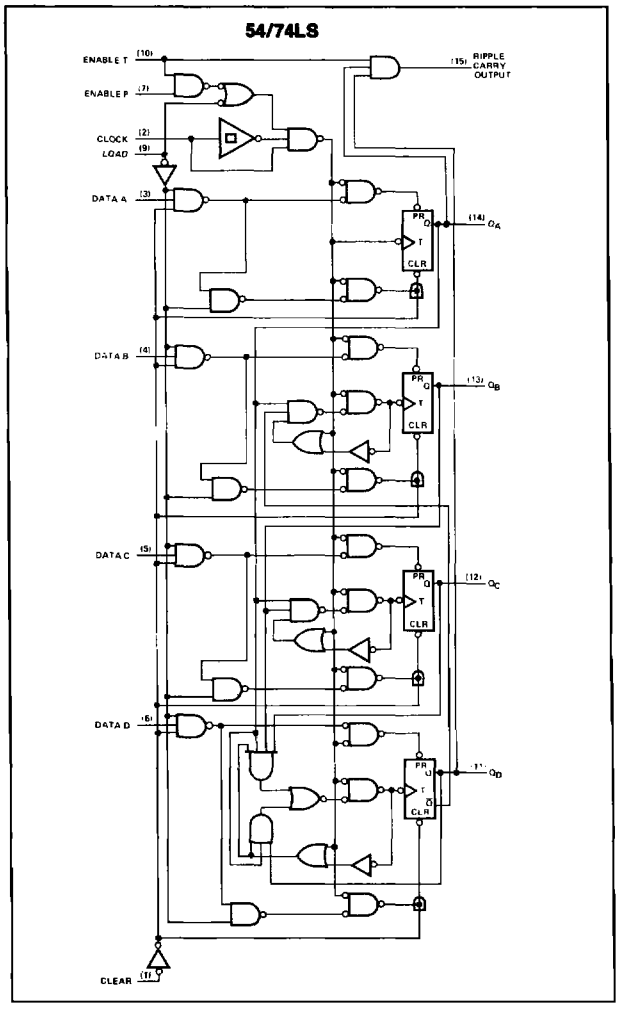
The 54/74LS162 features a fully independent clock circuit. Changes made to control inputs (enable P or T, load or clear) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading or counting) will be dictated solely by the conditions meeting the stable set up and hold times.

BLOCK DIAGRAMS

54/74



54/74LS



LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS			54/74 C_L=15pF R_L=400Ω			54/74LS C_L=15pF R_L=2KΩ			
PARAMETER	FROM INPUT	TO OUTPUT	MIN	TYP	MAX	MIN	TYP	MAX	UNIT
f_{Clock} Clock frequency			25	32		25	32		MHz
$t_{w(Clock)}$ Width of clock input pulse			25			25			ns
$t_{w(Clear)}$ Width of clear input pulse			20			20			ns
t_{Setup} Input setup time	$D_A - D_D$		15						ns
	Enable P		20						
	Load		25						
	Clear		20						
	A,B,C,D	Q				0↑			
	Enable P, Enable T	Q				20↑			
	Load	Q				20↑			
	Clear	Q				20↑			
t_{Hold} Input hold time	Any		0						ns
	A,B,C,D					25↑			
	Others					10↑			
Propagation delay time									
t_{PLH} Low-to-high	Clock	Carry		23	35		23	35	ns
t_{PHL} High-to-low				23	35		23	35	
t_{PLH} Low-to-high	Clock	Q		13	20		16	24	
t_{PHL} High-to-low	(load input high)			15	23		18	27	
t_{PLH} Low-to-high	Clock (load input low)	Q		17	25		17	25	
t_{PHL} High-to-low				19	29		19	29	
t_{PLH} Low-to-high	Enable T	Carry		10	14		15	23	
t_{PHL} High-to-low				10	14		15	23	
t_{PHL} High-to-low	Clear	Q		20	30		26	38	

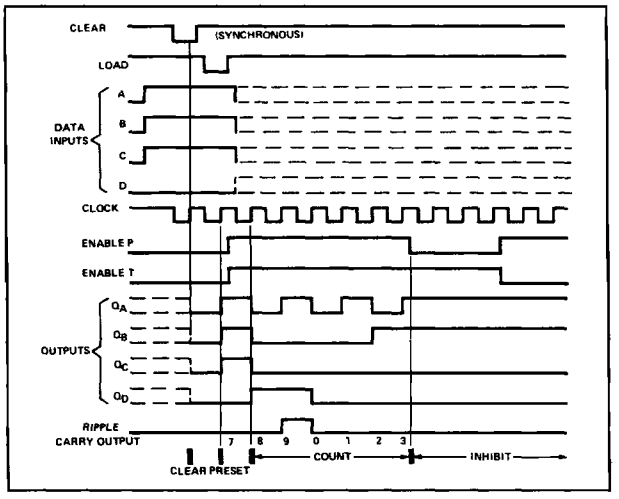
Load circuit typical and waveforms are shown at the front of section.

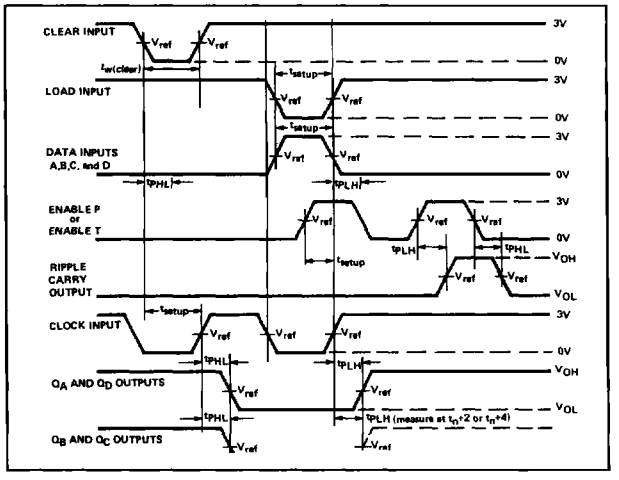
PARAMETER MEASUREMENT INFORMATION

TYPICAL CLEAR, PRESET, COUNT AND INHIBIT SEQUENCES

Illustrated below is the following sequence:

1. Clear outputs to zero
2. Preset to BCD seven
3. Count to eight, nine, zero, one, two, and three
4. Inhibit



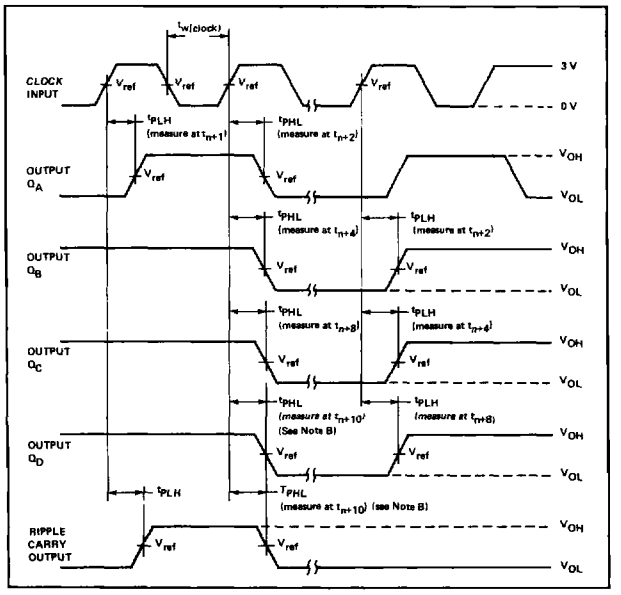


VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω; t_r < 15 ns, t_f ≤ 6 ns.
B. Enable P and enable T setup times are measured at t_{n+0}.
C. V_{ref} = 1.3 V.

FIGURE 2-SWITCHING TIMES



VOLTAGE WAVEFORMS

NOTES:

A. The input pulses are supplied by a generator having the following characteristics: PRR ≤ 1MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω; t_r ≤ 15 ns, t_f ≤ 6 ns; vary PRR to measure f_{max}.
B. Outputs Q_D and carry are tested at t_{n+10} where t_n is the bit time when all outputs are low.
C. V_{ref} = 1.5 V.

Load Circuit information is shown at the front of the book.

FIGURE 1-SWITCHING TIMES

LOGIC

TYPICAL APPLICATION DATA

N-BIT SYNCHRONOUS COUNTERS

This application demonstrates how the look-ahead carry circuit can be used to implement a high-speed n-bit counter. The 54/74LS162 will count in BCD. Virtually any count mode (modulo-N, N_1-toN_2, N_1-to-maximum) can be used with this fast look-ahead circuit.