Integrated Device Technology, Inc.

BiCMOS STATIC RAM 256K (32K x 8-BIT)

PRELIMINARY
IDT71B256

FEATURES:

- 32K x 8 BiCEMOS™ Static RAM
- High-speed address /chip select time
  - — Military: 20ns
  - — Commercial: 12/15/20ns
- One Chip Select plus one Output Enable pin
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Available in 28-pin sidebraze ceramic, 300 mil DIP; 300 mil plastic DIP and 28-pin, 300 mil plastic SOJ packages

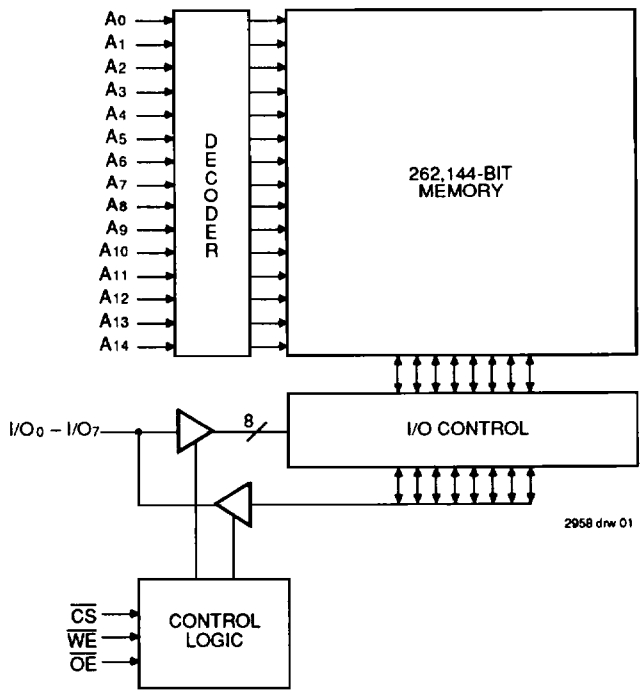
DESCRIPTION:

The IDT71B256 is a 262,144-bit high-speed static RAM organized as 32Kx8. It is fabricated using IDT's high-performance high-reliability BiCEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective solution for high-speed memory needs.

Address access times as fast as 12ns are available with power consumption of only 550mW (typ.). All inputs and outputs of the IDT71B256 are TTL-compatible and operation is from a single 5V supply. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation.

The IDT71B256 is packaged in a 28-pin, 300-mil side-braze; 28-pin, 300 mil plastic DIP and 28-pin, 300-mil SOJ packages.

FUNCTIONAL BLOCK DIAGRAM



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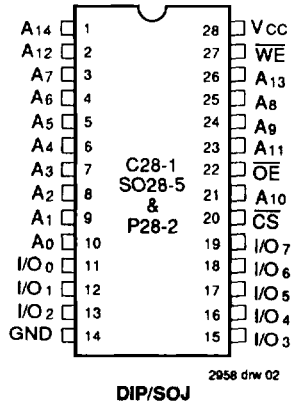
PIN CONFIGURATION



DIP/SOJ
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TA	Operating Temperature	0 to +70	-55 to +125	°C
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-55 to +125	-65 to +125	°C
PT	Power Dissipation	1.25	1.25	W
IOUT	DC Output Current	50	50	mA

NOTE: 2958 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE(1)

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O	Function
L	L	H	DOUT	Read
L	X	L	DIN	Write
L	H	H	Hi-Z	Output Disabled
H	X	X	Hi-Z	Deselect Chip

NOTE: 2958 tbl 01

1. H = VIH, L = VIL, x = Don't care.

CAPACITANCE (TA = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Max.	Unit
CIN	Input Capacitance	8	pF
COUT	Output Capacitance	12	pF

NOTE: 2958 tbl 03

1. This parameter is guaranteed by device characterization, but not production tested.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	-0.5	—	0.8	V

NOTE: 2958 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

DC ELECTRICAL CHARACTERISTICS

VCC = 5.0V ± 10%

Symbol	Parameter	Test Condition	IDT71B256			Unit
			Min.	Typ.(1)	Max.	
|ILI|	Input Leakage Current	VCC = Max., VIN = GND to VCC	—	—	10	µA
|ILO|	Output Leakage Current	VCC = Max., $\overline{CS}$ = VIH, VOUT = GND to VCC	—	—	10	µA
VOL	Output Low Voltage	IOL = 10mA, VCC = Min.	—	—	0.5	V
		IOL = 8mA, VCC = Min.	—	—	0.4	
VOH	Output High Voltage	IOH = -4mA, VCC = Min.	2.4	—	—	V

NOTE: 2958 tbl 05

1. Typical limits are at VCC = 5.0V, +25°C ambient.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 10%)

Symbol	Parameter	71B256S12		71B256S15		71B256S20		Unit
		Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX}[2]	200	—	190	—	180	190	mA

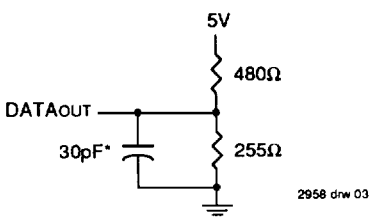
2958 tbl 05

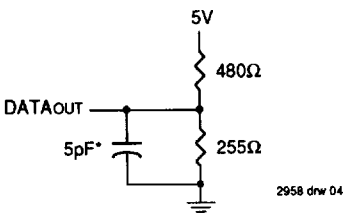
NOTES:
1. All values are maximum guaranteed values.
2. f_{MAX} = 1/t_{RC}.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 1

2958 tbl 06





*Including scope and jig (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

Figure 1. AC Test Loads

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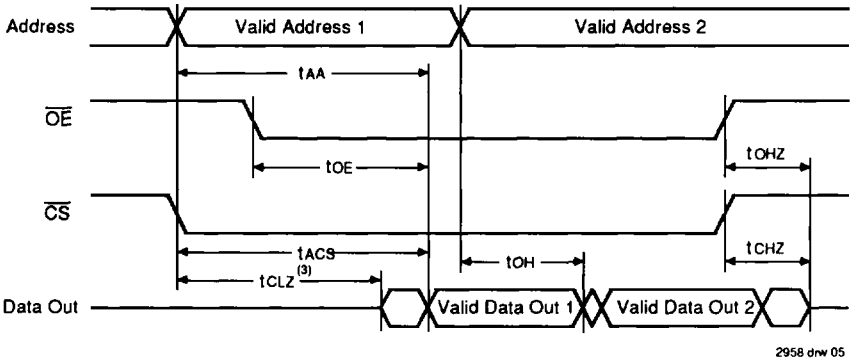
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71B256-12[1] Min.	71B256-12[1] Max.	71B256-15[1] Min.	71B256-15[1] Max.	71B256-20 Min.	71B256-20 Max.	Unit
Read Cycle								
tRC	Read Cycle Time	12	—	15	—	20	—	ns
tAA	Address Access Time	—	12	—	15	—	20	ns
tACS	$\overline{CS}$ Access Time	—	8	—	9	—	12	ns
tCLZ[2]	$\overline{CS}$ to Output in Low Z	3	—	4	—	5	—	ns
tCHZ[2]	$\overline{CS}$ to Output in High Z	—	4	—	5	—	6	ns
tOE	$\overline{OE}$ to Output Valid	—	8	—	9	—	10	ns
tOLZ[2]	$\overline{OE}$ to Output Low Z	3	—	4	—	5	—	ns
tOHZ[2]	$\overline{OE}$ to Output High Z	—	4	—	5	—	6	ns
tOH	Out Hold from Add Change	3	—	3	—	3	—	ns
Write Cycle								
tWC	Write Cycle Time	12	—	15	—	20	—	ns
tAW	Address to End of Write	9	—	10	—	12	—	ns
tAS	Address Setup Time	0	—	0	—	0	—	ns
tWP	Write Pulse Width	9	—	10	—	12	—	ns
tCW	$\overline{CS}$ to End of Write	8	—	9	—	10	—	ns
tWR	Write Recovery	0	—	0	—	0	—	ns
tWHZ[2]	$\overline{WE}$ to Out in High Z	—	5	—	6	—	7	ns
tDW	Data Setup	5	—	6	—	8	—	ns
tDH	Data Hold	2	—	2	—	2	—	ns
tOW[2]	Output from End of Write	3	—	4	—	4	—	ns

NOTE:
1. 0° to +70°C temperature range only.
2. This parameter is guaranteed, but not tested.

2958 tbl 08

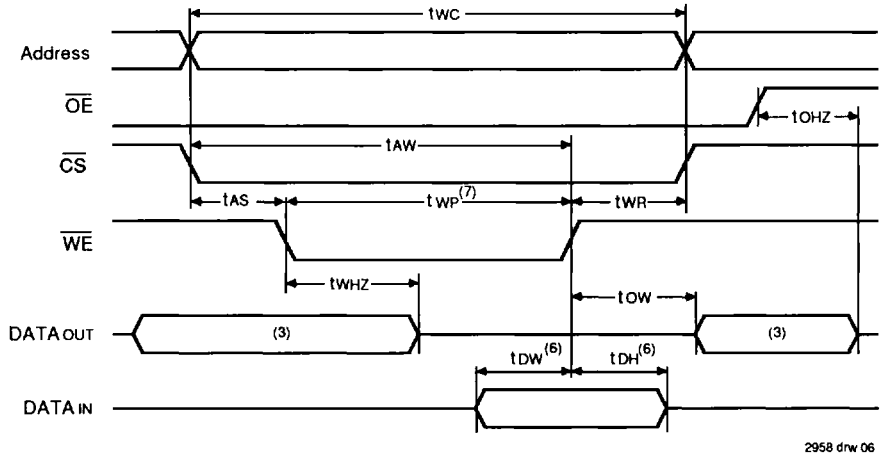
TIMING WAVEFORM OF READ CYCLE[1,2]



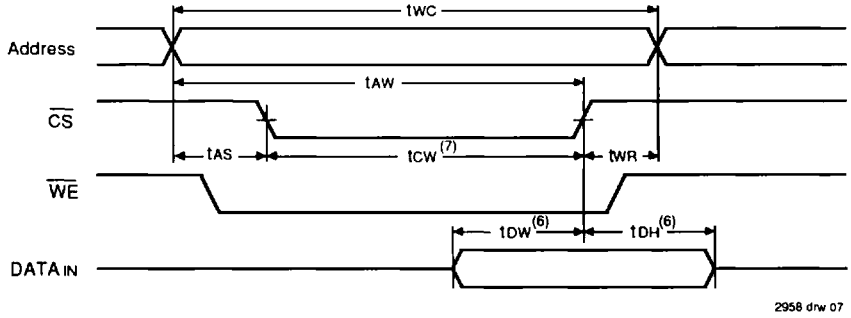
2958 drw 05

NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Address valid prior to or coincident with $\overline{CS}$ transition low.
3. Transition is measured ±200mV from steady state.

TIMING WAVEFORM OF WRITE CYCLE NO.1 ($\overline{WE}$ CYCLE)(1,2,4,5,6)



TIMING WAVEFORM OF WRITE CYCLE NO.2 ($\overline{CS}$ CYCLE)(1,2,4,5)



NOTES:
1. A write occurs during the overlap (tWC and tWP) of $\overline{CS}$ low and $\overline{WE}$ low.
2. tWF is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ being deasserted.
3. During this period, the I/O pins are in the output state, and input signals must not be applied on these pins.
4. If $\overline{CS}$ is asserted coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.
5. If $\overline{CS}$ is deasserted coincident with or before $\overline{WE}$ goes high, the output will remain in a high impedance state.
6. The transition is measured ±200mV from steady state with a 5pF load.
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ+tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION