MC145453

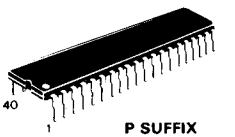
LCD Driver with Serial Interface
LSI CMOS

3

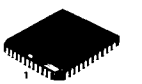
The MC145453 Liquid-Crystal Display Driver consists of a 36-stage serial-in/parallel-out shift register with 33 latches and drivers. Each package drives up to 33 non-multiplexed LCD segments; e.g., a 4½-digit, 7-segment-plus-decimal display. This device may be paralleled to increase the number of segments driven.

The input format is a Start Bit (high), followed by 33 Display Bits, plus 2 Trailing Bits (don't cares). A high Start Bit, after propagating to the last shift register stage, triggers generation of an internal load signal which transfers the 33 Display Bits into latches. An internal reset clears only the shift register which readies the device for the next bit stream.

- On-Chip Oscillator Provides 50 Percent Duty Cycle Backplane Drive
- No External Load Signal Required
- Operating Voltage Range: 3 to 10 V
- Operating Temperature Range: −40° to 85°C
- TTL-Compatible Inputs May Be Driven With CMOS
- May Be Used With Segmented-Alphanumeric, Bar-Graph, or Dot-Matrix LCDs
- Advantages Over Multiplexed LCD Systems: Wider Viewing Angle
  Optimum Contrast at Low Voltage
  Better Legibility at Extreme Temperature
- For Additional Applications Information, see AR266



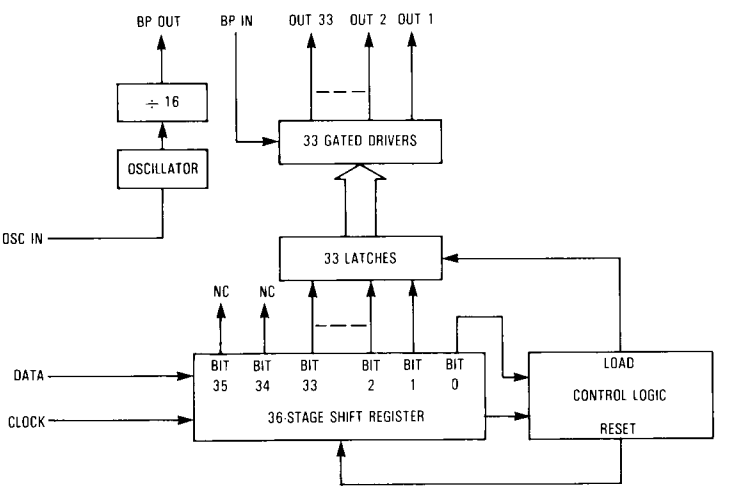
P SUFFIX
PLASTIC DIP
CASE 711



FN SUFFIX
PLCC
CASE 777

ORDERING INFORMATION
MC145453P Plastic DIP
MC145453FN PLCC

BLOCK DIAGRAM



MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +11.0	V
V_{in}	DC Input Voltage	−0.5 to V_{DD} +0.5	V
V_{out}	DC Output Voltage	−0.5 to V_{DD} +0.5	V
I_{in}	DC Input Current, per Pin	±20	mA
I_{out}	DC Output Current, per Pin	±25	mA
I_{CC}	DC Supply Current, V_{DD} and V_{SS} Pins	±50	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	Storage Temperature	−65 to +150	°C
T_L	Lead Temperature (10-Second Soldering)	260	°C

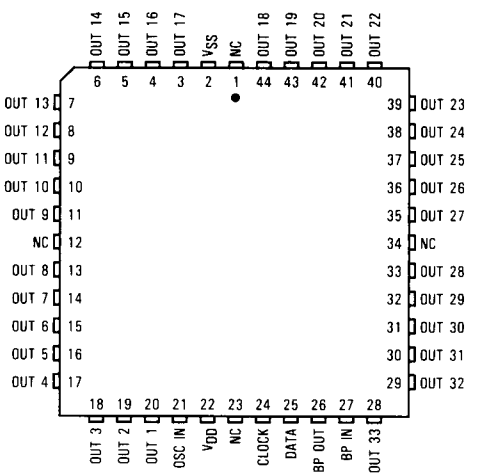
*Maximum Ratings are those values beyond which damage to the device may occur.
†Power Dissipation Temperature Derating: −12 mW/°C from 65°C to 85°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

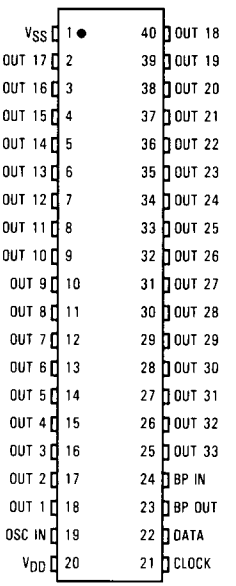
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD} except Osc In which must be tied to V_{SS}). Unused outputs must be left open.

3

PIN ASSIGNMENTS



NC = NO CONNECTION

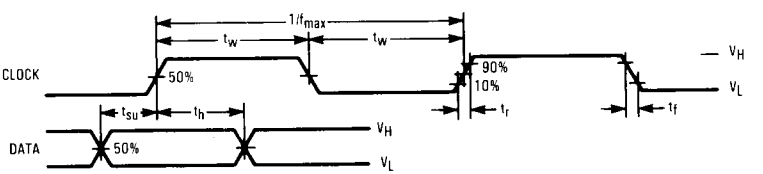


ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le 85°C$, Voltages Referenced to V_{SS})

Symbol	Parameter	Test Condition	V_{DD} V	Guaranteed Limit	Unit
V_{DD}	Power Supply Voltage Range		–	3.0 to 10.0	V
V_{IL}	Maximum Low-Level Input Voltage (Data, Clock, BP In)		3.0 4.5 10.0	0.4 0.8 0.8	V
V_{IH}	Minimum High-Level Input Voltage (Data, Clock, BP In)		3.0 5.5 10.0	2.0 2.0 8.0	V
I_{OL}	Minimum Low-Level Output Current (BP Out) (Out 1 to Out 33)	$V_{out} = 0.3$ V	 3.0 3.0	 320 20	μA
I_{OH}	Minimum High-Level Output Current (BP Out) (Out 1 to Out 33)	$V_{out} = 2.7$ V	 3.0 3.0	 −320 −20	μA
V_{OO}	Average DC Output Offset Voltage (BP Out Relative to Out 1 through Out 33)	BP Out: $C_L = 8750$ pF Out 1 to 33: $C_L = 250$ pF	3.0 10.0	±50 ±50	mV
I_{in}	Maximum Input Leakage Current (Data, Clock, BP In)	$V_{in} = V_{DD}$ or V_{SS}	10.0	±1.0	μA
I_{DD}	Maximum Quiescent Supply Current (per Package)	Osc In: $V_{in} = V_{SS}$ BP In, Data, Clock: $V_{in} = V_{DD}$ or V_{SS} $I_{out} = 0$ μA	10.0	10	μA
I_{dd}	Maximum RMS Operating Supply Current (per Package)	$R_X = 1.0$ MΩ, $C_X = 470$ pF BP Out Tied to BP In Clock, Data: $V_{in} = V_{DD}$ or V_{SS} $I_{out} = 0$ μA	10.0	40	μA

AC ELECTRICAL CHARACTERISTICS ($-40°C \le T_A \le 85°C$, Input $t_r = t_f = 50$ ns)

Symbol	Parameter	V_{DD} V	Guaranteed Limit	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figure 1)	3.0 4.5 10.0	400 850 1800	kHz
t_{su}	Minimum Setup Time, Data to Clock (Figure 1)	3.0 4.5 10.0	300 180 100	ns
t_h	Minimum Hold Time, Clock to Data (Figure 1)	3.0 4.5 10.0	300 130 50	ns
t_w	Minimum Pulse Width, Clock (Figure 1)	3.0 4.5 10.0	1250 585 275	ns
t_r, t_f	Maximum Input Rise and Fall Times, Clock (Figure 1)	3.0 4.5 10.0	300 300 300	ns
C_{in}	Maximum Input Capacitance	–	10	pF



$V_H = 3.0$ V, $V_L = 0$ V @ $V_{DD} = 3.0$ V, 4.5 V
$V_H = 10.0$ V, $V_L = 0$ V @ $V_{DD} = 10.0$ V

Figure 1. Switching Waveforms

PIN DESCRIPTIONS

INPUTS

Data

Serial data input. Data on this pin is serially entered into the on-chip shift register on the rising edge of Clock. The data stream consists of a Start Bit (high), followed by 33 Display Bits, plus 2 Trailing Bits (don't cares). This device does not contain a decoder, which allows the flexibility of formatting the segment information externally. Display Bit 1 controls the LCD segment connected to Out 1, Bit 2 controls Out 2, etc. If a Display Bit is high, the associated segment is activated. The Display Bits are stored in latches which eliminates display flicker during shifting.

Clock

Each rising edge on Clock causes Data to be shifted into the 36-bit shift register. The shift register is completely static, allowing clock rates down to DC in a continuous or intermittent mode. Clock need not be synchronous to Osc In nor BP In. The internal load shown in Figure 2 transfers the 33 Display Bits to the on-chip latches. The internal reset clears the shift register (only) to ready the device for the next set of data.

Upon power up, the MC145453 must be initialized to ensure synchronization with the MCU. This initialization consists of flushing the shift register by shifting in at least 36 lows (zeroes).

BP In

Backplane in. The signal applied to this input must also be tied to the backplane of the LCD. BP In is the common input to the 33 gated drivers, and may be sourced from the on-chip oscillator output, BP Out. (See Figure 3.) To reduce interference from the display driver in analog designs, BP In may be synchronized with a system clock. The BP In waveform must be a 50% duty cycle to minimize offset voltage to the LCD which impacts display lifetime. (See Figures 4 and 5.) The BP In frequency should be 25 to 250 Hz, depending on the display.

Osc In

Oscillator input. As shown in Figure 3, this pin is used in conjunction with an external resistor and capacitor to form an oscillator. The oscillator frequency is divided by 16 and appears at BP Out. With a 5 V supply, nominal values of 1 MΩ and 470 pF produce a 60 to 150 Hz waveform at BP Out. If the on-chip oscillator is not used, Osc In must be tied to V_{SS} which minimizes power consumption and insures reliable chip operation.

OUTPUTS

BP Out

Backplane output. This pin may be used to provide a 50% duty cycle waveform to directly drive the backplane of the LCD and BP In. (See Figure 3.) If the on-chip oscillator is not used, BP Out must be left unconnected. (See Figure 4.) When paralleling devices, BP Out fans out to drive the BP In pins of other packages. (See Figure 6.)

Out 1 through Out 33

Frontplane driver outputs which are tied directly to the LCD.

POWER

V_{SS}

Most negative supply potential. This pin is usually ground.

V_{DD}

Most positive supply potential. This voltage may range from +3 to +10 volts with respect to V_{SS}.

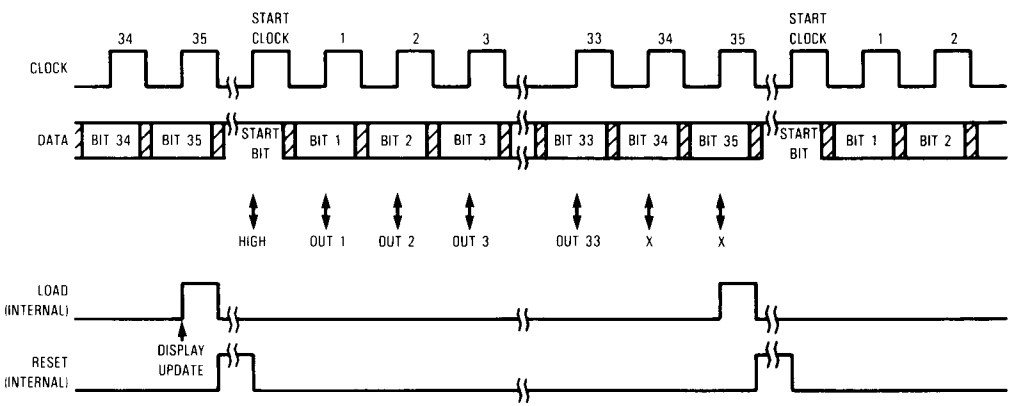


Figure 2. Timing Diagram

APPLICATIONS INFORMATION

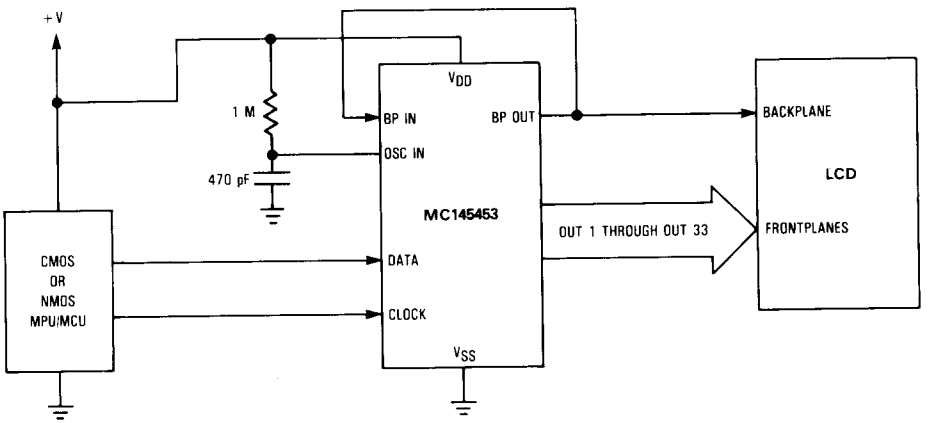


Figure 3. Using On-Chip Oscillator

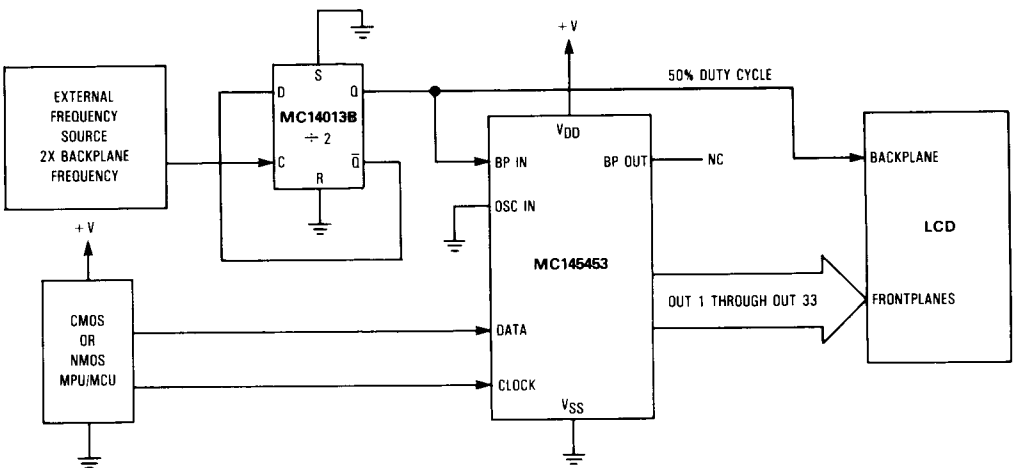


Figure 4. Converting External Backplane Frequency Source to 50% Duty Cycle

APPLICATIONS INFORMATION (CONT'D)

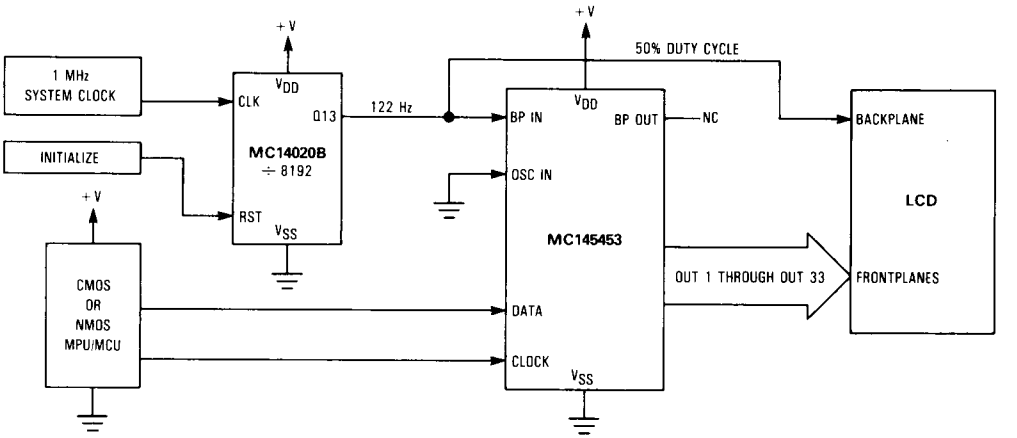


Figure 5. Using Low-Cost Divider to Sync Backplane Frequency

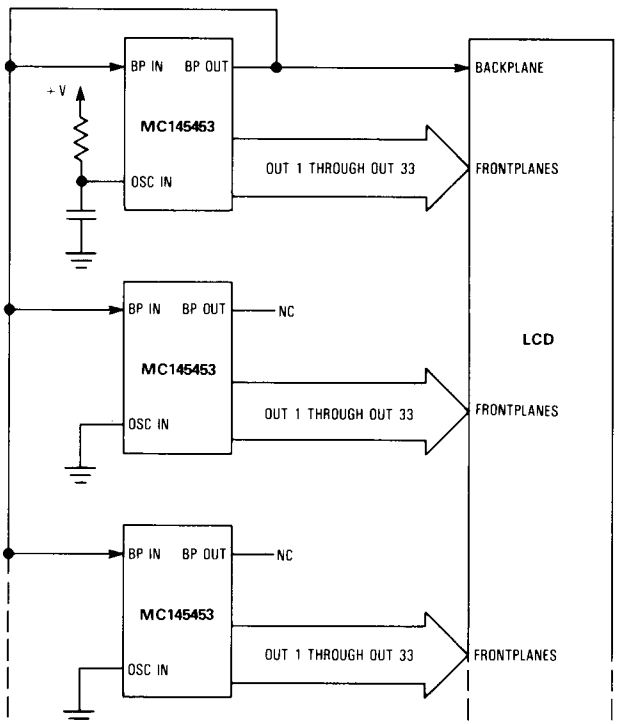


Figure 6. Paralleling Devices to Increase Number of Driven Segments