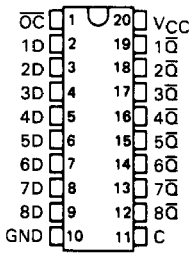
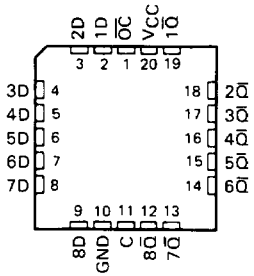
- 8 Latches in a Single Package
- 3-State Bus-Driving Inverting Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

SN54F563 . . . J PACKAGE
SN74F563 . . . DW OR N PACKAGE
(TOP VIEW)



SN54F563 . . . FK PACKAGE
(TOP VIEW)



description

These 8-bit latches feature three-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight latches are transparent D-type latches. When the enable (C) is high, the $\overline{Q}$ outputs will follow the complements of data (D) inputs. When the enable is taken low, the output will be latched at the inverses of the levels that were set up at the D inputs.

A buffered output-control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased high-logic level provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ($\overline{OC}$) does not affect the internal operation of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

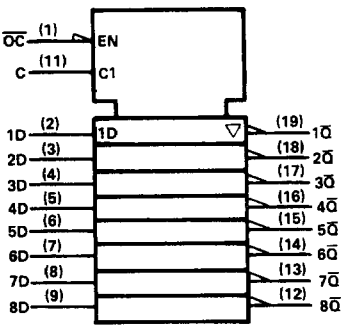
The SN54F563 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74F563 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(EACH LATCH)

INPUTS			OUTPUT
ENABLE			
$\overline{OC}$	C	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

2 Data Sheets

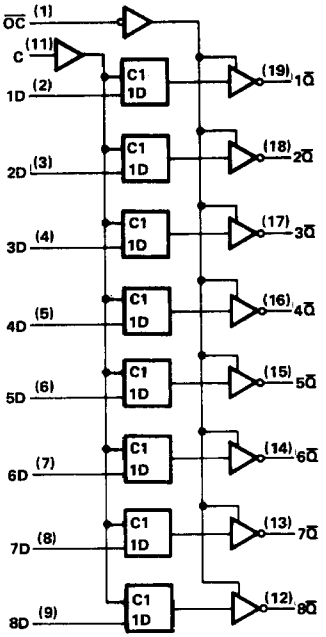
logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12

Pin numbers shown are for DW, J, and N packages.

logic diagram (positive logic)



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abolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} . . . . . −0.5 V to 7 V
Input voltage† . . . . . −1.2 V to 7 V
Input current . . . . . −30 mA to 5 mA
Voltage applied to any output in the disabled or power-off state . . . . . −0.5 V to 5.5 V
Voltage applied to any output in the high state . . . . . −0.5 V to V_{CC}
Current into any output in the low state: SN54F563 . . . . . 40 mA
SN74F563 . . . . . 48 mA
Operating free-air temperature range: SN54F563 . . . . . −55°C to 125°C
SN74F563 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

†The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F563			SN74F563			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			−18			−18	mA
I_{OH}	High-level output current			−3			−3	mA
I_{OL}	Low-level output current			20			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperatuare range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54F563			SN74F563			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = −1 mA	2.5	3.4		2.5	3.4		V
		I_{OH} = −3 mA	2.4	3.3		2.4	3.3		
	V_{CC} = 4.75 V,	I_{OH} = −1 to −3 mA				2.7			
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 20 mA		0.30	0.5				V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	μA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.5 V			−50			−50	μA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.5 V			−0.6			−0.6	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0	−60		−150	−60		−150	mA
I_{CCZ}	V_{CC} = 5.5 V,	See Note 1		38	61		38	61	mA

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second.
NOTE 1: I_{CCZ} is measured with $\overline{OC}$ at 4.5 V and all other inputs grounded.

timing requirements

		V_{CC} = 5 V, T_A = 25°C	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX†				UNIT
		'F563	SN54F563		SN74F563		
		MIN MAX	MIN	MAX	MIN	MAX	
t_{su}	Setup time, data before enable C↓	2	2		2		ns
t_h	Hold time, data before enable C↓	3	3		3		ns
t_w	Pulse duration, enable C high	6	6		6		ns

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX†				UNIT
			'F563			SN54F563		SN74F563		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3.2	6.5	9	3.2	12	3.2	10	ns
t_{PHL}			2.2	4.8	7	2.2	9	2.2	8	
t_{PLH}	C	Q	4.2	8.1	11	4.2	14	4.2	13	ns
t_{PHL}			2.2	5.2	7	2.2	9	2.2	8	
t_{PZH}	$\overline{OC}$	Q	1.2	7.3	10	1.2	12.5	1.2	11	ns
t_{PZL}			1.2	4.7	6.5	1.2	9	1.2	7.5	
t_{PHZ}	$\overline{OC}$	Q	1.2	4.3	6	1.2	8.5	1.2	7	ns
t_{PLZ}			1.2	3.7	5.5	1.2	7.5	1.2	6.5	

†For conditions shown as MIN or MAX, use the appropriate value specified under Recommended Operating Conditions.
NOTE 2: Load circuits and waveforms are shown in Section 1.

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