DESCRIPTION

The 8250, 8251 and 8252 are gate arrays for decoding and logic conversion applications. The 8250 converts 3 lines of input to a one-of-eight output. The fourth input line (D) is utilized as an inhibit to allow use in larger decoding networks.

The 8251 and 8252 convert a 4 line input code (with 1-2-4-8 weighting) to a one-of-ten output as shown in the Truth Table.

The 8252 is a direct replacement for the 9301 with all outputs being forced high when a binary code greater than nine is applied to the inputs.

The selected output is LOW.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V_{CC}=5V±5%; T_A=0°C to +75°C	MILITARY RANGES V_{CC}=5V±5%; T_A=−55°C to +125°C
Plastic DIP	Fig. A Fig. C	N8250N • N82S50N N8251N • N8252N • N82S52N	
Ceramic DIP	Fig. A Fig. C	N8250F • N82S50F N8251F • N8252F • N82S52F	S8250F S8251F • S8252F
Flatpak	Fig. B Fig. C		S8250W S8251W • S8252W

TRUTH TABLE

INPUT STATE				OUTPUT STATES											
				8250/82S50								8251/8252/82S52			
A	B	C	D	0	1	2	3	4	5	6	7	8	9	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	L
L	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H

PIN CONFIGURATIONS

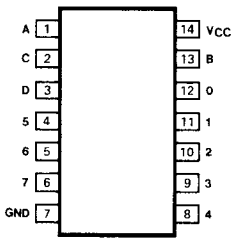


Figure A

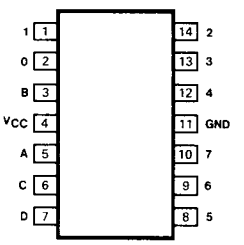


Figure B

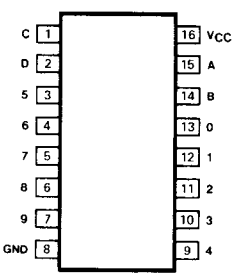
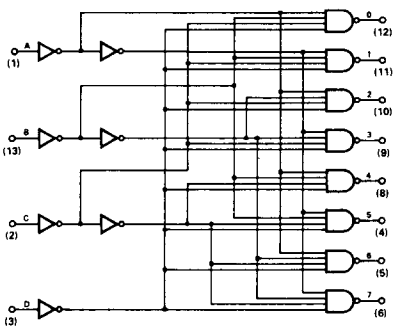


Figure C

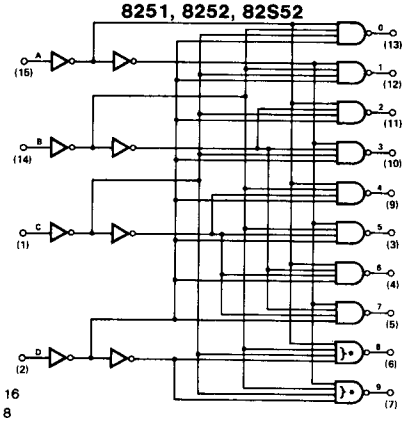
LOGIC DIAGRAMS

8250, 82S50



V_{CC} = Pin 14
GND = Pin 7
( ) = Denotes pin numbers for dip packages only.

8251, 8252, 82S52



V_{CC} = Pin 16
GND = Pin 8
( ) = Denotes pin numbers
*Connections made on 8252 only

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

	PARAMETER	TEST CONDITIONS	8250/51/52		UNIT
			Min	Max	
I_{OH}	Output HIGH voltage	V_{CC} = 4.75V, V_{OUT} = 5.25V	2.6		V
V_{OL}	Output LOW voltage	V_{CC} = 4.75V, I_{OL} = 16mA		0.4	V
I_{IH}	Input HIGH current	V_{CC} = 5.25V, V_{IN} = 4.5V		40	μA
I_{IL}	Input LOW current A,B,C, (8250/51) A,B,C,D (8252) D (8251 only) D (8250 only)	V_{CC} = 5.25V, V_{IN} = 0.4V		 −1.2 −1.6 −1.2 −1.0	 mA mA mA mA
V_{BD}	Voltage Breakdown	V_{CC} = 5.0V, I_{IN} = 10mA	5.5		V
I_{CC}	Supply Current (8250 only) (8251 and 8252)	V_{CC} = 5.0V, V_{OUT} = OV		 23.8 25.7	 mA mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

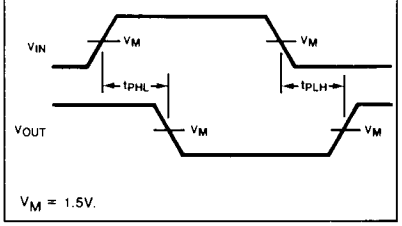
	PARAMETER	TEST CONDITIONS	82S50/S52		UNIT
			Min	Max	
I_{OH}	Output HIGH voltage	V_{CC} = 4.75V, V_{OUT} = 5.25V	2.7		V
V_{OL}	Output LOW voltage	V_{CC} = 4.75V, I_{OL} = 20mA		0.5	V
I_{IH}	Input HIGH current	V_{CC} = 5.25V, V_{IN} = 4.5V		10	μA
I_{IL}	Input LOW current	V_{CC} = 5.25V, V_{IN} = 0.5V		−400	μA
V_{CD}	Input clamp voltage	V_{CC} = 5.0V, I_{IN} = −18mA		−1.2	V
I_{CC}	Supply Current (82S50 only) (82S52 only)	V_{CC} = 5.0V		 72 85	 mA mA

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	8250/51/52 C_L = 30pF R_1 = ∞Ω R_2 = 84.5Ω		82S50/S52 C_L = 15pF R_L = 280Ω		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Input to output	Waveform 1		35 35		16 16	ns ns

AC WAVEFORM

WAVEFORM FOR INVERTING OUPUTS



V_M = 1.5V.

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