

74175, LS175, S175 Flip-Flops

Quad D Flip-Flop Product Specification

Logic Products

FEATURES

- Four edge-triggered D flip-flops
- Three speed-power ranges available
- Buffered common clock
- Buffered, asynchronous Master Reset

DESCRIPTION

The '175 is a quad, edge-triggered D-type flip-flop with individual D inputs and both Q and \bar{Q} outputs. The common buffered Clock (CP) and Master Reset (\overline{MR}) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge triggered. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output.

All Q outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the \overline{MR} input. The device is useful for applications where both true and complement outputs are required, and the Clock and Master Reset are common to all storage elements.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74175	35MHz	30mA
74LS175	40MHz	11mA
74S175	110MHz	60mA

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N74175N, N74LS175N, N74S175N
Plastic SO-16	N74LS175D, N74S175D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

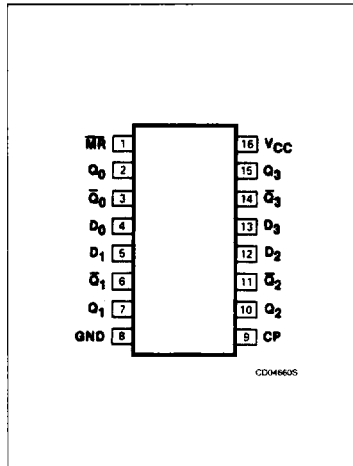
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
All	Inputs	1ul	1Sul	1LSul
All	Outputs	10ul	10Sul	10LSul

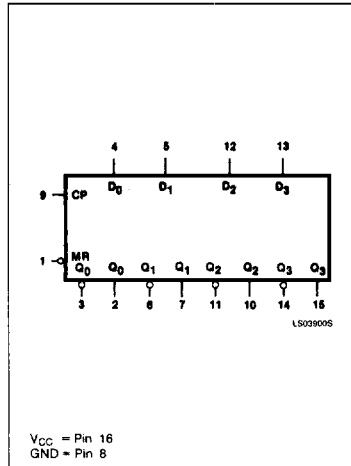
NOTE:

Where a 74 unit load (ul) is understood to be $40\mu A I_{IH}$ and $-1.6mA I_{IL}$, a 74S unit load (Sul) is $50\mu A I_{IH}$ and $-2.0mA I_{IL}$, and a 74LS unit load (LSul) is $20\mu A I_{IH}$ and $-0.4mA I_{IL}$.

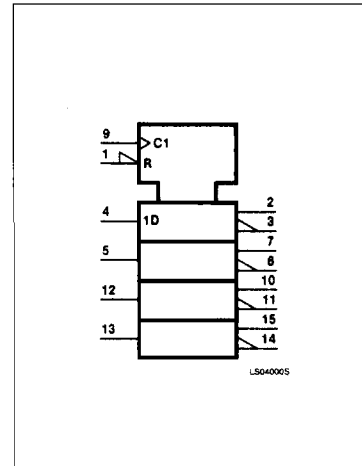
PIN CONFIGURATION



LOGIC SYMBOL



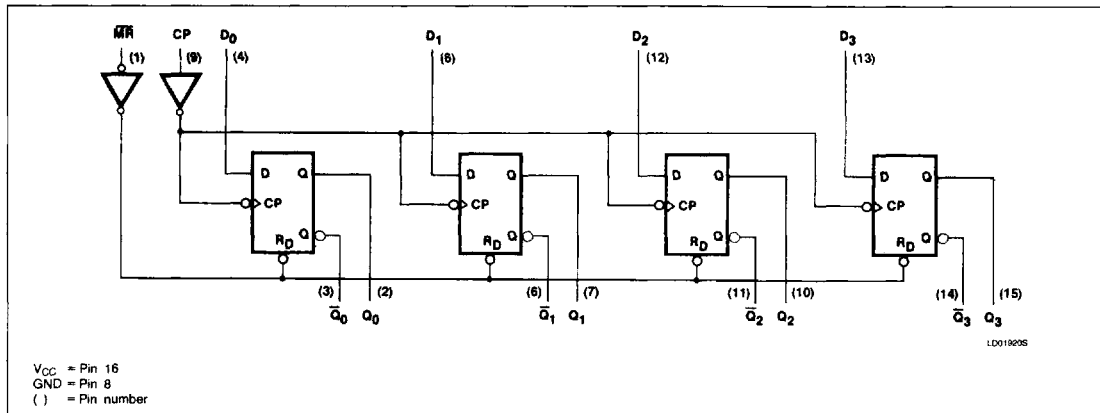
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	\overline{MR}	CP	D_n	Q_n	\overline{Q}_n
Reset (clear)	L	X	X	L	H
Load "1"	H	↑	h	H	L
Load "0"	H	↑	l	L	H

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER		74	74LS	74S	UNIT
V_{CC}	Supply voltage	7.0	7.0	7.0	V
V_{IN}	Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN}	Input current	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT}	Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A	Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max		
V_{CC}	Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH}	HIGH-level input voltage	2.0			2.0			2.0			V
V_{IL}	LOW-level input voltage			+0.8			+0.8			+0.8	V
I_{IK}	Input clamp current			-12			-18			-18	mA
I_{OH}	HIGH-level output current			-800			-400			-1000	μA
I_{OL}	LOW-level output current			16			8			20	mA
T_A	Operating free-air temperature	0		70	0		70	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹	74175			74LS175			74S175			UNIT
		Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max	
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX	2.4	3.4		2.7	3.4		2.7	3.4		V
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX	0.2	0.4		0.35	0.5			0.5	V
		I _{OL} = 4mA (74LS)				0.25	0.4				V
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}			-1.5			-1.5			-1.2	V
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V		1.0						1.0	mA
		V _I = 7.0V					0.1				mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V		40							μA
		V _I = 2.7V					20		50		μA
I _{IL} LOW-level input current	V _{CC} = MAX	V _I = 0.4V		-1.6			-0.4				mA
		V _I = 0.5V							-2.0		mA
I _{OS} Short-circuit output current ³	V _{CC} = MAX	-18		-57	-20		-100	-40		-100	mA
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX		30	45		11	18		60	96	mA

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- With all outputs open and 4.5V applied to all Data and Master Reset inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		C _L = 15pF, R _L = 400Ω		C _L = 15pF, R _L = 2kΩ		C _L = 15pF, R _L = 280Ω		
		Min	Max	Min	Max	Min	Max	
f _{MAX} Maximum clock frequency	Waveform 1	25		30		75		MHz
t _{PLH} Propagation delay t _{PHL} Clock to outputs	Waveform 1		30		25		12	ns
			35		25		17	
t _{PLH} Propagation delay t _{PHL} MR to outputs	Waveform 3		25		30		15	ns
			35		30		22	

NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r, t_f, pulse width or duty cycle.



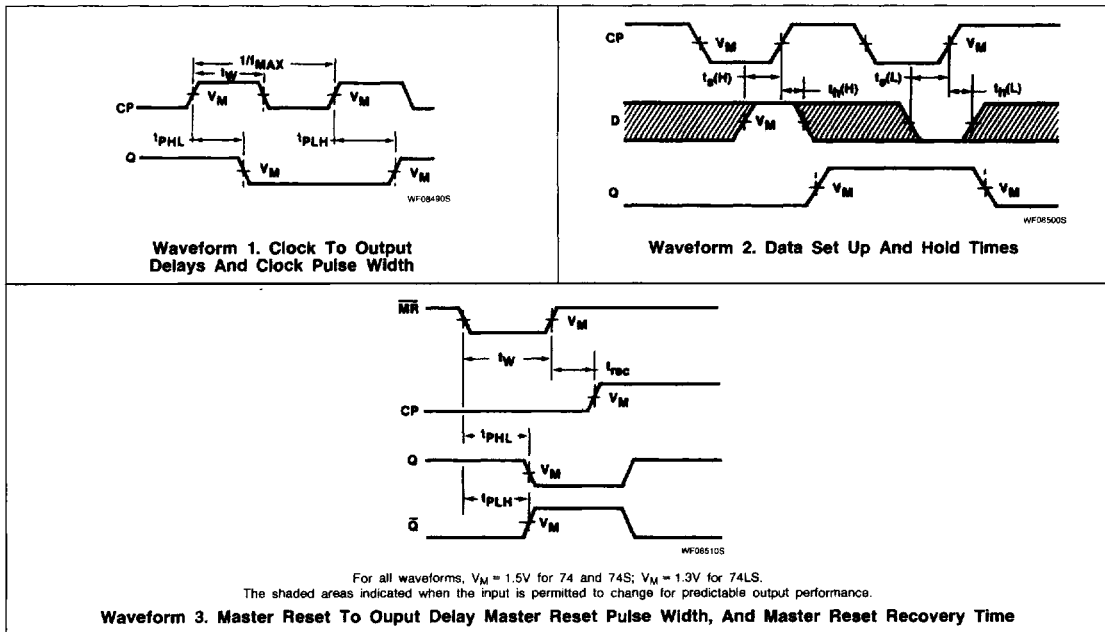
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AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		Min	Max	Min	Max	Min	Max	
t_W	Clock pulse width	Waveform 1	20		20		7	ns
t_W	Master Reset pulse width	Waveform 3	20		20		10	ns
$t_s(H)$	Set-up time, HIGH data to CP	Waveform 2	20		20		5	ns
$t_h(H)$	Hold time, HIGH data to CP	Waveform 2	5		5		3	ns
$t_s(L)$	Set-up time, LOW data to CP	Waveform 2	20		20		5	ns
$t_h(L)$	Hold time, LOW data to CP	Waveform 2	5		5		3	ns
t_{rec}	Recovery time, \overline{MR} to CP	Waveform 3	25		25		5	ns

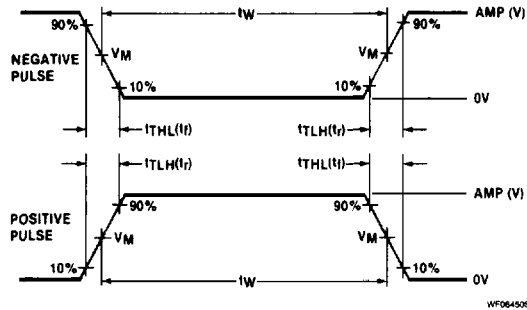
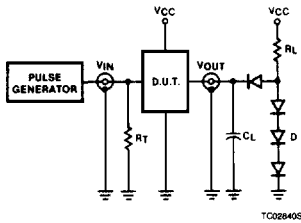
AC WAVEFORMS



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TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns