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April 1<sup>st</sup>, 2010 Renesas Electronics Corporation

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#### 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

## DESCRIPTION

The M5M5V416CWG is a family of low voltage 4-Mbit static RAMs - Single 2.7~3.6V power supply organized as 262144-words by 16-bit, fabricated by Renesas's high-performance 0.18µm CMOS technology.

The M5M5V416C is suitable for memory applications where a simple interfacing, battery operating and battery backup are the important design objectives.

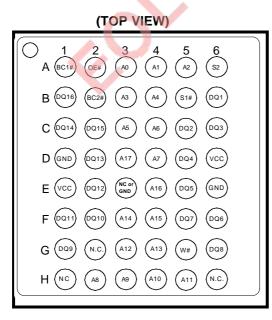
M5M5V416CWG is packaged in a CSP (chip scale package), with the outline of 7.0mm x 8.5mm, ball matrix of 6 x 8 (48ball) and ball pitch of 0.75mm. It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

## **FEATURES**

- Small stand-by current: 0.2µA (3.00V, typ.)
- No clocks. No refresh
- Data retention supply voltage =2.0V
- All inputs and outputs are TTL compatible.
- Easy memory expansion by S1#, S2, BC1# and BC2#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention in the I/O bus
- Process technology: 0.18µm CMOS
- Package: 48ball 7.0mm x 8.5mm CSP

Version,		_			Sta	and-by	current	: (µA)			Activ e
Operating	Part name	Power	Access time	* Typica	al(3.0V)	R	atings	(max.	@3.6V	)	current Icc1
temperature		Supply	max.	25°C	40°C	Voltage	25°C	40°C	70°C	85°C	(3.0V, typ.)
	M5M5V416CWG -55HI		55ns		5	3.0V	1.0	2.0	10	20	30mA
I-version -40 ~ +85°C		2.7 ~ 3.6V		0.2	0.4	3.3V	1.5	2.5	10	20	(10MHz) 5mA
	M5M5V416CWG -70HI		70ns			3.6V	2.5	4.0	10	20	(1MHz)

## **PIN CONFIGURATION**



\* Typical parameter indicates the value for the center

of distribution, and not 100% tested.

Pin	Function
A0 ~ A17	Address input
DQ1 ~ DQ16	Data input / output
S1#	Chip select input 1
S2	Chip select input 2
W#	Write control input
OE#	Output enable input
BC1#	Lower Byte (DQ1 ~ 8)
BC2#	Upper Byte (DQ9~16)
Vcc	Power supply
GND	Ground supply

Outline: 48FJA NC: No Connection \*Don't connect E3 ball to voltage level more than 0V.



#### 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

## **FUNCTION**

The M5M5V416CWG is organized as 262144-words by 16-bit. These devices operate on a single +2.7~3.6V power supply, and are directly TTL compatible to both input and output. Its fully static circuit needs no clocks and no refresh, and makes it useful.

The operation mode are determined by a combination of the device control inputs BC1# , BC2# , S1#, S2 , W# and OE#. Each mode is summarized in the function table.

A write operation is executed whenever the low level W# overlaps with the low level BC1# and/or BC2# and the low level S1# and the high level S2. The address(A0~A17) must be set up before the write cycle and must be stable during the entire cycle.

A read operation is executed by setting W# at a high level and OE# at a low level while BC1# and/or BC2# and S1# and S2 are in an active state(S1#=L,S2=H).

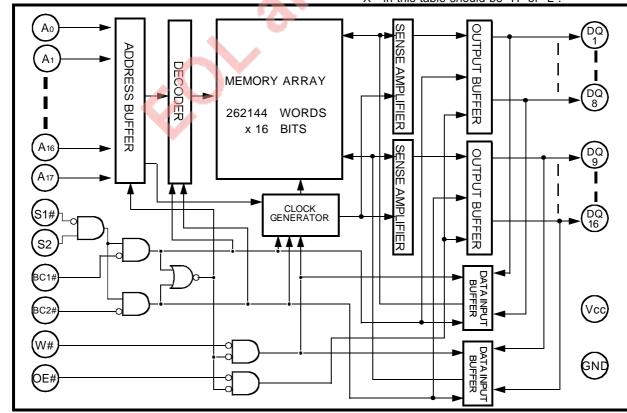
When setting BC1# at the high level and other pins are in an active stage, upper-byte are in a selectable mode in which both reading and writing are enabled, and lower-byte are in a non-selectable mode. And when setting BC2# at a high level and other pins are in an active stage, lowerbyte are in a selectable mode and upper-byte are in a non-selectable mode. When setting BC1# and BC2# at a high level or S1# at a high level or S2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by BC1#, BC2# and S1#, S2.

The power supply current is reduced as low as  $0.2\mu A(25^{\circ}C, typical)$ , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.



S2	BC1#	BC2#	W#	OE#	Mode	DQ1~8	DQ9~16	Icc
L	Х	Х	Х	Х	Non selection	High-Z	High-Z	Standby
Н	Х	Х	Х	X	Non selection	High-Z	High-Z	Standby
Х	Н	Н	Х	X	Non selection	High-Z	High-Z	Standby
Н	L	Н	L	X	Write	Din	High-Z	Activ e
Н	L	H	H	L	Read	Dout	High-Z	Activ e
Н	L	H	Η	Н		High-Z	High-Z	Activ e
Н	H	L	Ľ	Х	Write	High-Z	Din	Activ e
H	H	L	Н	L	Read	High-Z	Dout	Activ e
H	H	L	Н	Н		High-Z	High-Z	Activ e
H	L	L	L	Х	Write	Din	Din	Activ e
Н	L	L	Н	L	Read	Dout	Dout	Activ e
H	L	L	Н	Н		High-Z	High-Z	Activ e
			L  X  X    H  X  X    X  H  H    H  L  H    H  L  H    H  L  H    H  L  H    H  L  H    H  L  H    H  L  H    H  H  L    H  H  L    H  H  L    H  H  L    H  H  L    H  H  L	X      X      X        H      X      X      X        X      H      H      X        X      H      H      X        H      L      H      L        H      L      H      H        H      L      H      H        H      L      H      H        H      L      H      H        H      L      H      H        H      H      L      H        H      H      L      H        H      H      L      H        H      H      L      H        H      L      L      H        H      L      L      H	L  X  X  X    H  X  X  X    H  X  X  X    X  H  H  X  X    X  H  H  X  X    H  L  H  L  X    H  L  H  L  X    H  L  H  H  L    H  L  H  H  H    H  L  H  H    H  H  L  H    H  H  L  H    H  H  L  H    H  L  L  K    H  L  L  K	L    X    X    X    X    Non selection      H    X    X    X    Non selection      X    H    H    X    X    Non selection      X    H    H    X    X    Non selection      H    L    H    L    X    Write      H    L    H    L    Read      H    L    H    H    Ead      H    L    H    H    —      H    L    H    H    Ead      H    H    L    L    X    Write      H    H    L    H    L    Read      H    H    L    L    X    Write      H    L    L    L    X    Write      H    L    L    H    H    —	L    X    X    X    X    Non selection    High-Z      H    X    X    X    Non selection    High-Z      X    H    H    X    Non selection    High-Z      X    H    H    X    Non selection    High-Z      H    L    H    L    X    Write    Din      H    L    H    L    Read    Dout      H    L    H    H    —    High-Z      H    L    H    H    —    High-Z      H    L    H    H    —    High-Z      H    H    L    L    X    Write    High-Z      H    H    L    L    X    Write    High-Z      H    H    L    H    L    Read    High-Z      H    H    L    H    H    —    High-Z      H    H    L    H    H    —    High-Z      H    H    L    H    H </td <td>L    X    X    X    X    Non selection    High-Z    High-Z      H    X    X    X    Non selection    High-Z    High-Z      X    H    H    X    X    Non selection    High-Z    High-Z      X    H    H    X    X    Non selection    High-Z    High-Z      H    L    H    L    X    Write    Din    High-Z      H    L    H    L    Read    Dout    High-Z      H    L    H    H    —    High-Z    High-Z      H    L    H    H    —    High-Z    Din      H    L    H    H    —    High-Z    Din      H    L    H    H    —    High-Z    Din      H    H    L    X    Write    High-Z    Dout      H    H    L    Read    High-Z    Dout    High-Z      H    H    L    Read    High-Z    Dout    Dout</td>	L    X    X    X    X    Non selection    High-Z    High-Z      H    X    X    X    Non selection    High-Z    High-Z      X    H    H    X    X    Non selection    High-Z    High-Z      X    H    H    X    X    Non selection    High-Z    High-Z      H    L    H    L    X    Write    Din    High-Z      H    L    H    L    Read    Dout    High-Z      H    L    H    H    —    High-Z    High-Z      H    L    H    H    —    High-Z    Din      H    L    H    H    —    High-Z    Din      H    L    H    H    —    High-Z    Din      H    H    L    X    Write    High-Z    Dout      H    H    L    Read    High-Z    Dout    High-Z      H    H    L    Read    High-Z    Dout    Dout

note) "H" and "L" in this table mean VIH and VIL, respectively. "X" in this table should be "H" or "L".



Renesas Technology Corp.

#### **BLOCK DIAGRAM**

## 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

# **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Conditions	Ratings	Units
Vcc	Supply voltage	With respect to GND	-0.5* ~ +4.6	
Vı	Input voltage	With respect to GND	-0.3* ~ Vcc + 0.3	V
Vo	Output voltage	With respect to GND	0 ~ Vcc	
Pd	Power dissipation	Ta=25°C	700	mW
Ta	Operating temperature	I-v ersion	- 40 ~ +85	°C
T stg	Storage temperature		- 65 ~ +150	°C

\* -3.0V in case of AC (Pulse width  $\leq$  30ns)

# DC ELECTRICAL CHARACTERISTICS

(Vcc=2.7 ~ 3.6V, unless noted.)

Question	Demonster	Qualities				0	Limits	6	
Symbol	Parameter	Conditions			C 1	Min	Тур	Max	Units
Vн	High-lev el input voltage					2.2		Vcc+0.2V	
V⊾	Low-lev el input voltage					-0.2 *		0.4	V
Vон	High-level output voltage	lон= -0.5mA				2.4			v
Va	Low-lev el output voltage	la_=2mA		1				0.4	
h	Input leakage current	Vi=0 ~ Vcc						±1	
lo	Output leakage current	BC1#and BC2#=VIH or S1#=VIH or S2=VIL or OF	E# = MH, WO=0	~ Vcc				±1	μA
1001	Active supply current	BC1# and BC2# $\leq$ 0.2V, S1# $\leq$ 0.2V, S2 $\geq$ Vcc-0.2V other inputs $\leq$ 0.2V or $\geq$ Vcc-0.2V		f	= 10MHz	-	30	50	
Icc1	(AC,MOS level)	Output-open (duty 100%)		f	= 1MHz	-	5	10	mA
	Active supply current	BC1# and BC2# =V L, S1# =V L,S2 other pins =V H or V L	=V IH	f	= 10MHz	-	30	50	
lcc2	(AC,TTL level)	Output - open (duty 100%)		f	= 1MHz	-	5	10	
					3.0V			1.0	
		(1) S1# > Vcc-0.2V,	~ +25°	С	3.3V	-	0.2	1.5	
		$S2 \ge Vcc - 0.2V$ ,			3.6V			2.5	
Icc3	Stand by supply current	other inputs = $0 \sim Vcc$ (2) S2 $\leq 0.2V$ ,			3.0V			2.0	
	(MOS level)	other inputs = $0 \sim Vcc$ (3) BC1# and BC2# $\geq Vcc - 0.2V$	~ +40°	С	3.3V	-	0.4	2.5	μA
		S1# $\leq$ 0.2V, S2 $\geq$ Vcc - 0.2V other inputs = 0 ~ Vcc			3.6V			4.0	
		orner inputs = 0 ~ VCC	~ +70°	С	3.0V~3.6V	-	-	10	
			~ +85°	С	3.0V~3.6V	-	-	20	
lcc4	Stand by supply current ( TTL level )	BC1# and BC2# =V⊮ or S1# =V⊮ Other inputs= 0 ~ Vcc	H or S2=VI	L		-	-	2	mA

Note 1: Direction for current flowing into IC is indicated as positive (no mark) \* -1.0V in case of AC (Pulse width  $\leq$  30ns) Note 2: Typical parameter indicates the value for the center of distribution at 3.00V, and is not 100% tested.

# CAPACITANCE

(Vcc=2.7 ~ 3.6V, unless noted. )

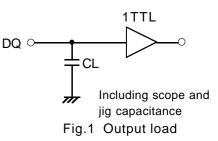
Svmbo	Parameter	Conditions		Limits	5	
Symbo	Farameter	Conditions	Min	Тур	Max	Units
Cı	Input capacitance	V⊨GND, V⊨25mVrms, f=1MHz			10	рF
Co	Output capacitance	Vo=GND,Vo=25mVrms, f=1MHz			10	рг



#### 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

## AC ELECTRICAL CHARACTERISTICS (Vcc=2.7 ~ 3.6V, unless noted. ) (1) TEST CONDITIONS

Supply voltage	2.7~3.6V					
Input pulse	V⊮=2.4V, V⊾=0.2V					
Input rise time and fall time	5ns					
Reference level	$V_{0H} = V_{0L} = 1.50V  \begin{array}{c} \text{Transition is measured } \pm 200 \text{mV from} \\ \text{steady state voltage.(for ten,tdis)} \end{array}$					
	Fig.1,CL=30pF					
Output loads	CL=5pF (for ten,tdis)					



# (2) READ CYCLE

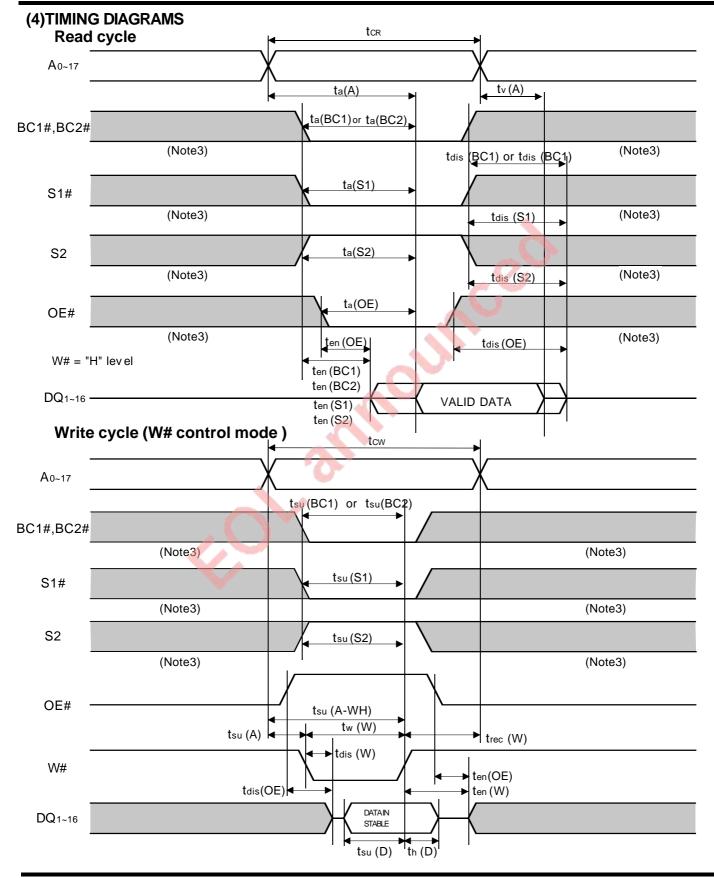
		Lin	nits	Lin	nits	
Symbol	Parameter		HI	70HI		Units
-		Min	Max	Min	Max	
tcr	Read cycle time	55		70		ns
ta(A)	Address access time	<u> </u>	55		70	ns
ta(S1)	Chip select 1 access time		55		70	ns
ta(S2)	Chip select 2 access time		55		70	ns
ta(BC1)	Byte control 1 access time		55		70	ns
ta(BC2)	Byte control 2 access time		55		70	ns
ta(OE)	Output enable access time		30		35	ns
tdis(S1)	Output disable time after S1# high		20		25	ns
tdis(S2)	Output disable time after S2 low		20		25	ns
tdis(BC1)	Output disable time after BC1# high		20		25	ns
tdis(BC2)	Output disable time after BC2# high		20		25	ns
tdis(OE)	Output disable time after OE# high		20		25	ns
ten(S1)	Output enable time after S1# low	10		10		ns
ten(S2)	Output enable time after S2 high	10		10		ns
ten(BC1)	Output enable time after BC1# low	5		5		ns
ten(BC2)	Output enable time after BC2# low	5		5		ns
ten(OE)	Output enable time after OE# low	5		5		ns
t∨(A)	Data valid time after address	10		10		ns

# (3) WRITE CYCLE

		Lin	nits	Lin	nits	
Symbol	Parameter	55	55HI		70HI	
<u>,</u>		Min	Max	Min	Max	
tcw	Write cycle time	55		70		ns
t <sub>w</sub> (W)	Write pulse width	45		55		ns
tsu(A)	Address setup time	0		0		ns
tsu(A-WH)	Address setup time with respect to W#	50		60		ns
tsu(BC1)	Byte control 1 setup time	50		60		ns
tsu(BC2)	Byte control 2 setup time	50		60		ns
tsu(S1)	Chip select 1 setup time	50		60		ns
tsu(S2)	Chip select 2 setup time	50		60		ns
tsu(D)	Data setup time	30		35		ns
th(D)	Data hold time	0		0		ns
trec(W)	Write recovery time	0		0		ns
tdis(W)	Output disable time from W# low		20		25	ns
tdis(OE)	Output disable time from OE# high		20		25	ns
ten(W)	Output enable time from W# high	5		5		ns
ten(OE)	Output enable time from OE# low	5		5		ns

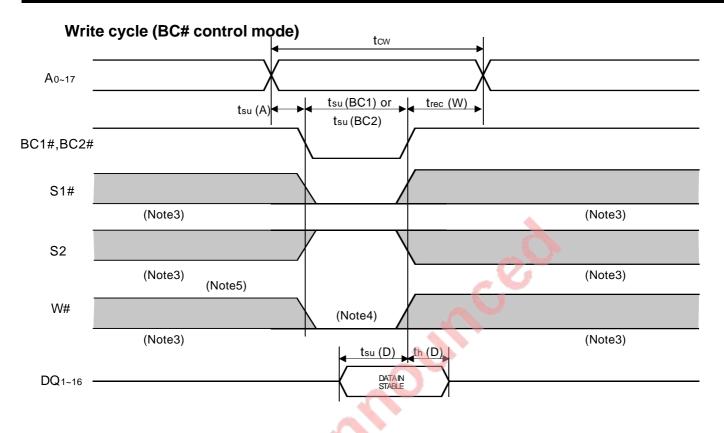


## 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM





### 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM



Note 3: Hatching indicates the state is "don't care"

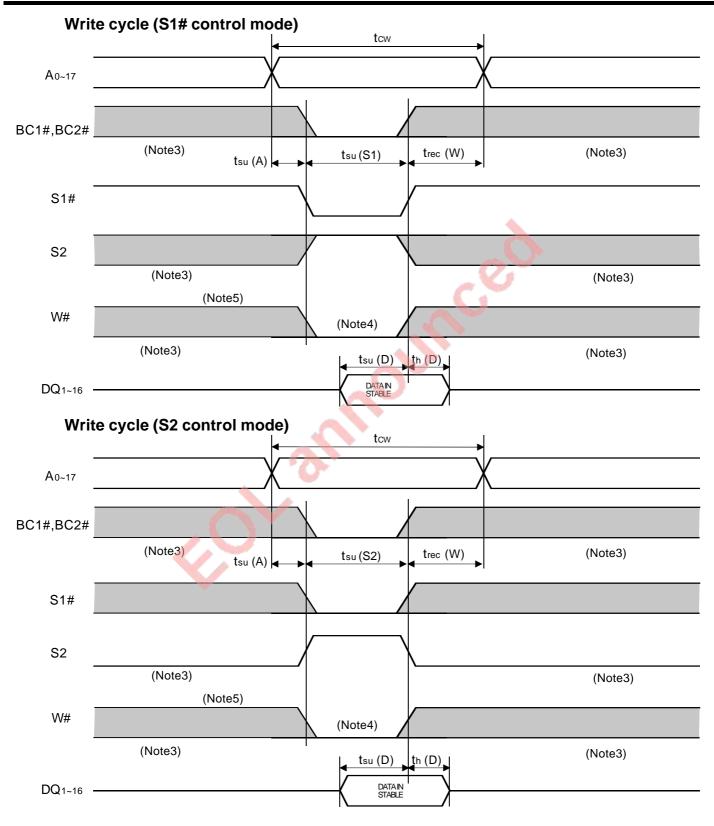
Note 4: A Write occurs during S1# low, S2 high ov erlaps BC1# and/or BC2# low and W# low.

Note 5: When the falling edge of W# is simultaneously or prior to the falling edge of BC1# and/or BC2# or the falling edge of S1# or rising edge of S2, the outputs are maintained in the high impedance state.

Note 6: Don't apply inverted phase signal externally when DQ pin is in output mode.



## 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM





## 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

# POWER DOWN CHARACTERISTICS

# (1) ELECTRICAL CHARACTERISTICS

Ourse had	Devementer				Limits		
Symbol	Parameter	Test conditions		Min	Тур	Max	Units
Vcc (PD)	Power down supply voltage			2.0			V
	Byte control input BC1# &	2.2V <u>≤</u> Vcc(PD)		2.2			.,
VI (BC)	BC2#	2.0V <u>≤</u> Vcc(PD) <u>≤</u> 2.2V			Vcc(PD)		V
Much		$2.2V \leq Vcc(PD)$		2.2			
VI (S1)	Chip select input S1#	$2.0V \leq Vcc(PD) \leq 2.2V$			Vcc(PD)		V
VI (S2)	Chip select input S2					0.2	V
		Vcc=2.0V (1) S1#≥Vcc-0.2V,	~ +25°C	-	0.05	0.8	
Icc (PD)	Power down	other inputs = $0 \sim Vcc$ (2) S2 $\leq 0.2V$ ,	~ +40°C		0.1	1.5	
100 (12)	supply current	other inputs = $0 \sim Vcc$ (3) BC1# and BC2# $\geq Vcc - 0.2V$	~ +70°C	0	-	7.5	μA
		S1#≤0.2V, S2≥Vcc-0.2V other inputs=0~Vcc	~ +85°C		-	15	

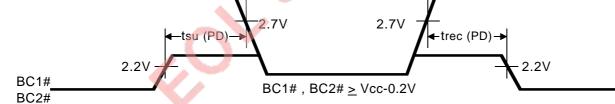
## (2) TIMING REQUIREMENTS

Note 7: Typical parameter of Icc(PD) indicates the value for the center of distribution at 2.0V, and not 100% tested.

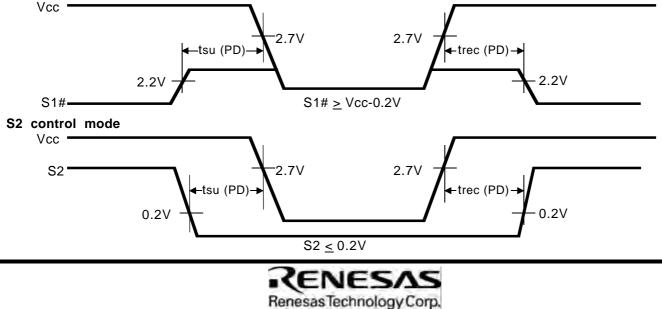
Symbol						
Symbol	Parameter	Test conditions	Min	Тур	Max	Units
tsu (PD)	Power down set up time		0			ns
trec (PD)	Power down recovery time		5			ms

# (3) TIMING DIAGRAM

**BC# control mode** On the BC# control mode, the level of S1# and S2 must be fixed at S1#, S2  $\geq$  Vcc-0.2V or S2  $\leq$  0.2V.



**S1# control mode** On the S1# mode, the level of S2 must be fixed at S2  $\geq$  Vcc-0.2V or S2  $\leq$  0.2V.



#### 4194304-BIT (262144-WORD BY 16-BIT) CMOS STATIC RAM

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#### Keep safety first in your circuit designs!

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