512Kx8 bit Low Power CMOS Static RAM

FEATURES

- Process Technology : 0.4•• CMOS
- Organization : 512Kx8
- Power Supply Voltage : Single 5V •• 10%
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard 32-DIP, 32-SOP, 32-TSOP(II)-Forward/Reverse

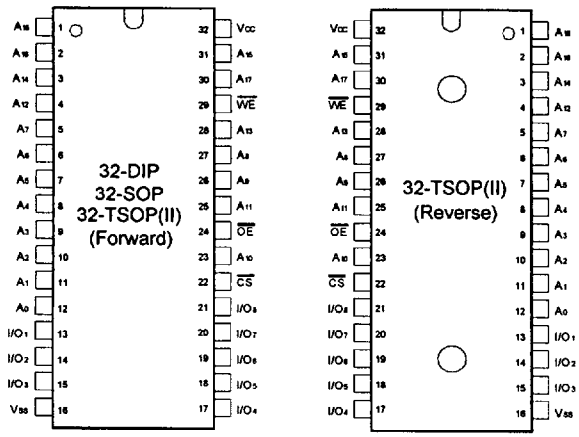
GENERAL DESCRIPTION

The KM684000A family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

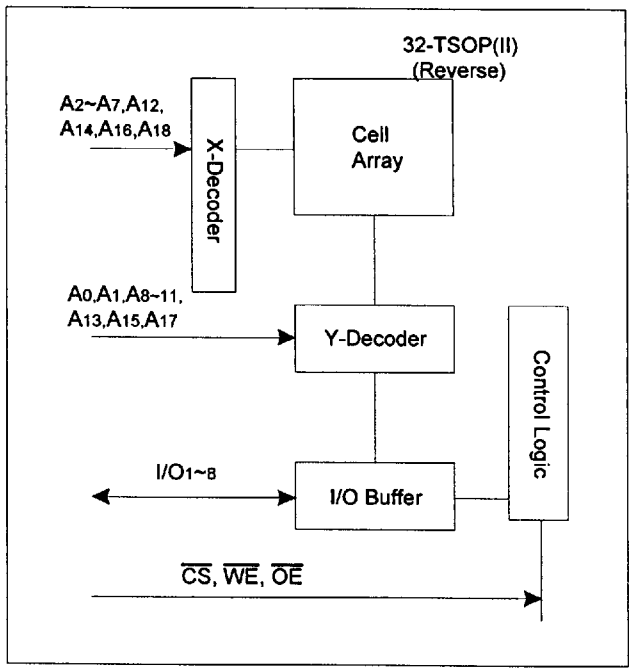
Product Family	Operating Temperature.	Vcc Range (V)	Speed (ns)	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2})	
KM684000AL KM684000AL-L	Commercial (0~70••)	4.5~5.5V	55/70ns	100•• 20••	90mA	32-DIP,32SOP 32-TSOP(II)-R/F
KM684000ALI KM684000ALI-L	Industrial (-40~85••)	4.5~5.5V	70/100ns	100•• 50••		32-SOP 32-TSOP(II)-R/F

PIN DESCRIPTION



Pin Name	Function
A_0~A_{18}	Address Inputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input
$\overline{OE}$	Output Enable Input
I/O_1~I/O_8	Data Inputs/Outputs
Vcc	Power (5V)
Vss	Ground

FUNCTIONAL BLOCK DIAGRAM

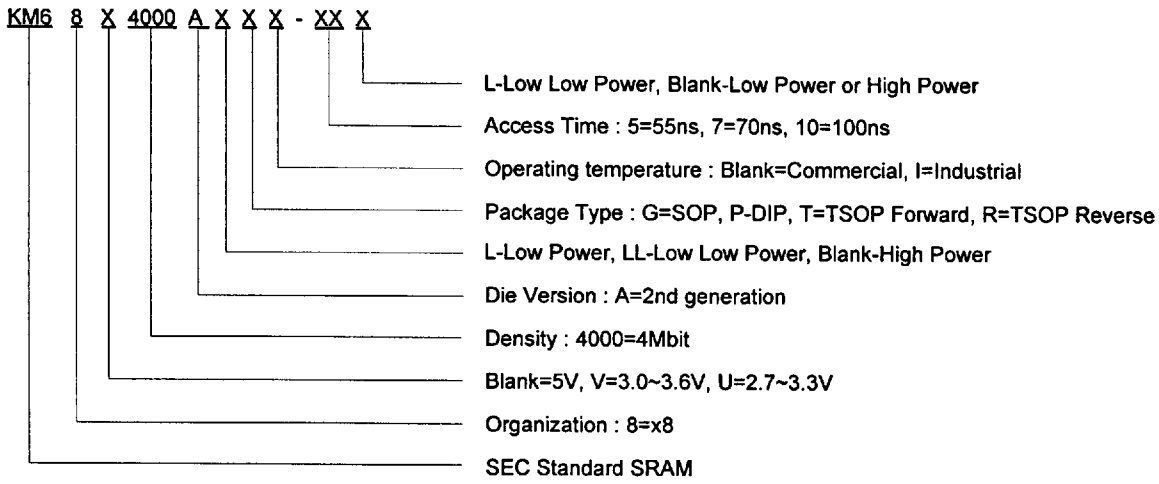


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Product (0~70••)		Industrial Temp Products (-40~85••)	
Part Name	Function	Part Name	Function
KM684000ALP-5	32-DIP, 55ns, L-pwr	KM684000ALGI-7	32-SOP,70ns, L-pwr
KM684000ALP-5L	32-DIP, 55ns, LL-pwr	KM684000ALGI-7L	32-SOP, 70ns, LL-pwr
KM684000ALP-7	32-DIP, 70ns, L-pwr	KM684000ALGI-10	32-SOP, 100ns, L-pwr
KM684000ALP-7L	32-DIP, 70ns, LL-pwr	KM684000ALGI-10L	32-SOP, 100ns, LL-pwr
KM684000ALG-5	32-SOP, 55ns, L-pwr	KM684000ALTI-7	32-TSOP(II)F, 70ns, L-pwr
KM684000ALG-5L	32-SOP, 55ns, LL-pwr	KM684000ALTI-7L	32T-SOP(II)F, 70ns, LL-pwr
KM684000ALG-7	32-SOP, 70ns, L-pwr	KM684000ALTI-10	32-TSOP(II)F, 100ns, L-pwr
KM684000ALG-7L	32-SOP, 70ns, LL-pwr	KM684000ALTI-10L	32-TSOP(II)F, 100ns, LL-pwr
KM684000ALT-5	32-TSOP(II)F, 55ns, L-pwr	KM684000ALRI-7	32-TSOP(II)R, 70ns, L-pwr
KM684000ALT-5L	32-TSOP(II)F, 55ns, LL-pwr	KM684000ALRI-7L	32T-SOP(II)R, 70ns, LL-pwr
KM684000ALT-7	32-TSOP(II)F, 70ns, L-pwr	KM684000ALRI-10	32-TSOP(II)R, 100ns, L-pwr
KM684000ALT-7L	32-TSOP(II)F, 70ns, LL-pwr	KM684000ALRI-10L	32-TSOP(II)R, 100ns, LL-pwr
KM684000ALR-5	32-TSOP(II)R, 55ns, L-pwr		
KM684000ALR-5L	32-TSOP(II)R, 55ns, LL-pwr		
KM684000ALR-7	32-TSOP(II)R, 70ns, L-pwr		
KM684000ALR-7L	32-TSOP(II)R, 70ns, LL-pwr		

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to 7.0	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.5 to 7.0	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	••	-
Operating Temperature	T_A	0 to 70	••	KM684000AL/L-L
		-40 to 85	••	KM684000ALI/LI-L
Soldering temperature and time	T_{SOLDER}	260••, 10sec (Lead Only)	-	-

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stres s rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input high voltage	V_{IH}	2.2	-	Vcc+0.5V	V
Input low voltage	V_{IL}	-0.5***	-	0.8	V

* 1) Commercial Product : T_A=0 to 70••, unless otherwise specified
2) Industrial Product : T_A=-40 to 85••, unless otherwise specified
** T_A=25••
*** V_{IL}(min)=-3.0V for •• 50ns pulse width

CAPACITANCE* (f=1MHz, T_A=25••)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

* Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	••
Output leakage current		I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL} V_{IO}=Vss to Vcc		-1	-	1	••
Operating power supply current		I_{CC}	$\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, I_{IO}=0mA	Read	-	-	15	mA
				Write	-	-	35	
Average operating current		I_{CC1}	Cycle time=1•• 100% duty I_{IO}=0mA $\overline{CS}$••0.2V, V_{IL}••0.2V V_{IH}••Vcc-0.2V	Read	-	-	15	mA
				Write	-	-	35	
		I_{CC2}	Min cycle, 100% duty $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, I_{IO}=0mA		-	-	90	mA
Output low voltage		V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage		V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)		I_{SB}	$\overline{CS}$=V_{IH}		-	-	3	mA
Standby Current (CMOS)	KM684000AL/L-L	I_{SB1}	$\overline{CS}$••Vcc-0.2V Others=0~Vcc	Low Power	-	-	100	••
				Low Low Power	-	-	20	••
	KM684000ALI/L-L			Low Power	-	-	100	••
				Low Low Power	-	-	50	••

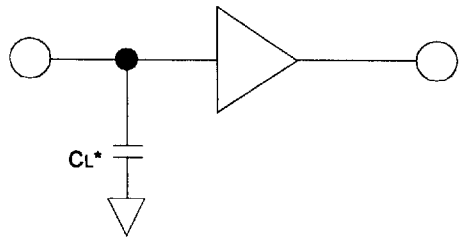
* 1) Commercial Product : T_A=0 to 70••, Vcc=5V••10% unless otherwise specified
2) Industrial Product : T_A=-40 to 85••, Vcc=5V••10% unless otherwise specified
** T_A=25••

A.C CHARACTERISTICS

TEST CONDITIONS(1.Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.8 to 2.4V	-
Input rising & falling time	5ns	-
input and output reference voltage	1.5V	-
Output load (See right)	*C_L=100pF+1TLL	-

* See DC Operating conditions



* Including scope and jig capacitance

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM684000AL/L-L	0~70••	5V •• 10%	55/70ns	Commercial
KM684000ALI/LI-L	-40~85••	5V •• 10%	70/100ns	Industrial

PARAMETER LIST FOR EACH SPEED BIN

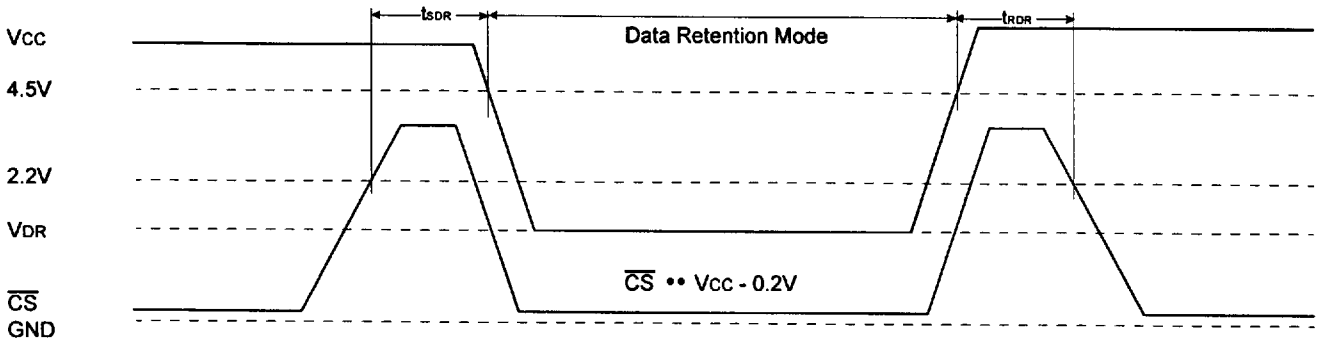
Parameter List		Symbol	Speed Bins						Units
			55ns		70ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	55	-	70	-	100	-	ns
	Address access time	tAA	-	55	-	70	-	100	ns
	Chip select to output	tCO	-	55	-	70	-	100	ns
	Output enable to valid output	tOE	-	25	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	20	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	20	0	25	0	30	ns
	Output hold from address change	tOH	10	-	10	-	10	-	ns
Write	Write cycle time	tWC	55	-	70	-	100	-	ns
	Chip select to end of write	tCW	45	-	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	45	-	60	-	80	-	ns
	Write pulse width	tWP	40	-	50	-	60	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	20	0	25	0	30	ns
	Data to write time overlap	tDW	25	-	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	V_{DR}		$\overline{CS}$••Vcc-0.2V		2.0	-	5.5	V
Data retention current	I_{DR}	KM684000AL/L-L	Vcc=3.0V $\overline{CS}$••Vcc-0.2V	L-Ver	-	-	50	••
				LL-Ver	-	-	15	
		KM684000ALI/LI-L		L-Ver	-	-	50	
				LL-Ver	-	-	20	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70 ••, unless otherwise specified
2) Industrial Product : Ta=-40 to 85 ••, unless otherwise specified
** T_A=25••

DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

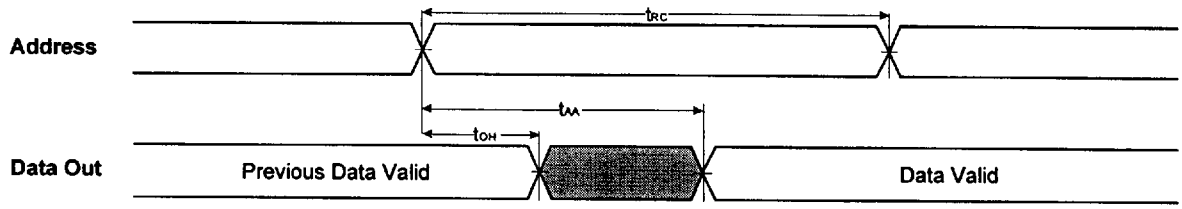
$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	Dout	I_{CC}
L	L	X	Write	Din	I_{CC}

* X means don't care

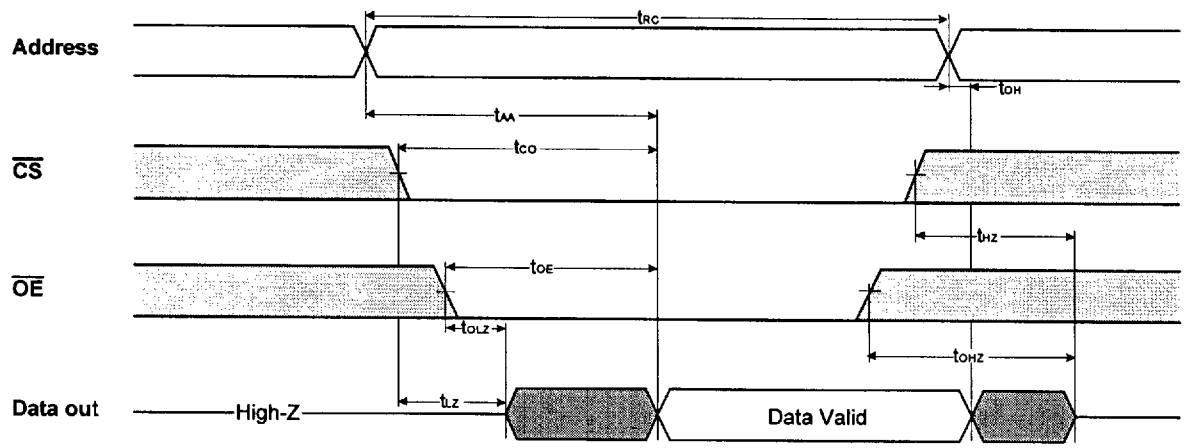
TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)

(CS=OE=V_{IL}, WE=V_{IH})



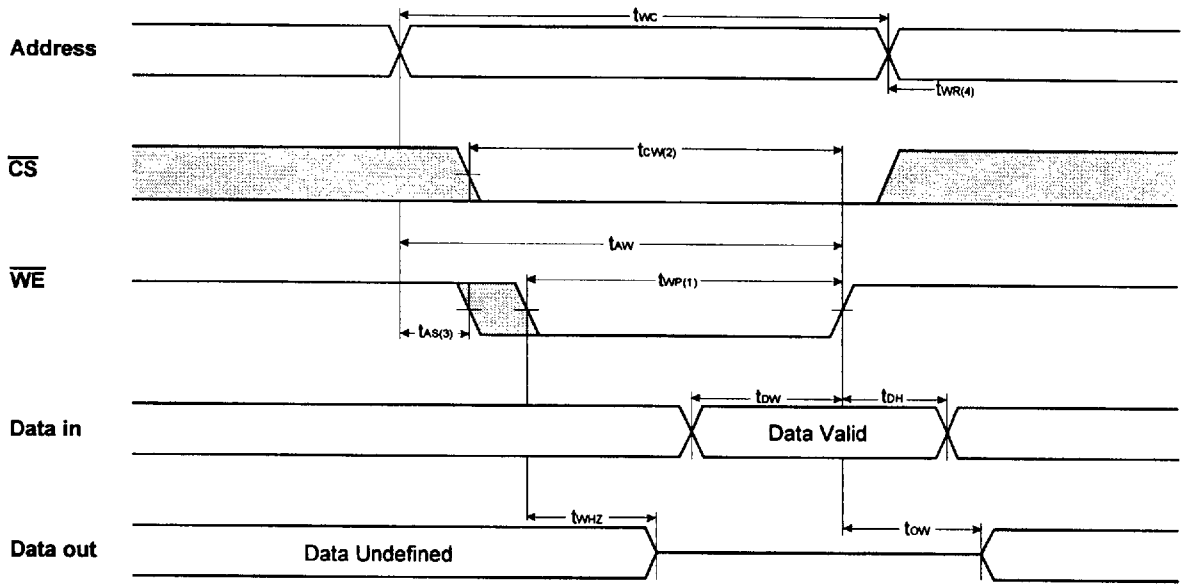
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



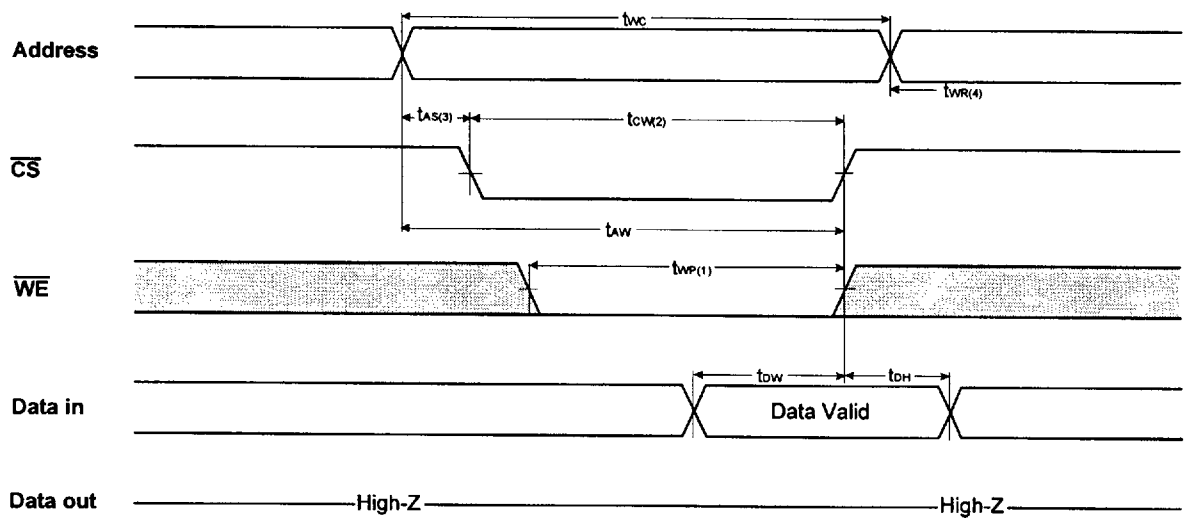
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage le vels.
2. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE(1)($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2)($\overline{CS}$ Controlled)



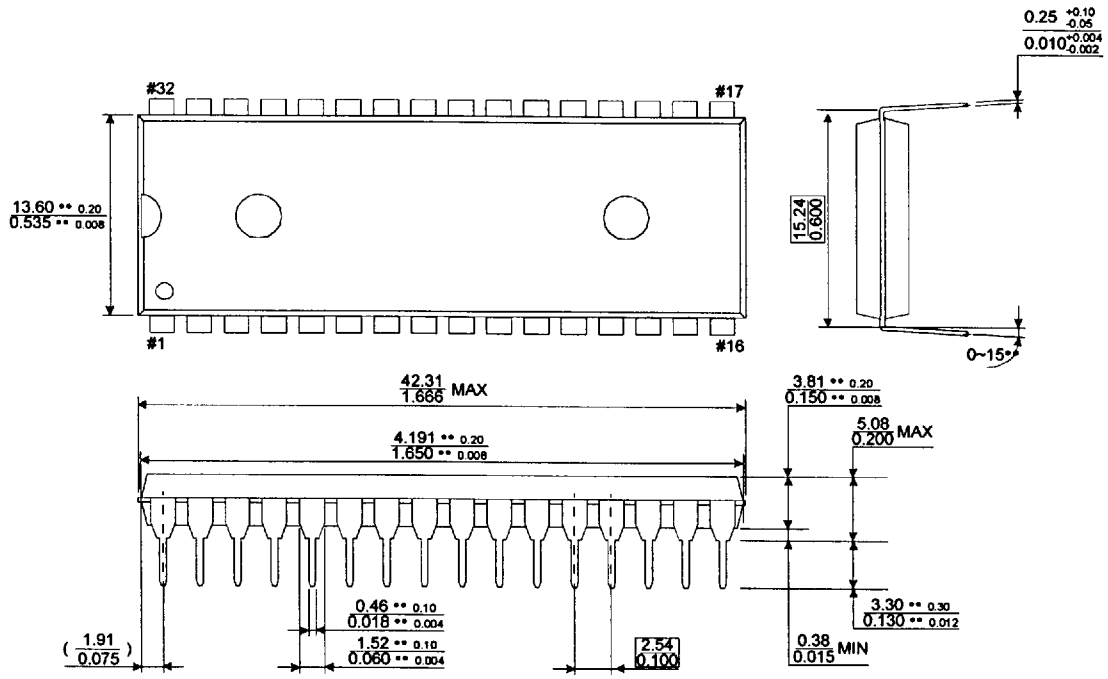
NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$. A write begins at the latest transition among $\overline{CS}$ going low and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS}$ going high and $\overline{WE}$ going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$, or $\overline{WE}$ going high.

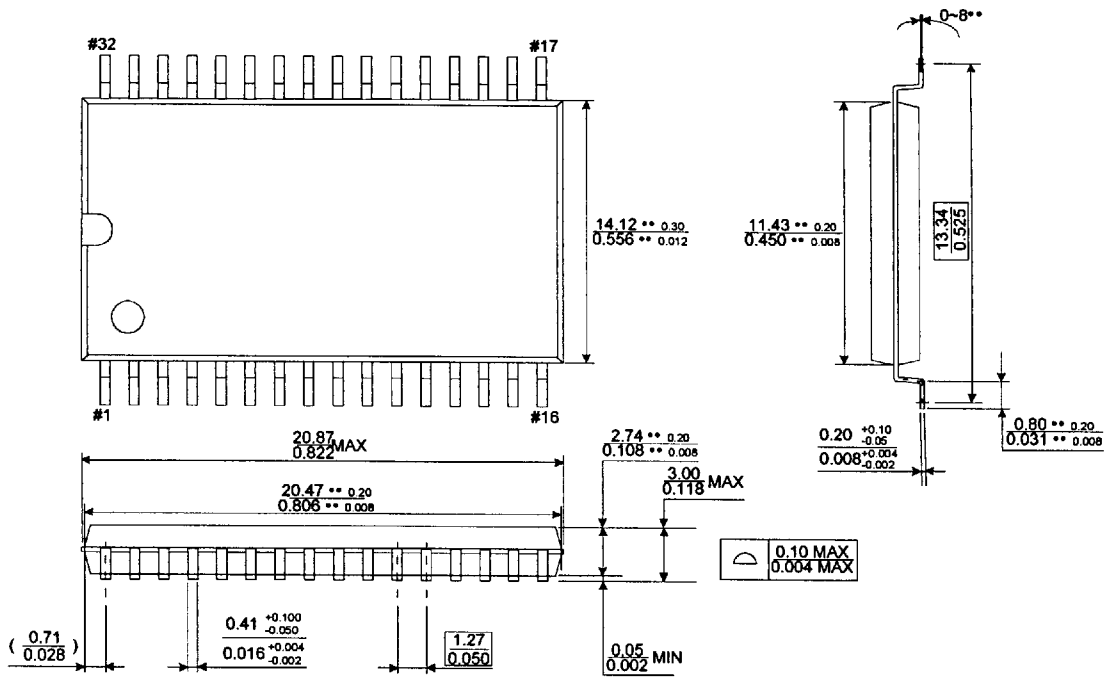
PACKAGE DIMENSIONS

Units :MillimeterS(Inches)

32 PIN DUAL INLINE PACKAGE (600mil)



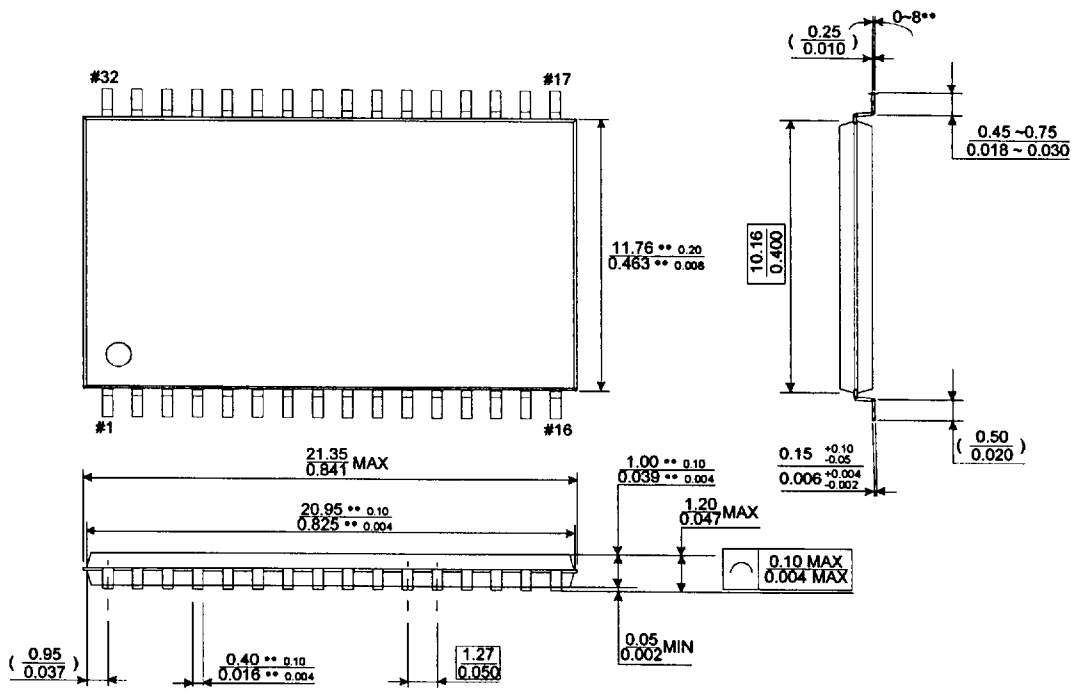
32 PIN PLASTIC SMALL OUTLINE PACKAGE (525mil)



PACKAGE DIMENSIONS

Units :MillimeterS(Inches)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)



32 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)