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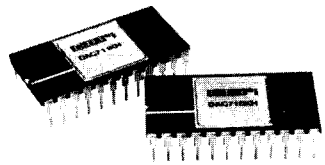


DAC710
DAC711

Monolithic 16-Bit
ROBOTICS DIGITAL-TO-ANALOG CONVERTERS

FEATURES

- DESIGNED SPECIFICALLY FOR CLOSED-LOOP SERVO-CONTROL APPLICATIONS
- MONOTONIC TO 15 BITS OVER TEMPERATURE
- MONOLITHIC CONSTRUCTION
- V_{OUT} AND I_{OUT} MODELS
- PIN-COMPATIBLE WITH DAC702, DAC703
- VERY-LOW COST FOR MULTIPLE-CHANNEL APPLICATIONS

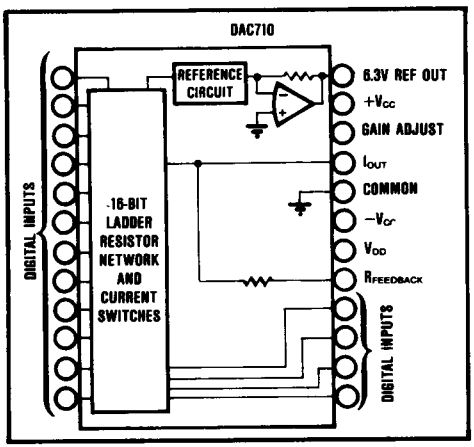
DESCRIPTION

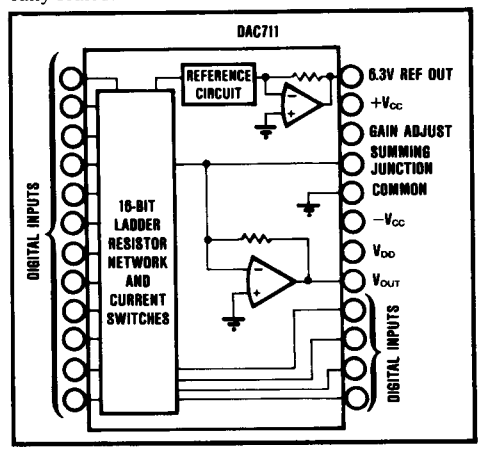
Robotics, numerical controllers, and other applications that involve the driving of servomotors require D/A converters that have very-good differential linearity around the zero output point. The DAC710KH (current output) and DAC711KH (voltage output) have been optimized for this characteristic.

DAC710 and DAC711 are complete 16-bit D/A converters on one chip. They include a precision buried-zener voltage reference, a fast settling operational amplifier (DAC711 only) as well as the D/A converter circuits. A combination of current switch design techniques accomplishes a guaranteed monotonicity of 15 bits around Bipolar Zero over the entire specification temperature range, 0°C to +70°C.

Digital inputs are complementary binary coded and are TTL-, LSTTL-, 54/74C-, and 54/74HC-compatible over the entire temperature range. Outputs are ±10V for the DAC711KH and ±1mA for the DAC710KH.

This D/A family is pin-compatible with the voltage and current output DAC703 and DAC702 model families. These D/A converters are packaged in 24-pin ceramic side-brazed packages that are hermetically sealed.





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PDS-546B

SPECIFICATIONS

ELECTRICAL

At T_A = +25°C and rated power supplies and after 10 minutes of warm-up time unless otherwise noted.

MODEL	DAC710KH/DAC711KH			UNITS
	MIN	TYP	MAX	
INPUT				
DIGITAL INPUT				
Resolution			16	Bits
Digital Inputs[1]: V_{IH}	+2.4		+V_{CC}	V
V_{IL}	−1.0		+0.8	V
I_{IH}, V_I = +2.7V			+40	µA
I_{IL}, V_I = +0.4V		−0.35	−0.5	mA
TRANSFER CHARACTERISTICS				
ACCURACY[2]				
Differential Linearity Error (near bipolar zero)[4,5]			+0.006, −0.003	% of FSR[3]
Monotonicity (near bipolar zero)[4]	15			Bits
Linearity Error			±0.0045	% of FSR
Gain Error[6]		±0.15	±0.30	%
Bipolar Zero Error[6,7]		±0.05	±0.1	% of FSR
DRIFT (over specification temperature range)				
Differential Linearity Error (near bipolar zero) over Temperature[4,5]			+0.009, −0.003	% of FSR
Monotonicity (near bipolar zero) over Temperature[4]	15			Bits
Linearity Error over Temperature			±0.009	% of FSR
Gain Drift		±25	±50	ppm/°C
Bipolar Zero Drift		±5	±12	ppm of FSR/°C
SETTLING TIME (to ±0.003% of FSR)[8]				
DAC711 (V_{OUT} Models)				
Full Scale Step (2kΩ load)		4	8	µsec
For 1LSB Step Change at Worst-Case Code[9]		2.5	4	µsec
Slew Rate		10		V/µsec
DAC710 (I_{OUT} Models)				
Full Scale Step (2mA): 10Ω to 100Ω load		350		nsec
1kΩ load		1		µsec
OUTPUT				
VOLTAGE OUTPUT				
DAC711		±10		V
Output Current	±5			mA
Output Impedance		0.15		Ω
Short Circuit to Common Duration		Indefinite		
CURRENT OUTPUT				
DAC710				
Output Range (±30% typ)		±1		mA
Output Impedance (±30% typ)		4.0		kΩ
Compliance	−2.5		+2.5	V
REFERENCE VOLTAGE				
Voltage		+6.3		V
Source Current Available for External Loads		+2.5		mA
Short Circuit to Common Duration		Indefinite		
POWER SUPPLY REQUIREMENTS				
Voltage: +V_{CC}	+13.5	+15	+16.5	V
−V_{CC}	−13.5	−15	−16.5	V
V_{DD}	+4.5	+5	+16.5	V
Current: (No Load)				
DAC711 (V_{OUT} Model): +V_{CC}		+16	+30	mA
−V_{CC}		−18	−30	mA
V_{DD}		+4	+8	mA
DAC710 (I_{OUT} Model): +V_{CC}		+10	+25	mA
−V_{CC}		−13	−25	mA
V_{DD}		+4	+8	mA
Power Dissipation (V_{DD} = +5.0V)[10]: DAC711		530	940	mW
DAC710		365	790	mW
Power Supply Rejection: +V_{CC}		±0.003	±0.006	% of FSR/%V_{CC}
−V_{CC}		±0.003	±0.006	% of FSR/%V_{CC}
V_{DD}		±0.0001	±0.001	% of FSR/%V_{DD}
TEMPERATURE RANGE				
Specification	0		+70	°C
Storage	−60		+150	°C

NOTES: (1) Digital inputs are TTL-, LSTTL-, 54/74C-, 54/74HC-, and 54/74HTC-compatible over the operating voltage range of V_{DD} = +5V to +15V and over the specified temperature range. The input switching threshold remains at the TTL threshold of 1.4V over the supply range of V_{DD} = +5V to +15V. As logic "0" and logic "1" inputs vary over 0V to +0.8V and +2.4V to +10V, respectively, the change in the D/A converter output voltage will not exceed ±0.006% of FSR. (2) DAC710KH is specified and tested with an external output operational amplifier using the internal feedback resistor in all parameters except settling time. (3) FSR means Full Scale Range and is 20V for the DAC711KH and 2mA for the DAC710KH. (4) This specification is for ±2048 consecutive codes around the bipolar zero code; that is, from $77FF_H$ to $87FF_H$. (5) ±0.003% of FSR is 1LSB for 15-bit resolution. (6) Adjustable to zero with external trim potentiometer. Adjusting the gain potentiometer rotates the transfer function around the bipolar zero point. (7) Error at input code $7FFF_H$, bipolar zero. (8) Maximum represents the 3σ limit. Not 100% tested for this parameter. (9) At the major carry, $7FFF_H$ to 8000_H and 8000_H to $7FFF_H$. (10) Power dissipation is an additional 40mW when V_{DD} is operated at +15V.

ORDERING INFORMATION

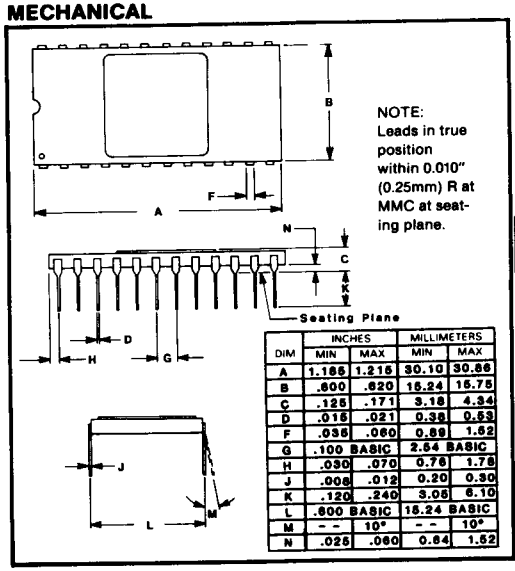
Model	Package	Temperature Range	Output
DAC710KH	Hermetic Ceramic	0°C to +70°C	Current, ±1mA
DAC711KH	Hermetic Ceramic	0°C to +70°C	Voltage
BURN-IN SCREENING OPTION See text for details.			
Model	**Package**	**Temperature Range**	**Burn-In Temp. (160h)[1]**
DAC710KH-BI	Hermetic Ceramic	0°C to +70°C	85°C
DAC711KH-BI	Hermetic Ceramic	0°C to +70°C	85°C

NOTE: (1) Or equivalent combination of time and temperature.

PIN ASSIGNMENTS

Pin No.	Function DAC710	Function DAC711
1	Bit 1 (MSB)	Bit 1 (MSB)
2	Bit 2	Bit 2
3	Bit 3	Bit 3
4	Bit 4	Bit 4
5	Bit 5	Bit 5
6	Bit 6	Bit 6
7	Bit 7	Bit 7
8	Bit 8	Bit 8
9	Bit 9	Bit 9
10	Bit 10	Bit 10
11	Bit 11	Bit 11
12	Bit 12	Bit 12
13	Bit 13	Bit 13
14	Bit 14	Bit 14
15	Bit 15	Bit 15
16	Bit 16 (LSB)	Bit 16 (LSB)
17	$R_{FEEDBACK}$	V_{OUT}
18	V_{DD}	V_{DD}
19	$-V_{CC}$	$-V_{CC}$
20	Common	Common
21	I_{OUT}	Summing Junction (Zero Adjust)
22	Gain Adjust	Gain Adjust
23	$+V_{CC}$	$+V_{CC}$
24	+6.3V Ref. Out.	+6.3V Ref. Out.

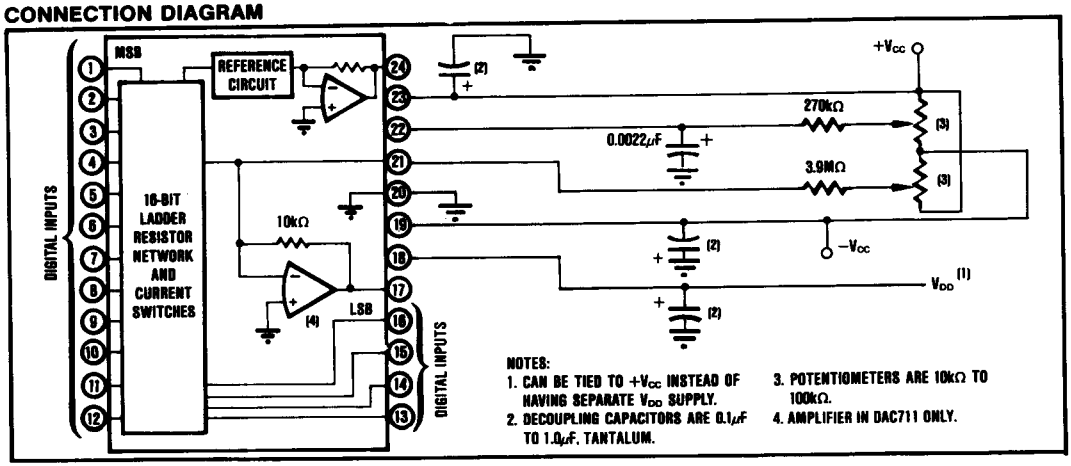
MECHANICAL



NOTE: Leads in true position within 0.010" (0.25mm) R at MMC at seating plane.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	1.185	1.215	30.10	30.86
B	.600	.620	15.24	15.75
C	.125	.171	3.18	4.34
D	.015	.021	0.38	0.53
F	.035	.060	0.89	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.05	6.10
L	.600 BASIC		15.24 BASIC	
M	- -	10°	- -	10°
N	.025	.060	0.64	1.52

CONNECTION DIAGRAM



ABSOLUTE MAXIMUM RATINGS

V_{DD} to Common	0V to +18V
$+V_{CC}$ to Common	0V to +18V
$-V_{CC}$ to Common	0V to -18V
Digital Data Inputs (pins 1-16) to Common	-1V to +18V
Reference out (pin 24) to Common	Indefinite Short to Common
External Voltage Applied to R_F (pin 21, DAC710KH)	±18V
External Voltage Applied to D/A Output (pin 17, DAC711KH)	-5V to +5V
V_{OUT} (pin 17, DAC711)	Indefinite Short to Common
Power Dissipation	1000mW
Storage Temperature	-60°C to +150°C
Lead Temperature (soldering, 10s)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

DISCUSSION OF SPECIFICATIONS

DIGITAL INPUT CODES

The DAC710/711KH accept complementary binary digital input codes in bipolar format. They may be connected by the user for either complementary offset binary (COB) or complementary two's complement (CTC) codes (see Table I).

ACCURACY

Linearity

Linearity error is the deviation of the analog output from a straight line drawn through the end points (all bits ON point and all bits OFF point).

Differential Linearity

For servomotor control applications, differential linearity error (DLE) is one of the most important performance measures of a D/A converter. DLE is the deviation from an ideal 1LSB change in the output when the input changes from one adjacent code to the next. A differential linearity error specification of +0.006% of FSR maximum means that an output step size can be between 1LSB and 3LSB (at 15 bits) when the input changes between adjacent codes. A DLE specification of −0.003% maximum ensures 15-bit monotonicity.

Monotonicity

When a D/A converter is monotonic, the analog output increases or remains the same for an increasing input digital code. For ±2048 consecutive codes around bipolar zero, the DAC710KH and DAC711KH are monotonic to 15 bits over the entire specification temperature range.

DRIFT

Gain Drift

Gain drift is a measure of the change in the full-scale range output over temperature expressed in parts-per-million per degree centigrade (ppm/°C). Gain drift is established by (1) testing the end point difference for each D/A at t_{min}, +25°C and t_{max} (2) calculating the gain error with respect to the +25°C value, and (3) dividing by the temperature change.

Zero Drift

Zero drift is a measure of the change in the output with $7FFF_H$ (bipolar zero) applied to the digital inputs. This code corresponds to 0V (DAC711KH) or 0mA (DAC710KH) at the analog output. The maximum change in offset at t_{min} or t_{max} is referenced to the zero error at +25°C and is divided by the temperature change. This drift is expressed in parts-per-million of full-scale range per degree centigrade (ppm of FSR/°C).

TABLE I. Digital Input Codes.

Digital Input Codes	Analog Output	
	Complementary Offset Binary (COB)	*Complementary Two's Complement (CTC)
0000_H	+ Full Scale	−1LSB
$7FFF_H$	Bipolar Zero	− Full Scale
8000_H	−1LSB	+ Full Scale
$FFFF_H$	− Full Scale	Bipolar Zero

*Invert the MSB of the COB code with an external inverter to obtain CTC code.

SETTLING TIME

Settling time of the D/A is the total time required for the output to settle within an error band around its final value after a change in input. Refer to Figure 1 for typical values.

Voltage Output, DAC711KH

Settling times are specified to ±0.003% of FSR for two input conditions: a full-scale range change of 20V and a ±0.006% of FSR (±1LSB in 14 bits) change at the major carry, the point at which the worst-case setting time occurs.

Current Output, DAC710KH

Settling times are specified to ±0.003% of FSR for a full-scale range change for two output load conditions: one for 10Ω to 100Ω and one for 1000Ω.

COMPLIANCE VOLTAGE

Compliance voltage applies only to current output models. It is the maximum voltage swing allowed on the output while maintaining specified accuracy.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in either the positive supply ($+V_{CC}$), negative supply ($-V_{CC}$) or logic supply (V_{DD}) about the nominal power supply voltages (see Figure 2).

REFERENCE SUPPLY

All models have an internal +6.3V reference voltage derived from an on-chip buried-zener diode. This reference voltage, available at pin 24, has a tolerance of ±5%. A minimum of 1.5mA is available for external loads. Gain and Zero adjustments should be made under constant load conditions.

If a varying load is to be driven by the reference supply, an external buffer amplifier is recommended to drive the load in order to isolate the bipolar offset (connected internally to the reference) from load variations.

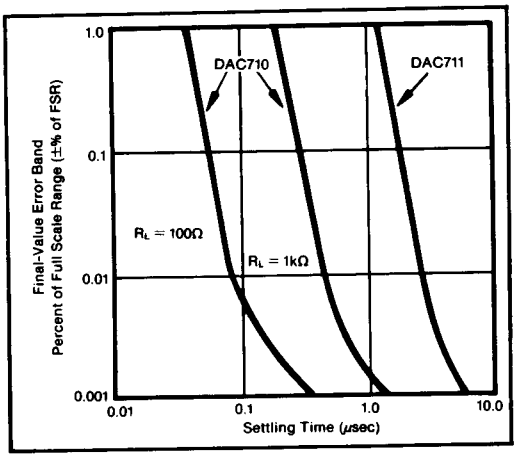


FIGURE 1. Final-Value Error Band Versus Full-Scale Range Settling Time.

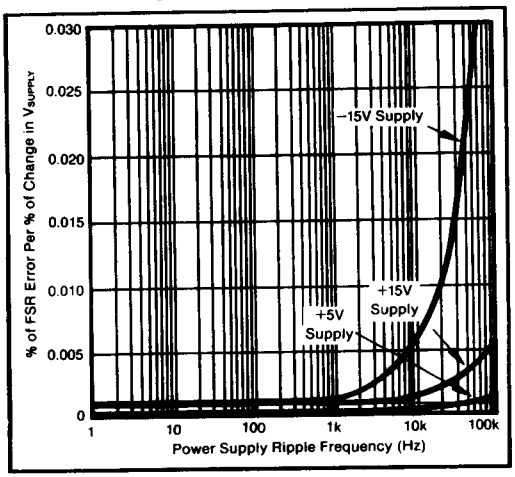


FIGURE 2. Power Supply Rejection Versus Power Supply Ripple Frequency.

OPERATING INSTRUCTIONS

POWER SUPPLY CONNECTIONS

For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagram. The 1μF tantalum capacitors should be located close to the D/A converter.

EXTERNAL ZERO AND GAIN ADJUSTMENT

Zero and gain may be trimmed by installing external zero and gain potentiometers. Connect these potentiometers as shown in the Connection Diagram and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 270kΩ resistors (±20% carbon or better) should be located close to the D/A converter to prevent noise pickup. If it is not convenient to use these high-value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in place of the 3.9MΩ part. A 0.001μF to 0.01μF ceramic capacitor should be connected (even if GAIN ADJUST is not used) from GAIN ADJUST (pin 22) to COMMON to prevent noise pickup. Refer to Figure 4 for the relationship of zero and gain adjustments.

Zero Adjustment

Apply the digital input code ($7FFF_H$) that produces zero output voltage or current. See Table II for corresponding codes and the Connection Diagram for zero adjustment circuit connections. Zero calibration should be made before Gain calibration.

Gain Adjustment

Apply the digital input code (0000_H) that gives the maximum positive output voltage or current. Adjust the gain potentiometer for this positive full-scale voltage or current. See Table II for positive full-scale values and the Connection Diagram for gain adjustment circuit connections.

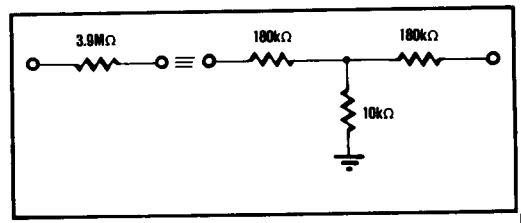


FIGURE 3. Equivalent Resistances.

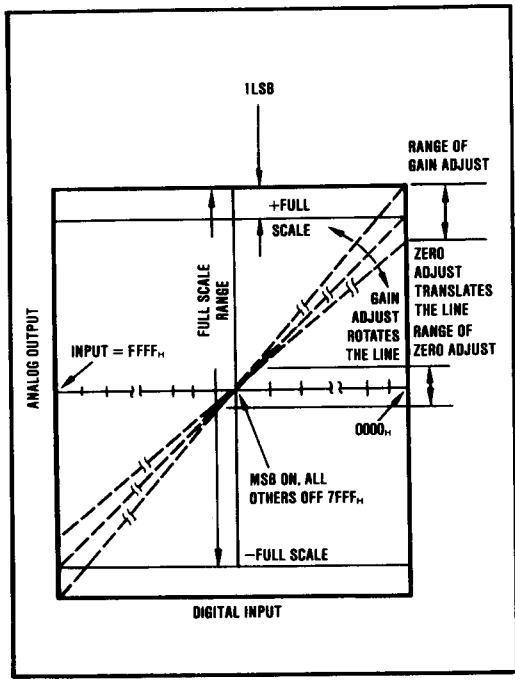


FIGURE 4. Relationship of Zero and Gain Adjustments.

TABLE II. Digital Input and Analog Output Relationships.

Digital Input Code	Analog Output							
	DAC710 Current Output				DAC711 Voltage Output			
	16-bit	15-bit	14-bit	Units	16-bit	15-bit	14-bit	Units
1LSB	0.031	0.061	0.122	μA	305	610	1224	μV
0000_H	−0.99997	−0.99994	−0.99988	mA	+9.99960	+9.99939	+9.99878	V
$7FFF_H$	0.00000	0.00000	0.00000	mA	0.00000	0.00000	0.00000	V
$FFFF_H$	+1.00000	+1.00000	+1.00000	mA	−10.0000	−10.0000	−10.0000	V

INSTALLATION CONSIDERATIONS

Due to the extremely high resolution and linearity of the D/A converter, system design problems such as grounding and contact resistance become very important. For a 16-bit converter with a +10V full-scale range, 1LSB is 153μV. With a load current of 5mA, series wiring and connector resistance of only 30mΩ will cause the output to be in error by 1LSB. To understand what this means in terms of a system layout, the resistance of #23 wire is about 0.021Ω/ft. Ignoring contact resistance, less than six inches of wire will produce a 1LSB error in the analog output voltage!

In Figures 5, 6, and 7, lead and contact resistances are represented by R_1 through R_5. As long as the load resistance (R_L) is constant, R_2 simply introduces a gain error and can be removed during initial calibration. R_3 is part of R_L, if the output voltage is sensed at COMMON (pin 20), and therefore introduces no error. If R_L is variable, then R_2 should be less than $R_{Lmin}/2^{16}$ to reduce voltage drops due to wiring to less than 1LSB. For example, if R_{Lmin} is 5kΩ, then R_2 should be less than 0.08Ω. R_L should be located as close as possible to the D/A converter for optimum performance. The effect of R_4 is negligible.

In many applications it is impractical to sense the output voltage at pin 20. Sensing the output voltage at the system ground point is permissible with the DAC710/711 because the D/A converter is designed to have a constant return current of approximatley 2mA flowing from pin 20. The variation in this current is under 20μA (with changing input codes), therefore R_4 can be as large as 3Ω without adversely affecting the linearity of the D/A converter. The voltage drop across R_4 ($R_4 \times 2mA$) appears as a zero error and can be removed with the zero calibration adjustment. This alternate sensing point (the system ground point) is shown in Figures 5, 6, and 7.

Figures 6 and 7 show two methods of connecting the current output model (DAC710KH) with external precision output operational amplifiers. By sensing the output voltage at the load resistor (i.e., by connecting R_F to the output of A_1 at R_L), the effect of R_1 and R_2 is greatly reduced. R_1 will cause a gain error but is independent of the value of R_L and can be eliminated by initial calibration adjustments. The effect of R_2 is negligible because it is inside the feedback loop of the output op amp and is therefore greatly reduced by the loop gain. If the output cannot be sensed at COMMON (pin 20), or the system ground point as mentioned above, then the differential output circuit shown in Figure 7 is recommended. In this circuit the output voltage is sensed at the load common and not at the D/A converter common as in the previous circuits. The value of R_6 and R_7 must be adjusted for maximum common-mode rejection at R_L. Note that if R_3 is negligible, the circuit of Figure 7 can be reduced to the one shown in Figure 6. Again, the effect of R_4 is negligible.

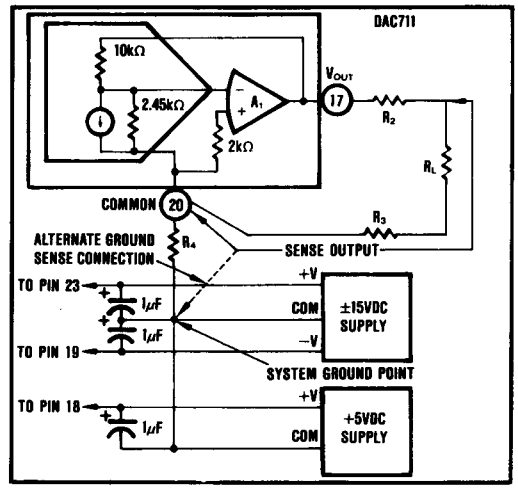


FIGURE 5. Output Circuit for DAC711.

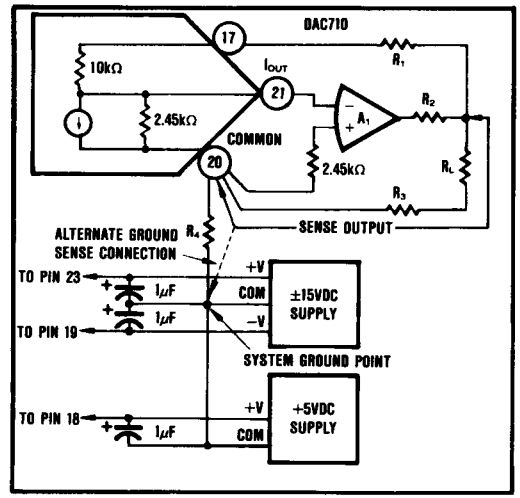


FIGURE 6. Preferred External Op Amp Configuration for DAC710.

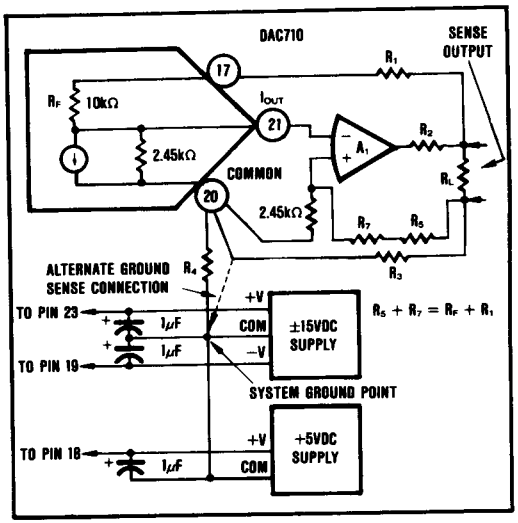


FIGURE 7. Differential Sensing Output Op Amp Configuration for DAC710.

The D/A converter and the wiring to its connectors should be located to provide optimum isolation from sources of RFI and EMI. The key concept in elimination of RF radiation pickup is small loop area. If a signal lead and its return conductor are wired close together, they present a small flux-capture cross section for external fields.

APPLICATIONS

DRIVING AN EXTERNAL OP AMP WITH CURRENT OUTPUT D/A'S

DAC710KH is a current output device and will drive the summing junction of an op amp to produce an output voltage as shown in Figure 8. Use of the internal feedback resistor (pin 17) is required to obtain specified gain accuracy and low gain drift.

DAC710KH can be scaled for any desired voltage range with an external feedback resistor at the expense of increased drift with temperature. The resistors in the DAC710KH ratio track to ±1ppm/°C but their absolute TCR may be as high as ±50ppm/°C.

An alternative method of scaling the output voltage of the D/A converter and preserving the low gain drift is shown in Figure 9.

OUTPUTS LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use an I_{OUT} value of ±1mA to calculate the output voltage range (see Figure 10). Use protection diodes as shown when a high voltage op amp is used.

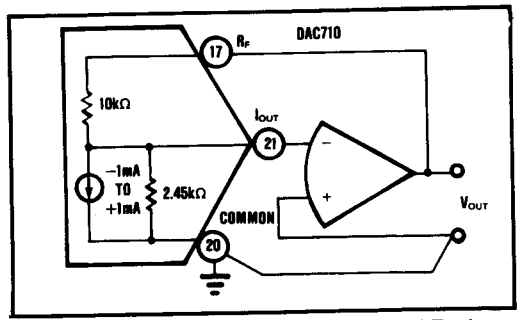


FIGURE 8. External Op Amp Using Internal Feedback Resistors (DAC710).

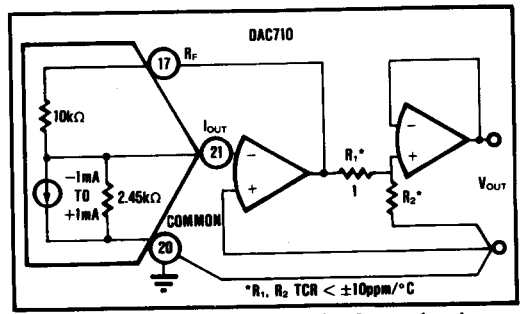


FIGURE 9. External Op Amp Using Internal and External Feedback Resistors to Maintain Low Gain Drift (DAC710).

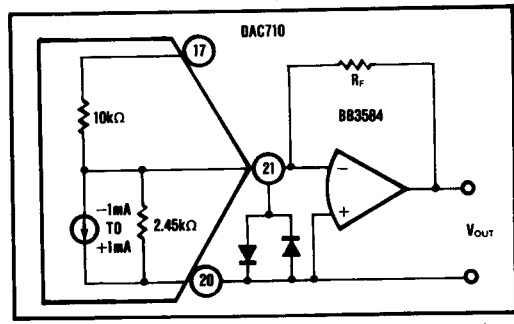


FIGURE 10. External Op Amp Using External Feedback Resistors (DAC710).

BURN-IN SCREENING

Burn-in screening is an option available for the entire DAC711 family of products. Burn-in duration is 160 hours at 85°C (or equivalent combination of time and temperature).

All units are tested after burn-in to ensure that grade specifications are met. To order burn-in, add "-BI" to the base model number.