

**512K x 8 Static RAM**

**Features**

- **High speed**
  - $t_{AA} = 12 \text{ ns}$
- **Low active power**
  - 504 mW (max.)
- **Low CMOS standby power (Commercial L version)**
  - 1.8 mW (max.)
- **2.0V Data Retention (660  $\mu\text{W}$  at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features**

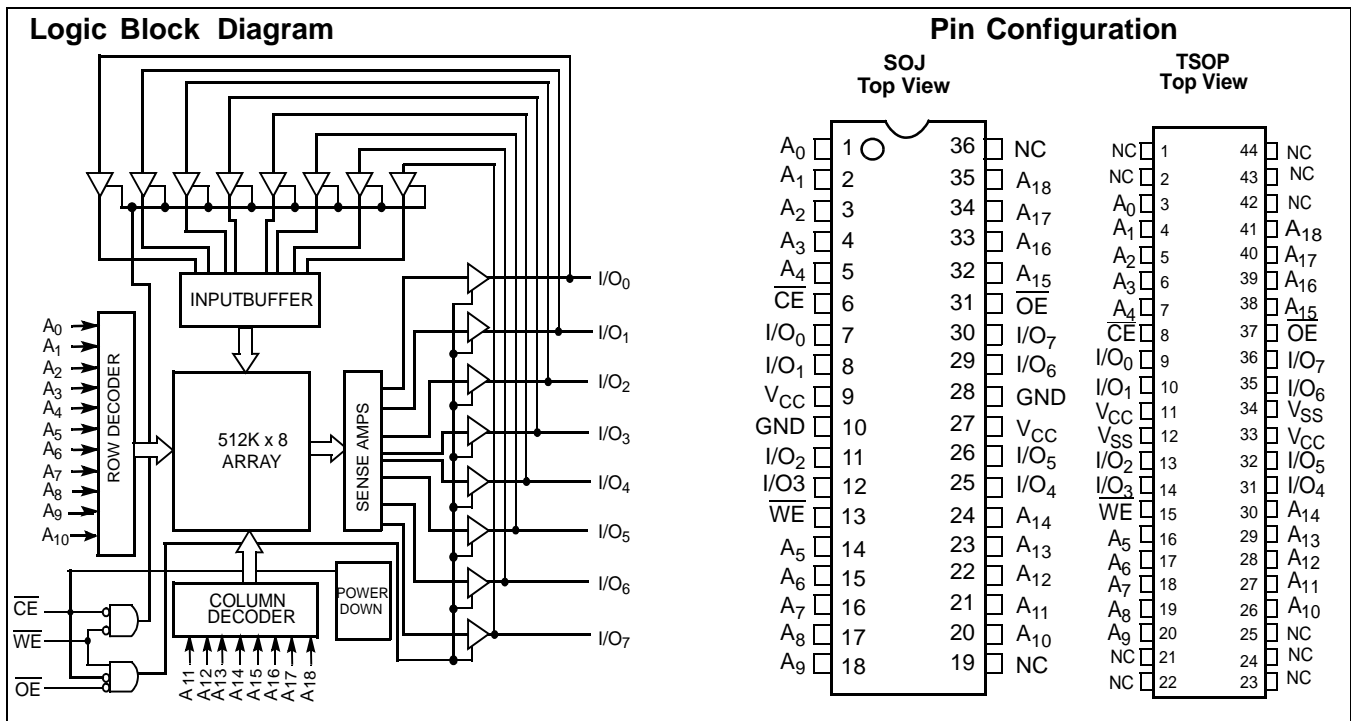
**Functional Description<sup>[1]</sup>**

The CY7C1049BNV33 is a high-performance CMOS Static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ( $\overline{\text{CE}}$ ), an active LOW Output Enable ( $\overline{\text{OE}}$ ), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Write Enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the eight I/O pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) is then written into the location specified on the address pins ( $\text{A}_0$  through  $\text{A}_{18}$ ).

Reading from the device is accomplished by taking Chip Enable ( $\overline{\text{CE}}$ ) and Output Enable ( $\overline{\text{OE}}$ ) LOW while forcing Write Enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins ( $\text{I/O}_0$  through  $\text{I/O}_7$ ) are placed in a high-impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW, and  $\overline{\text{WE}}$  LOW).

The CY7C1049BNV33 is available in a standard 400-mil-wide 36-pin SOJ and 44-pin TSOPII packages with center power and ground (revolutionary) pinout.



**Selection Guide**

			-12	-15	-20
Maximum Access Time (ns)			12	15	20
Maximum Operating Current (mA)	Com'l		200	180	160
	Ind'l		220	200	170
Maximum CMOS Standby Current (mA)	Com'l/Ind'l		8	8	8
	Com'l	L	0.5	0.5	0.5

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to +150°C

Ambient Temperature with Power Applied ..... -55°C to +125°C

Supply Voltage on  $V_{CC}$  to Relative GND<sup>[2]</sup> ..... -0.5V to +4.6V

DC Voltage Applied to Outputs<sup>[2]</sup> in High Z State ..... -0.5V to  $V_{CC} + 0.5V$

DC Input Voltage<sup>[2]</sup> ..... -0.5V to  $V_{CC} + 0.5V$

Current into Outputs (LOW) ..... 20 mA

**Operating Range**

Range	Ambient Temperature	$V_{CC}$
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	-40°C to +85°C	

**DC Electrical Characteristics** Over the Operating Range

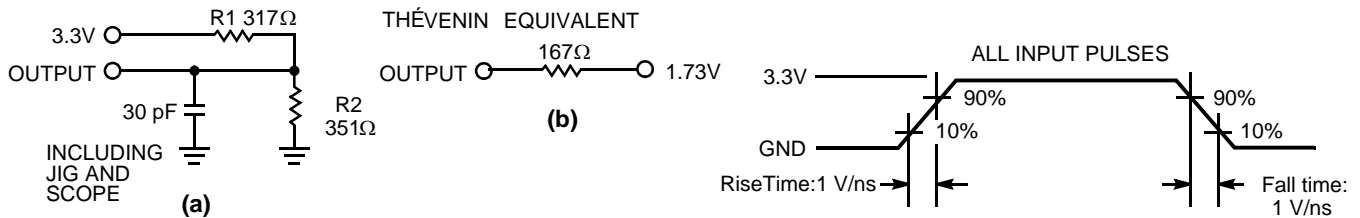
Parameter	Description	Test Conditions	-12		-15		-20		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ , $I_{OH} = -4.0 \text{ mA}$	2.4		2.4		2.4		V	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ , $I_{OL} = 8.0 \text{ mA}$		0.4		0.4		0.4	V	
$V_{IH}$	Input HIGH Voltage		2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	2.2	$V_{CC} + 0.5$	V	
$V_{IL}$	Input LOW Voltage <sup>[2]</sup>		-0.5	0.8	-0.5	0.8	-0.5	0.8	V	
$I_{IX}$	Input Leakage Current	$GND \leq V_I \leq V_{CC}$	-1	+1	-1	+1	-1	+1	µA	
$I_{OZ}$	Output Leakage Current	$GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled	-1	+1	-1	+1	-1	+1	µA	
$I_{CC}$	$V_{CC}$ Operating Supply Current	$V_{CC} = \text{Max.}$ , $f = f_{MAX} = 1/t_{RC}$	Com'l			200		180		mA
			Ind'l			220		200		170
$I_{SB1}$	Automatic CE Power-Down Current —TTL Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{IH}$ $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$		30		30		30	mA	
$I_{SB2}$	Automatic CE Power-Down Current —CMOS Inputs	Max. $V_{CC}$ , $\overline{CE} \geq V_{CC} - 0.3V$ , $V_{IN} \geq V_{CC} - 0.3V$ , or $V_{IN} \leq 0.3V$ , $f = 0$	Com'l/Ind'l			8		8		mA
			Com'l	L		0.5		0.5		0.5

**Capacitance<sup>[3]</sup>**

Parameter	Description	Test Conditions	Max.	Unit
$C_{IN}$	Input Capacitance	$T_A = 25^\circ\text{C}$ , $f = 1 \text{ MHz}$ , $V_{CC} = 3.3V$	8	pF
$C_{OUT}$	I/O Capacitance		8	pF

**Notes:**

- For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at [www.cypress.com](http://www.cypress.com).
- $V_{IL}$  (min.) = -2.0V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

**AC Test Loads and Waveforms**

**AC Switching Characteristics<sup>[4]</sup> Over the Operating Range**

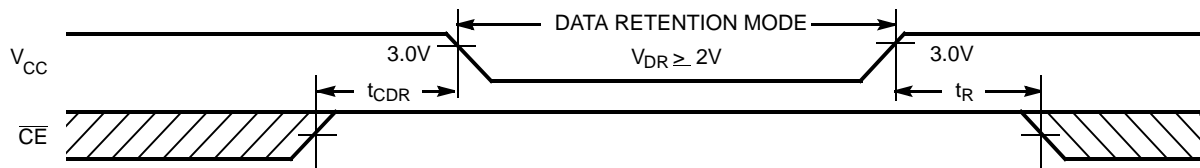
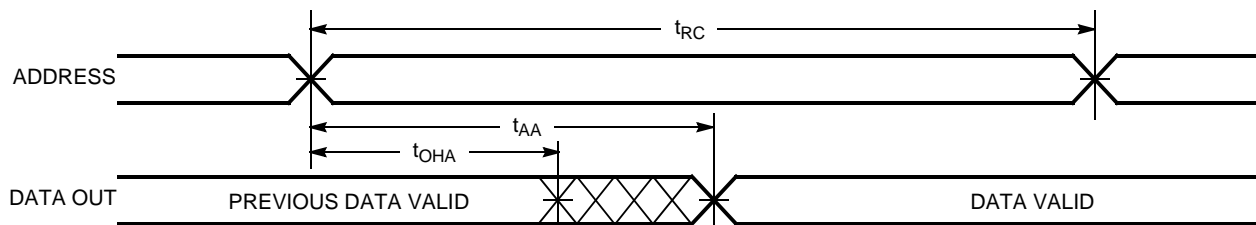
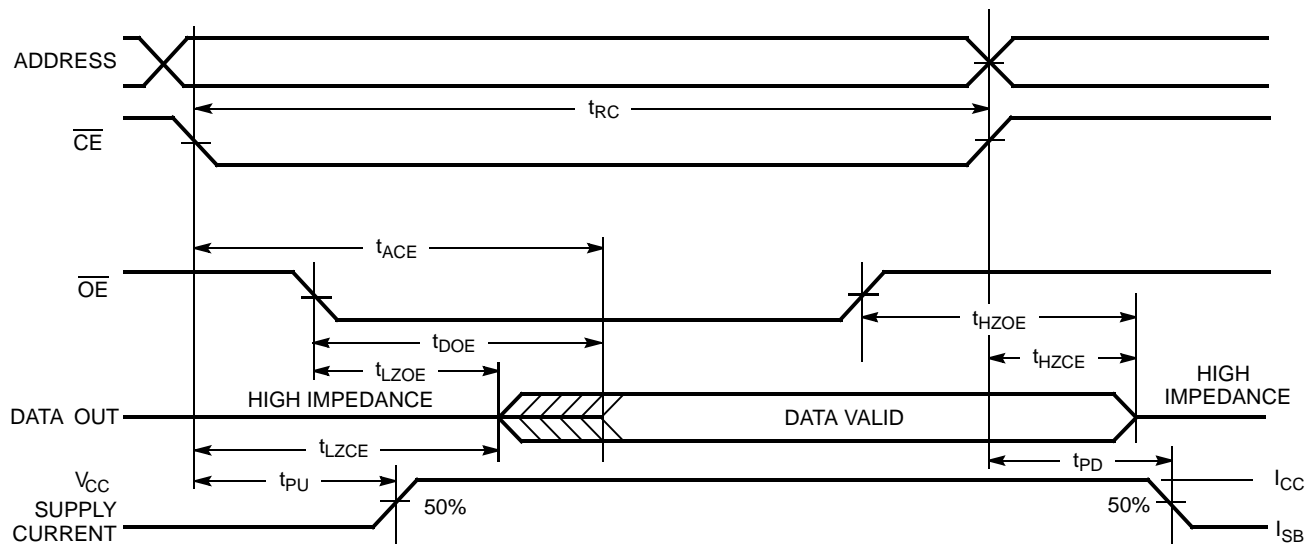
Parameter	Description	-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
<b>Read Cycle</b>								
$t_{power}$	$V_{CC}$ (typical) to the First Access <sup>[5]</sup>	1		1		1		$\mu s$
$t_{RC}$	Read Cycle Time	12		15		20		ns
$t_{AA}$	Address to Data Valid		12		15		20	ns
$t_{OHA}$	Data Hold from Address Change	3		3		3		ns
$t_{ACE}$	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		6		7		8	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z	0		0		0		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		8	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[6, 7]</sup>		6		7		8	ns
$t_{PU}$	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
$t_{PD}$	$\overline{CE}$ HIGH to Power-Down		12		15		20	ns
<b>Write Cycle<sup>[8, 9]</sup></b>								
$t_{WC}$	Write Cycle Time	12		15		20		ns
$t_{SCE}$	$\overline{CE}$ LOW to Write End	10		12		13		ns
$t_{AW}$	Address Set-Up to Write End	10		12		13		ns
$t_{HA}$	Address Hold from Write End	0		0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	10		12		13		ns
$t_{SD}$	Data Set-Up to Write End	7		8		9		ns
$t_{HD}$	Data Hold from Write End	0		0		0		ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low Z <sup>[7]</sup>	3		3		3		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High Z <sup>[6, 7]</sup>		6		7		8	ns

**Notes:**

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally.  $T_{power}$  time has to be provided initially before a read/write operation is started.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured  $\pm 500$  mV from steady-state voltage.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW, and  $\overline{WE}$  LOW.  $\overline{CE}$  and  $\overline{WE}$  must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- No input may exceed  $V_{CC} + 0.5V$
- $t_r \leq 3$  ns for the -12 and -15 speeds.  $t_r \leq 5$  ns for the -20 ns and slower speeds.

**Data Retention Characteristics** Over the Operating Range (For L version only)

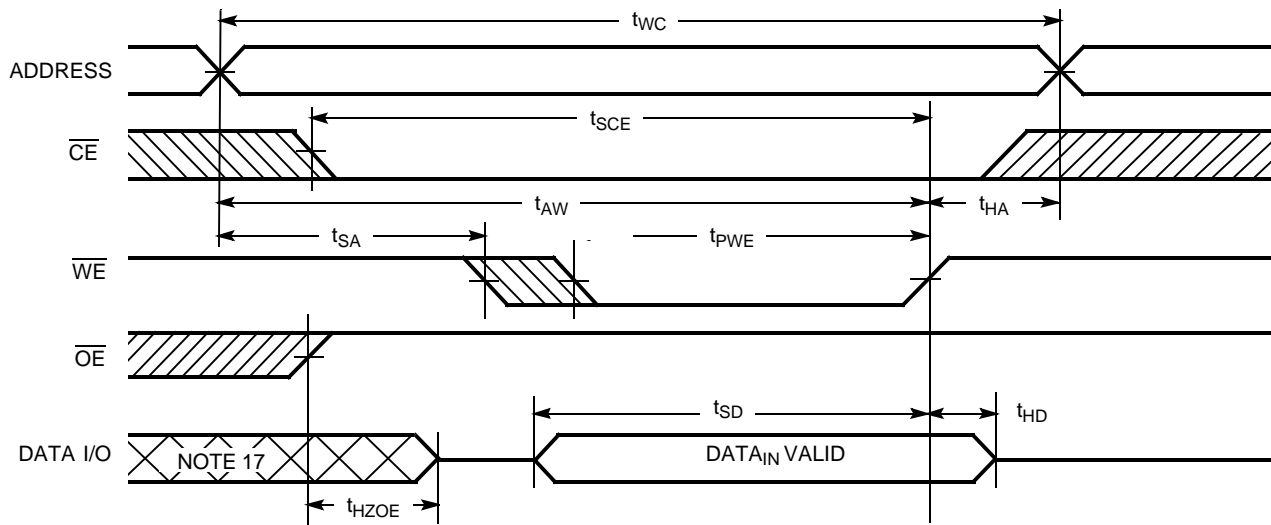
Parameter	Description	Conditions <sup>[10]</sup>	Min.	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2.0		V
$I_{CCDR}$	Data Retention Current	$V_{CC} = V_{DR} = 2.0V$ , $CE \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		330	$\mu A$
$t_{CDR}^{[3]}$	Chip Deselect to Data Retention Time		0		ns
$t_R^{[11]}$	Operation Recovery Time		$t_{RC}$		ns

**Data Retention Waveform**

**Switching Waveforms**
**Read Cycle No. 1<sup>[12, 13]</sup>**

**Read Cycle No. 2 ( $\overline{OE}$  Controlled)<sup>[13, 14]</sup>**

**Notes:**

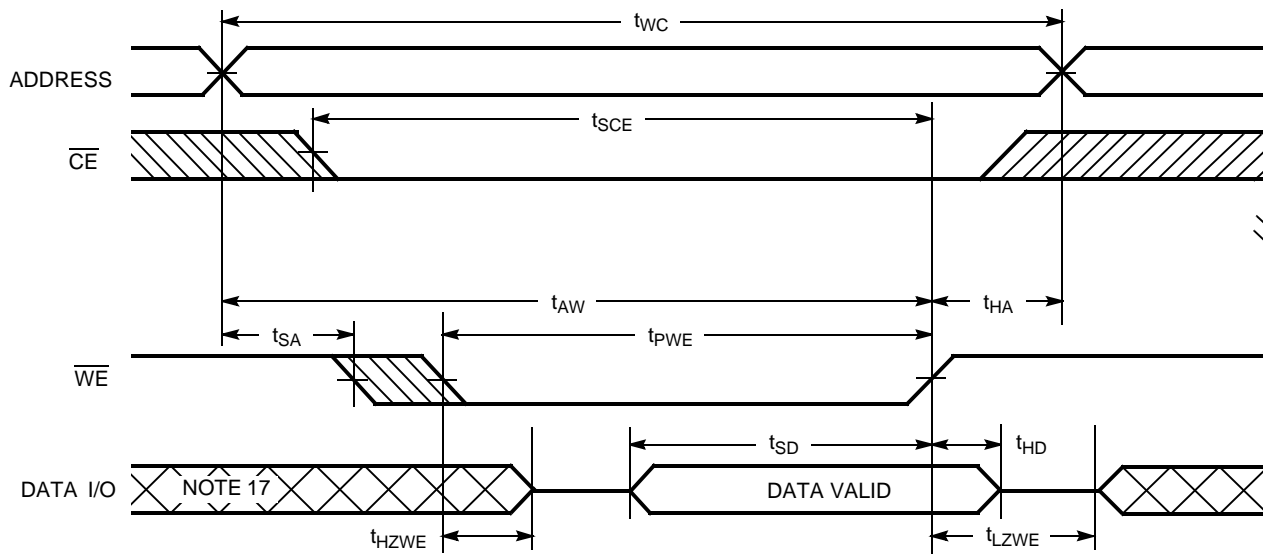
12. Device is continuously selected.  $\overline{OE}$ ,  $\overline{CE} = V_{IL}$ .
13. WE is HIGH for read cycle.
14. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ( $\overline{WE}$  Controlled,  $\overline{OE}$  HIGH During Write)<sup>[15, 16]</sup>



Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)<sup>[16]</sup>



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O <sub>0</sub> - I/O <sub>7</sub>	Mode	Power
H	X	X	High Z	Power-Down	Standby (I <sub>SB</sub> )
L	L	H	Data Out	Read	Active (I <sub>CC</sub> )
L	X	L	Data In	Write	Active (I <sub>CC</sub> )
L	H	H	High Z	Selected, Outputs Disabled	Active (I <sub>CC</sub> )

Notes:

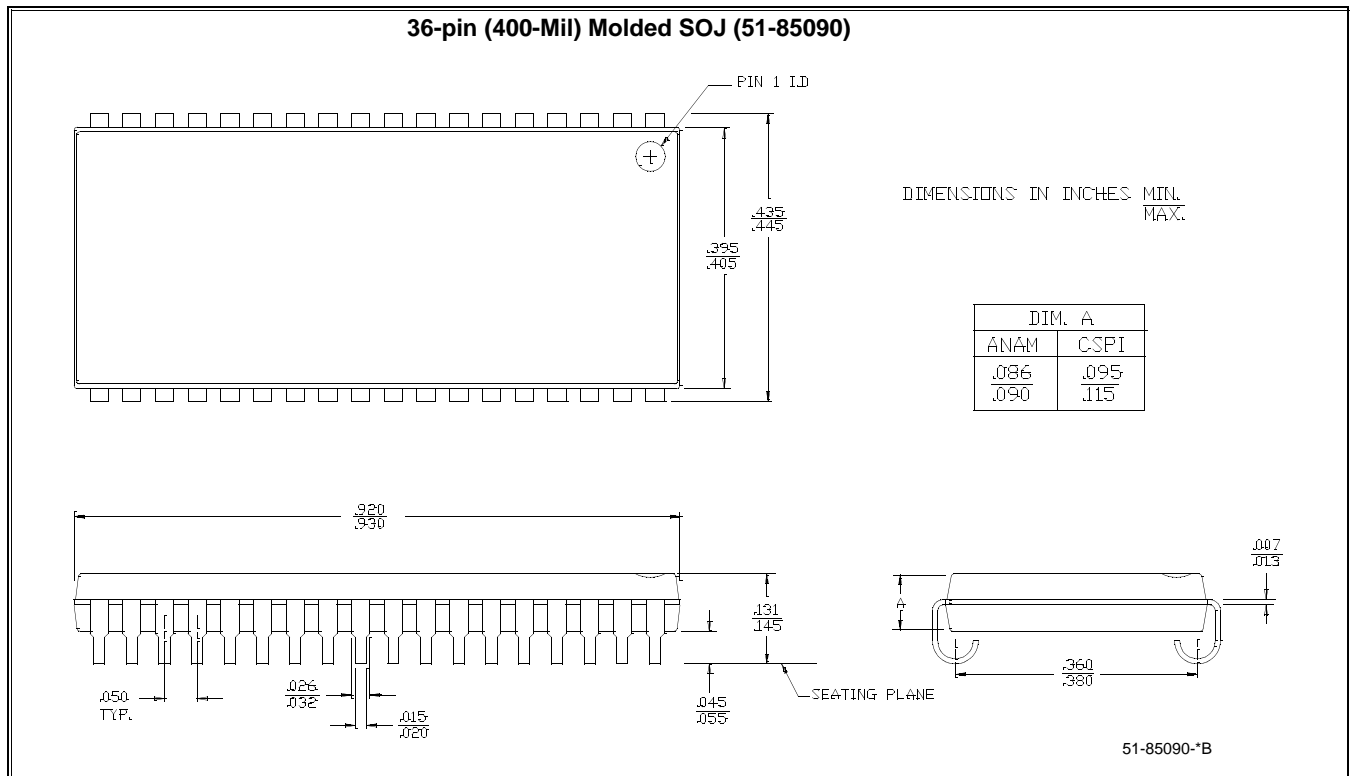
- 15. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
- 16. If  $\overline{CE}$  goes HIGH simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
- 17. During this period the I/Os are in the output state and input signals should not be applied.

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1049BNV33-12ZC	51-85087	44-Pin TSOP II Z44	Commercial
	CY7C1049BNV33-12VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BNV33-12VI	51-85090	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BNV33-12VXI	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
15	CY7C1049BNV33-15VC	51-85090	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BNV33-15VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BNV33L-15VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BNV33-15ZC	51-85087	44-Pin TSOP II Z44	
	CY7C1049BNV33-15VI	51-85090	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BNV33-15VXI	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BNV33-15ZI	51-85087	44-Pin TSOP II Z44	
20	CY7C1049BNV33-20VC	51-85090	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BNV33-20VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BNV33-20VXI	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	Industrial

Please contact local sales representative regarding availability of these parts

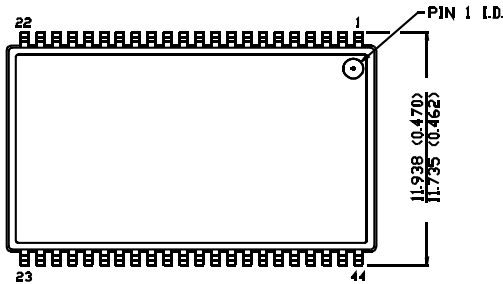
**Package Diagrams**



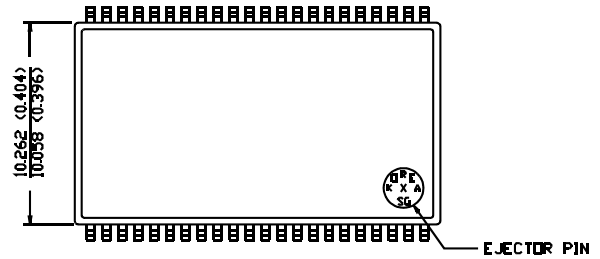
Package Diagrams (continued)

44-Pin TSOP II Z44 (51-85087)

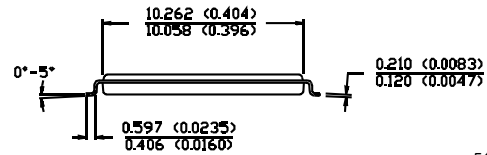
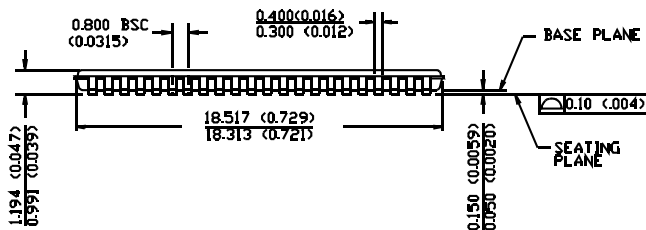
DIMENSION IN MM (INCH)  
MAX  
RTT



TOP VIEW



BOTTOM VIEW



51-85087-A

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**Document History Page**

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<b>REV.</b>	<b>ECN NO.</b>	<b>Issue Date</b>	<b>Orig. of Change</b>	<b>Description of Change</b>
**	423847	See ECN	NXR	New Data Sheet