MILITARY SRAM

256K x 4 SRAM

AVAILABLE AS MILITARY SPECIFICATIONS

- MIL-STD-883, Class B
- Radiation tolerant (consult factory)

FEATURES

- High speed: 20, 25, 35 and 45ns
- Battery Backup: 2V data retention
- Low power standby
- Power down (gated inputs)
- High-performance, low-power, CMOS double-metal process
- Single +5V (±10%) power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

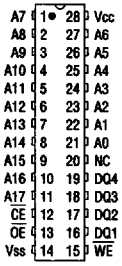
OPTIONS

	MARKING
• Timing	
20ns access	-20
25ns access	-25
35ns access	-35
45ns access	-45
55ns access	-55*
70ns access	-70*
• Packages	
Ceramic DIP (400 mil)	C
Ceramic Flat Pack	F
Ceramic LCC	EC
Ceramic SOJ	DCJ
• 2V data retention, low power standby	L
• Power down (gated inputs)	P

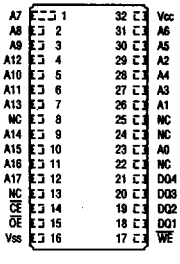
*Electrical characteristics identical to those provided for the 45ns access devices.

PIN ASSIGNMENT (Top View)

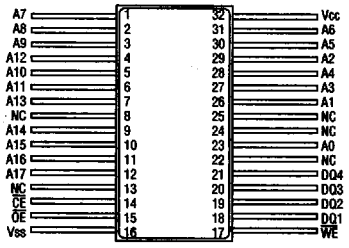
28-Pin DIP



32-Pin LCC
32-Pin SOJ



32-Pin Flat Pack



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology. Micron SRAMs are manufactured and quality controlled in the USA at our modern Boise, Idaho, facility.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) capability. These enhancements can place the outputs in High-Z for additional flexibility in system design. Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH while $\overline{CE}$ and $\overline{OE}$ go LOW. The devices offer a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

The "L" version provides an approximate 50 percent reduction in CMOS standby current (I_{SBC2}) over the standard version. The "P" version provides an approximate 80 percent reduction in TTL standby current (I_{SBT1}). This is achieved by including gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines. The gated inputs also facilitate the design of battery-backed systems where the designer needs to protect against inadvertent battery-current drain during power-down, when inputs may be at undefined levels.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

FAST SRAM

FUNCTIONAL BLOCK DIAGRAM

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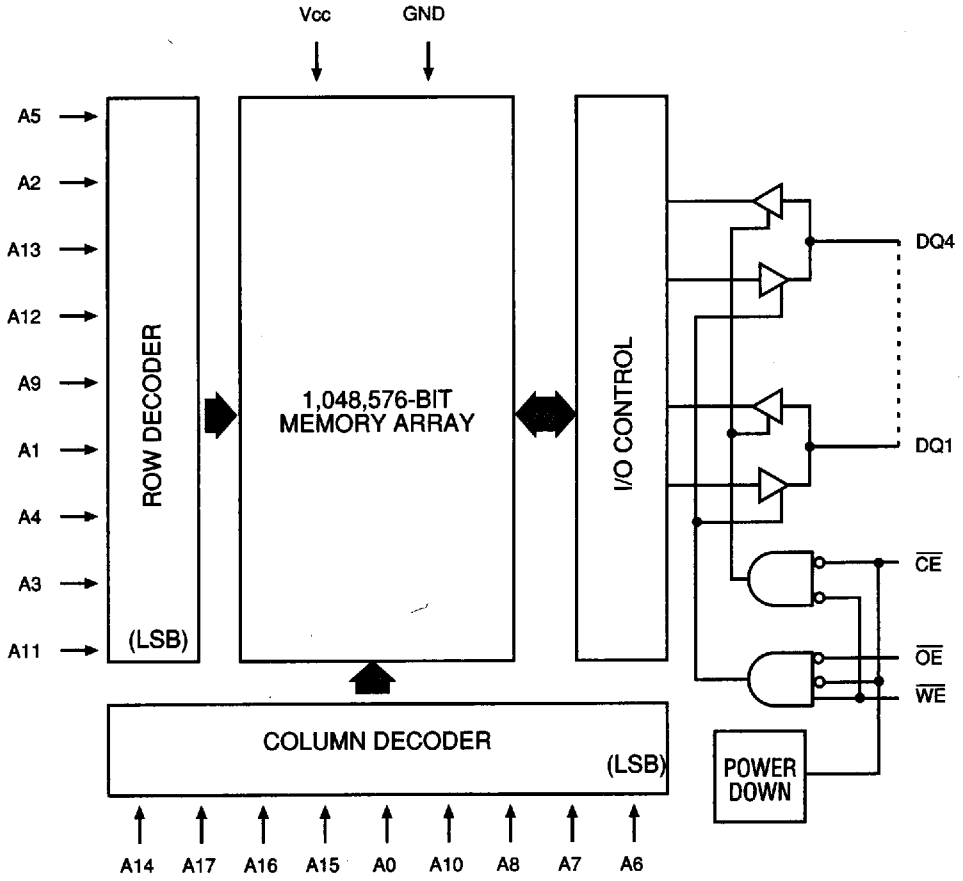

NOTE: The two least significant row address bits (A11 and A3) are encoded using gray code.

TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Input or DQ Relative to Vss ....-2V to +7V
Voltage on Vcc Supply Relative to Vss .....-1V to +7V
Storage Temperature .....-65°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA
Lead Temperature (soldering 10 seconds) .....+260°C
Junction Temperature .....+175°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55°C \le T_C \le 125°C$; $V_{CC} = 5.0V \pm 10\%$)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	Vcc+1.0	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	$0V \le V_{IN} \le V_{CC}$	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled $0V \le V_{OUT} \le V_{CC}$	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MAX -20	MAX -25	MAX -35	MAX -45	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE} \le V_{IL}$; V_{CC} = MAX f = MAX = 1/ ^tRC (MIN) Outputs Open	I_{CC}	155	140	125	115	mA	3
Power Supply Current: Standby	$\overline{CE} \ge V_{IH}$; V_{CC} = MAX f = MAX = 1/ ^tRC (MIN) Outputs Open	I_{SBT1}	40	35	32	30	mA	
	"P" Version Only	I_{SBT1}	10	10	10	10	mA	
	$\overline{CE} \ge V_{IH}$, All Other Inputs $\le V_{IL}$ or $\ge V_{IH}$, V_{CC} = MAX f = 0 Hz	I_{SBT2}	25	25	25	25	mA	
	"P" Version Only	I_{SBT2}	10	10	10	10	mA	
	$\overline{CE} \ge V_{CC}$ -0.2V; V_{CC} = MAX $V_{IL} \le V_{SS}$ +0.2V $V_{IH} \ge V_{CC}$ -0.2V; f = 0 Hz	I_{SBC2}	10	10	10	10	mA	
	"L" Version Only	I_{SBC2}	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance (A0-A2, A12-A15)	T_A = 25°C, f = 1MHz	C_I		10	pF	4
Output Capacitance (DQ1-DQ4)	V_{CC} = 5V	C_O		8	pF	4
Input Capacitance (All Other Inputs)		C_I		8	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (-55°C ≤ T_C ≤ 125°C; Vcc = 5V ± 10%)

DESCRIPTION		-20		-25		-35		-45			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
READ Cycle											
READ cycle time	^tRC	20		25		35		45		ns	
Address access time	^tAA		20		25		35		45	ns	
Chip Enable access time	^tACE		20		25		35		45	ns	
Output hold from address change	^tOH	3		3		3		3		ns	
Chip Enable to output in Low-Z	^tLZCE	5		5		5		5		ns	7
Chip disable to output in High-Z	^tHZCE		8		10		15		18	ns	6, 7
Chip Enable to power-up time	^tPU	0		0		0		0		ns	
Chip disable to power-down time	^tPD		20		25		35		45	ns	
Output Enable access time	^tAOE		7		8		12		15	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	
Output disable to output in High-Z	^tHZOE		7		9		12		15	ns	6
WRITE Cycle											
WRITE cycle time	^tWC	20		25		35		45		ns	
Chip Enable to end of write	^tCW	15		16		20		25		ns	
Address valid to end of write	^tAW	15		16		20		25		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	^tWP	15		16		20		25		ns	
Data setup time	^tDS	8		10		13		15		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	4		4		4		4		ns	7
Write Enable to output in High-Z	^tHZWE	0	9	0	10	0	13	0	15	ns	6, 7

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AC TEST CONDITIONS

Input pulse levels	Vss to 3V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

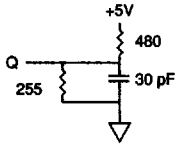


Fig. 1 OUTPUT LOAD EQUIVALENT

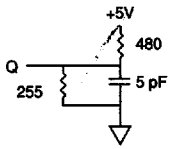


Fig. 2 OUTPUT LOAD EQUIVALENT

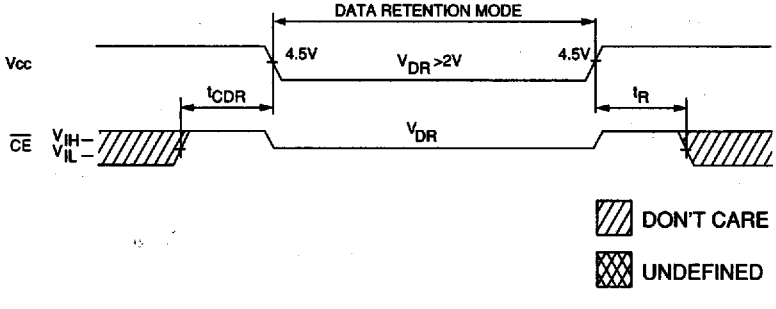
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates. The specified value applies with the outputs unloaded, and $f = \frac{1}{{}^tRC\ (MIN)}$ Hz
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ${}^tHZCE$, ${}^tHZOE$ and ${}^tHZWE$ are specified with CL = 5 pF as in Fig. 2. Transition is measured ± 500mV typical from steady state voltage, allowing for actual tester RC time constant.
7. At any given temperature and voltage condition, ${}^tHZCE$ is less than ${}^tLZCE$ and ${}^tHZWE$ is less than ${}^tLZWE$.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. Chip enable and output enable are held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ${}^tRC$ = READ cycle time.
12. Chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) can initiate and terminate a WRITE cycle.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data			V_{DR}	2		—	V	
Data Retention Current	$\overline{CE}$ ≥ (Vcc - 0.2V) V_{IN} ≥ (Vcc - 0.2V) or ≤ 0.2V	Vcc = 2V	I_{CCDR}			1.0	mA	
		Vcc = 3V				1.5	mA	
Chip Deselect to Data Retention Time			${}^tCDR$	0		—	ns	4
Operation Recovery Time			${}^tR$	${}^tRC$			ns	4, 11

LOW Vcc DATA RETENTION WAVEFORM



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READ CYCLE NO. 1 [8, 9]

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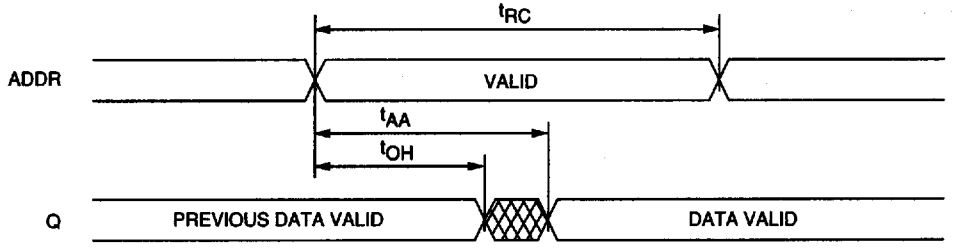
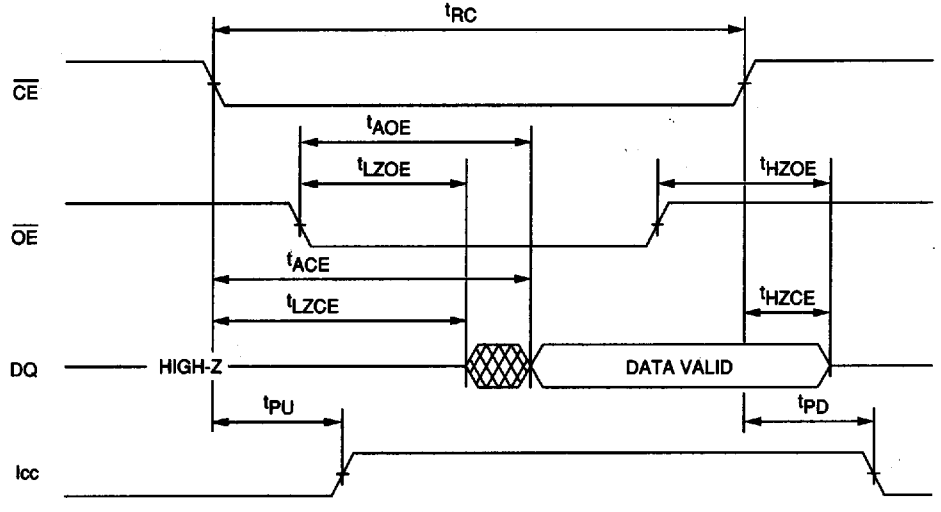


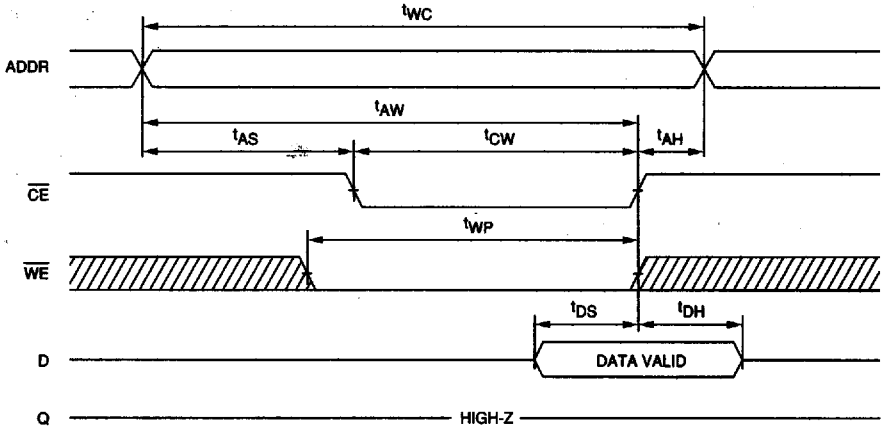
READ CYCLE NO. 2 [7, 8, 10]



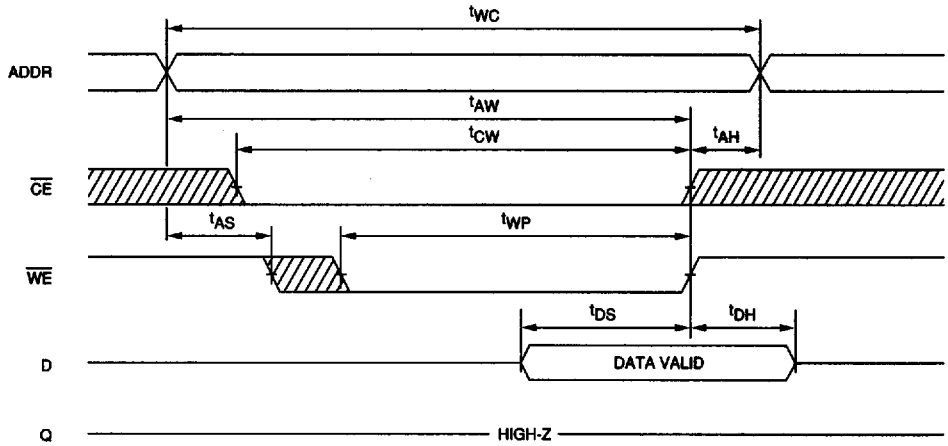
DON'T CARE

UNDEFINED

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [7, 12]
(Write Enable Controlled)



DON'T CARE

UNDEFINED

NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

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ELECTRICAL TEST REQUIREMENTS

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MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.