512Kx8 bit Low Power & Low Vcc CMOS Static RAM

FEATURE SUMMARY

- Process Technology : 0.4 um CMOS
- Organization : 512K x 8
- Power Supply Voltage : 3.3 +/- 0.3V *
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type : JEDEC Standard
  32-SOP, 32-TSOP(II)-Forward/Reverse

GENERAL DESCRIPTION

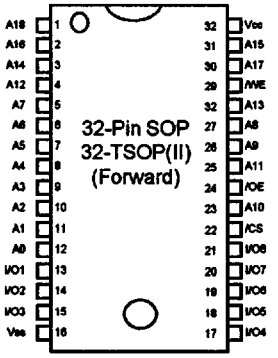
The KM68V4000A family is fabricated by SAMSUNG's advanced CMOS process technology. The family can support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

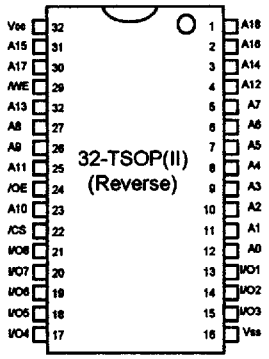
PRODUCT FAMILY

Product List	Operating Temp.	Vcc Range	Speed (ns)	PKG Type	Power Dissipation	
					Standby (Isb1, Max)	Operating (Icc2)
KM68V4000AL KM68V4000AL-L	Commercial (0~70 °C)	3.0~3.6V	70*/100	32-SOP 32-TSOP(II)-R/F	50/15uA	50mA
KM68V4000ALI KM68V4000ALI-L	Industrial (-40~85 °C)	3.0~3.6V	70*/100	32-SOP 32-TSOP(II)-R/F	50/20uA	

* measured with 30pF test load

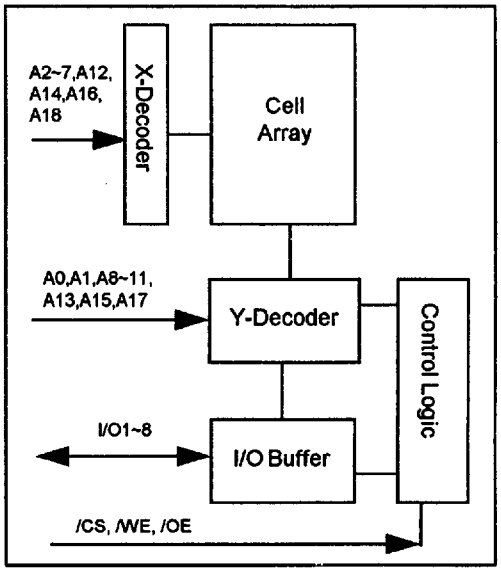
PIN DESCRIPTION





Name	Function	Name	Function
A0~A18	Address Inputs	Vcc	Power
/WE	Write Enable Input	Vss	Ground
/CS	Chip Select Input		
/OE	Output Enable Input		
I/O1~I/o8	Data Input/Output		

FUNCTIONAL BLOCK DIAGRAM

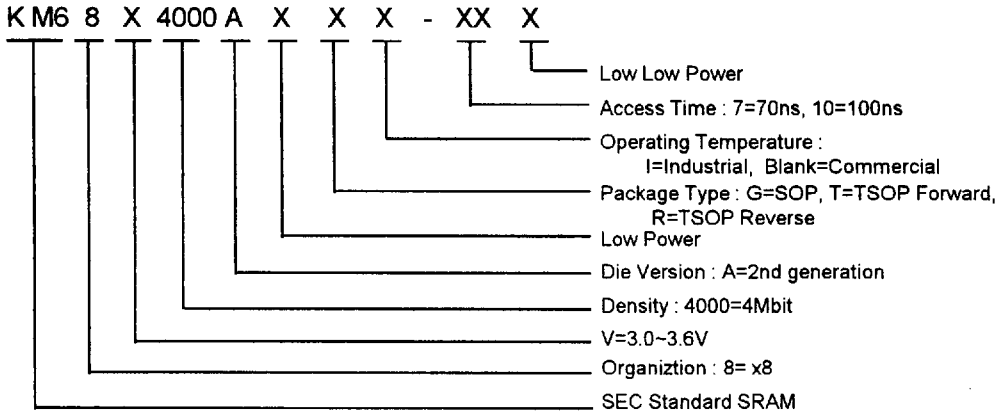


PRODUCT LIST & ORDERING INFORMATION

PRODUCT LIST

Commercial Temp Products (0~70 °C)		Industrial Temp Products (-40~85 °C)	
Part Name	**Function**	**Part Name**	**Function**
KM68V4000ALG-7	32-SOP, 70ns, 3.3V, L	KM68V4000ALGI-7	32-SOP, 70ns, 3.3V, L
KM68V4000ALG-7L	32-SOP, 70ns, 3.3V, LL	KM68V4000ALGI-7L	32-SOP, 70ns, 3.3V, LL
KM68V4000ALG-10	32-SOP, 100ns, 3.3V, L	KM68V4000ALGI-10	32-SOP, 100ns, 3.3V, L
KM68V4000ALG-10L	32-SOP, 100ns, 3.3V, LL	KM68V4000ALGI-10L	32-SOP, 100ns, 3.3V, LL
KM68V4000ALT-7L	32-TSOP (II) F, 70ns, 3.3V, L	KM68V4000ALTI-7L	32-TSOP(II) F, 70ns, 3.3V, L
KM68V4000ALT-7	32-TSOP (II) F, 70ns, 3.3V, LL	KM68V4000ALTI-7	32-TSOP(II) F, 70ns, 3.3V, LL
KM68V4000ALT-10	32-TSOP (II) F, 100ns, 3.3V, L	KM68V4000ALTI-10	32-TSOP (II) F, 100ns, 3.3V, L
KM68V4000ALT-10L	32-TSOP (II) F, 100ns, 3.3V, LL	KM68V4000ALTI-10L	32-TSOP (II) F, 100ns, 3.3V, LL
KM68V4000ALR-7	32-TSOP (II) R, 70ns, 3.3V, L	KM68V4000ALRI-7	32-TSOP (II) R, 70ns, 3.3V, L
KM68V4000ALR-7L	32-TSOP (II) R, 70ns, 3.3V, LL	KM68V4000ALRI-7L	32-TSOP (II) R, 70ns, 3.3V, LL
KM68V4000ALR-10	32-TSOP (II) R, 100ns, 3.3V, L	KM68V4000ALRI-10	32-TSOP (II) R, 100ns, 3.3V, L
KM68V4000ALR-10L	32-TSOP (II) R, 100ns, 3.3V, LL	KM68V4000ALRI-10L	32-TSOP (II) R, 100ns, 3.3V, LL

ORDERING INFORMATION



ABSOLUTE MAXIMUM RATINGS *

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	Vin, Vout	-0.5 to Vcc+0.5	V	-
Voltage on Vcc supply relative to Vss	Vcc	-0.3 to 4.6	V	-
Power Dissipation	Pd	0.7	W	-
Storage temperature	Tstg	-65 to 150	°C	-
Operating Temperature	Ta	0 to 70	°C	KM68V4000AL/L-L
		-40 to 85	°C	KM68V4000ALI/LI-L
Soldering temperature and time	Tsolder	260 °C , 10sec (Lead Only)	-	-

* Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not impilied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS*

Item	Symbol	Min	Typ**	Max	Unit
Supply voltage	Vcc	3.0	3.3	3.6	V
Ground	Vss	0	0	0	V
Input high voltage	Vih	2.2	-	Vcc+0.3	V
Input low voltage	Vil	-0.3***	-	0.4	V

* 1) Commercial Product : Ta=0 to 70 °C unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C unless otherwise specified
** Ta=25 °C
*** Vil(min)=-3.0V for ≤30ns pulse

CAPACITANCE * (f=1MHz, Ta=25 °C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	Cin	Vin=0V	-	8	pF
Input/Output capacitance	Cio	Vio=0V	-	10	pF

* Capacitance is sampled not 100% tested

DC AND OPERATING CHARACTERISTICS

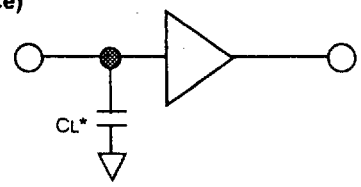
Item		Symbol	Test Conditions*		Min	Typ**	Max	Unit
Input leakage current		Ili	Vin=Vss to Vcc		-1	-	1	uA
Output leakage current		Ilo	/CS=Vih or Vil Vio=Vss to Vcc		-1	-	1	uA
Operating power supply current		Icc	/CS=Vil, Vin=Vih or Vil, Iio=0mA		-	-	15	mA
Average operating current		Icc1	Cycle time=1uS 100% duty /CS≤0.2V, Vil≤0.2V, Vin≥Vcc-0.2V, Iio=0mA		-	-	15	mA
		Icc2	Min cycle, 100% duty /CS=Vil, Iio=0mA, Vin=Vih or Vil		-	-	50	mA
Output low voltage		Vol	Iol=2.1mA		-	-	0.4	V
Output high voltage		Voh	Ioh=-1.0mA		2.2	-	-	V
Standby Current(TTL)		Isb	/CS=Vih		-	-	0.5	mA
Standby Current (CMOS)	KM68V4000AL	Isb1	/CS≥Vcc-0.2V Vin≤0.2V or	L	-	-	50	uA
	KM68V4000AL-L			LL	-	-	15	uA
	KM68V4000ALI		Vin≥Vcc-0.2V	L	-	-	50	uA
	KM68V4000ALI-L			LL	-	-	20	uA

* 1) Commercial Product : Ta=0 to 70 °C, Vcc=3.3 +/- 0.3V(68V4000A Family)
2) Industrial Product : Ta=-40 to 85 °C, Vcc=3.3 +/- 0.3V(68V4000AIFamily)
** Ta=25 °C

AC CHARACTERISTICS

TEST CONDITIONS(1. Test Load and Test Input/Output Reference)*

Item	Value	Remark
Input pulse level	0.4 to 2.2V	-
Input rise fall time	5ns	-
Input and output reference voltage	1.5V	-
Output load(See right)	C_L=100pF+1TTL **C_L=30pF+1TTL	-



* Including scope and jig capacitance

* See test condition of DC and Operating characteristics
** Test load for 70ns Industrial product

TEST CONDITIONS(2. Temperature and Vcc Conditions)

Product Family	Temperature	Power Supply(Vcc)	Speed Bin	Comments
KM68V4000AL/L-L	0~70 °C	3.3V +/- 0.3	70*/100ns	Commercial
KM68V4000ALI/LI-L	-40~85 °C	3.3V +/- 0.3	70*/100ns	Industrial

* All the parameters are measured with 30pF test load

PARAMETER LIST FOR EACH SPEED BIN

Parameter List		Symbol	Speed Bins				Units
			70ns*		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	100	-	ns
	Address access time	tAA	-	70	-	100	ns
	Chip select to output	tCO	-	70	-	100	ns
	Output enable to valid output	tOE	-	35	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	30	ns
	Output disable to high-Z output	tOHZ	0	25	0	30	ns
	Output hold from address change	tOH	10	-	15	-	ns
Write	Write cycle time	tWC	70	-	100	-	ns
	Chip select to end of write	tCW	60	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	80	-	ns
	Write pulse width	tWP	55	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	ns

* Test load for measuring parameters : Commercial product-100pF, Industrial product-30pF

DATA RETENTION CHARACTERISTICS

Item	Symbol		Test Condition*		Min	Typ**	Max	Unit
Vcc for data retention	Vdr		/CS≥Vcc-0.2V		2.0	-	3.6	V
Data retention current	Idr	KM68V4000AL/L-L	Vcc=3.0V	L-Ver	-	1	30	uA
			/CS≥Vcc-0.2V	LL-Ver	-	0.5	15	
		KM68V4000ALI/LI-L		L-Ver	-	-	30	
				LL-Ver	-	-	20	
Data retention set-up time	tSDR		See data retention waveform		0	-	-	ms
Recovery time	tRDR				5	-	-	

* 1) Commercial Product : Ta=0 to 70 °C , unless otherwise specified
2) Industrial Product : Ta=-40 to 85 °C , unless otherwise specified
** Ta=25 °C

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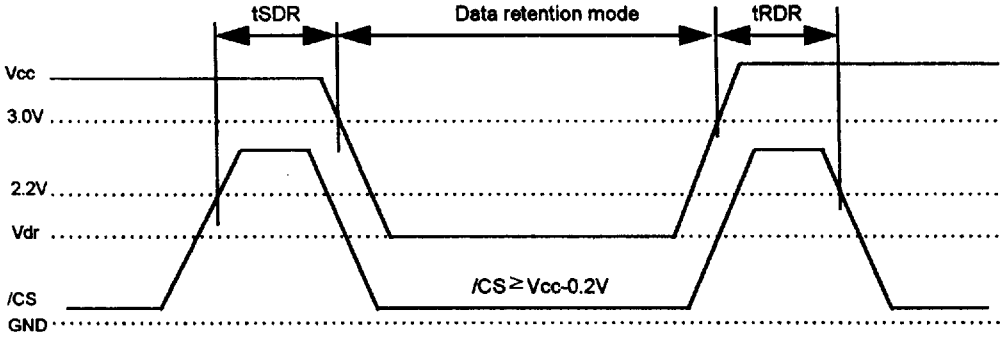
DATA RETENTION TIMING DIAGRAM



FUNCTIONAL DESCRIPTION

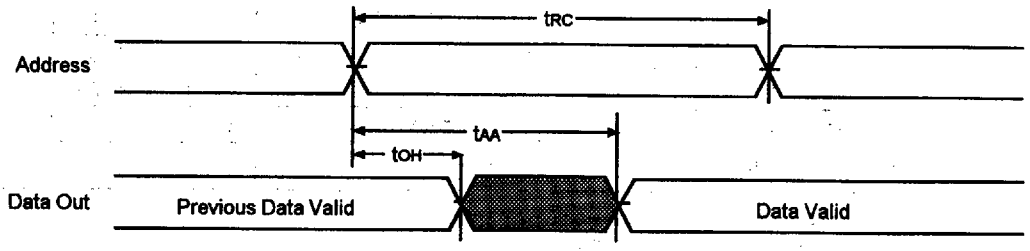
/CS	/WE	/OE	Mode	I/O Pin	Current Mode
H	X	X	Power Down	High-Z	Isb, Isb1
L	H	H	Ouput Disable	High-Z	Icc
L	H	L	Read	Dout	Icc
L	L	X	Write	Din	Icc

* X means don't care

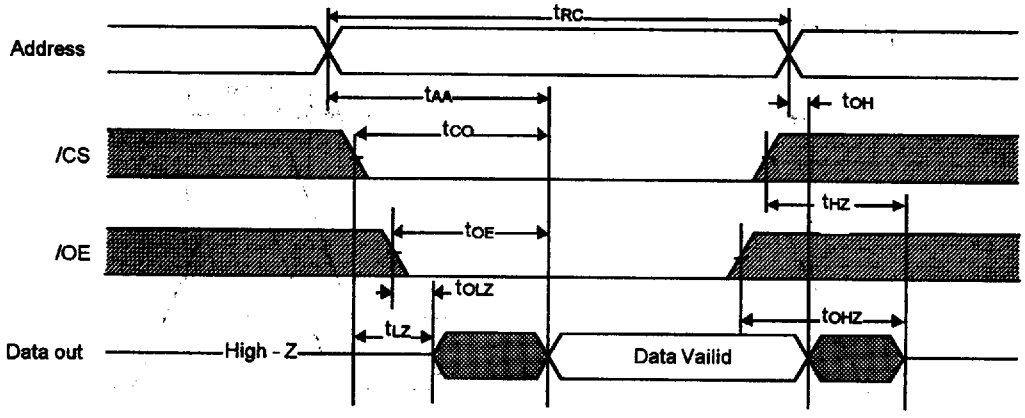
TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (1) (Address Controlled)

(/CS=/OE=Vil, /WE=Vih)



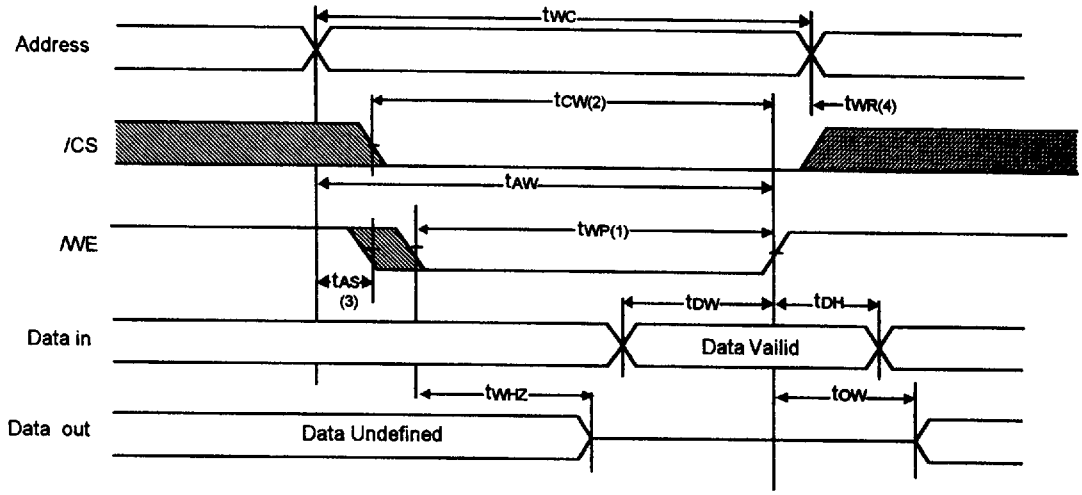
TIMING WAVEFORM OF READ CYCLE (/WE= VIH)



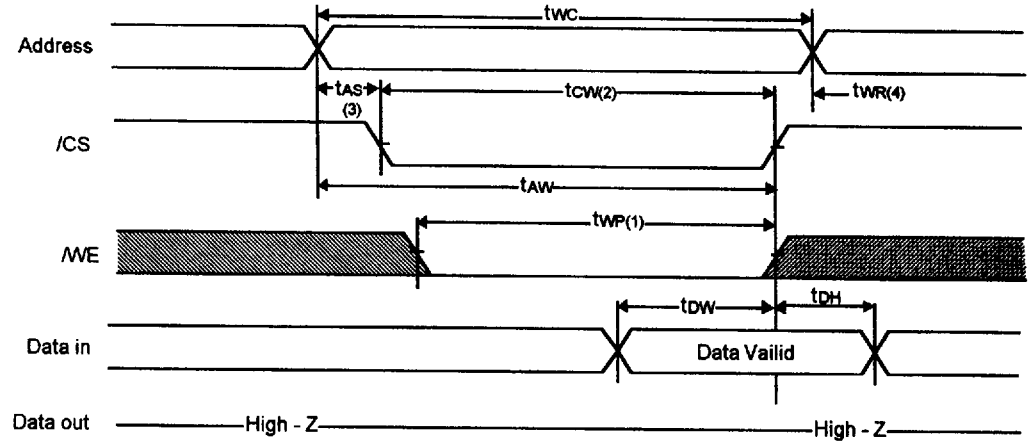
Notes (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ} (max.) is less than t_{LZ} (min.)both for a given device and from device to device.

TIMING WAVEFORM OF WRITE CYCLE (/WE Controlled)



TIMING WAVEFORM OF WRITE CYCLE (/CS Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap(tWP) of a low /CSand low /WE. A write begins at the latest transition among /CS going low and WE going low : A write end at the earliest transition among /CSgoing high and WE going high, tWP is measured from the beginning of write to the end of write.
2. tCW is measured from the later of /CS going low to end of write.
3. tAS is measured from the address valid to the beginning of write.
4. tWR is measured from the end of write to the address change. tWR applied in case a write ends as /CS,or /WE going high.