Integrated Device Technology, Inc.

CMOS STATIC RAM 16K (2K x 8-BIT)

IDT 6116SA
IDT 6116LA

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FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed
  - Military: 25/30/35/45/55/70/90/120/150ns (max.)
  - Commercial: 15/19/20/25/30/35/45ns (max.)
- Low-power operation
  - IDT6116SA
    Active: 180mW (typ.)
    Standby: 100µW (typ.)
  - IDT6116LA
    Active: 160mW (typ.)
    Standby: 20µW (typ.)
- Battery backup operation – 2V data retention voltage (LA version only)
- Produced with advanced CEMOS™ high-performance technology
- CEMOS process virtually eliminates alpha particle soft-error rates
- Single 5V (±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 24-pin DIP, 24-pin THINDIP and plastic DIP, 24-, 28- and 32-pin LCC, 24-pin SOIC and 24-lead CERPACK and Flatpack
- Military product compliant to MIL-STD-883, Class B
- Standard Military Drawing# 84036 is listed on this function. Refer to Section 2/page 2-4.

DESCRIPTION:

The IDT6116SA/LA is a 16,384-bit high-speed static RAM organized as 2K x 8. It is fabricated using IDT's high-performance, high-reliability technology – CEMOS. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost-effective alternative to bipolar and fast NMOS memories. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

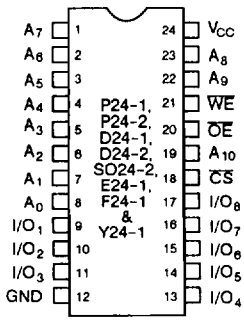
Access times as fast as 15ns are available with maximum power consumption of only 666mW. The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a standby power mode as long as $\overline{CS}$ remains high. In the standby mode, the low-power device consumes less than 20µW typically. This capability provides significant system level power and cooling savings. The low-power (LA) version also offers a battery backup data retention capability where the circuit typically consumes only 1µW to 4µW operating off a 2V battery.

All inputs and outputs of the IDT6116SA/LA are TTL-compatible and operation is from a single 5V supply, simplifying system designs. Fully static asynchronous circuitry is used, requiring no clocks or refreshing for operation, providing equal access and cycle times for ease of use.

The IDT6116SA/LA is packaged in 24-pin 600 and 300 mil plastic or ceramic DIP, 24-, 28- and 32-pin leadless chip carriers, 24-lead CERPACK and flatpack, and a 24-lead gull-wing SOIC, providing high board-level packing densities.

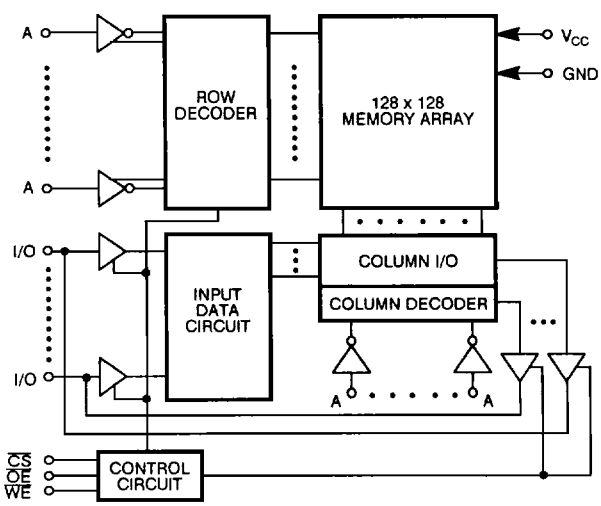
Military grade product is manufactured in compliance to the latest version of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

PIN CONFIGURATION



DIP/SOIC/FLATPACK/CERPACK TOP VIEW

FUNCTIONAL BLOCK DIAGRAM



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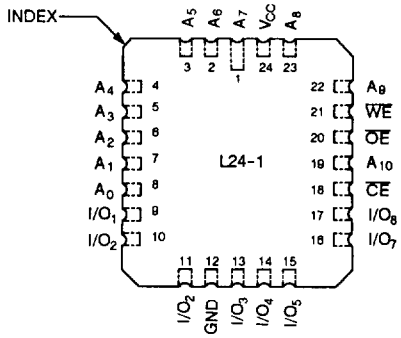
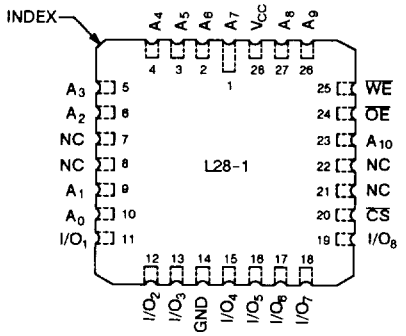
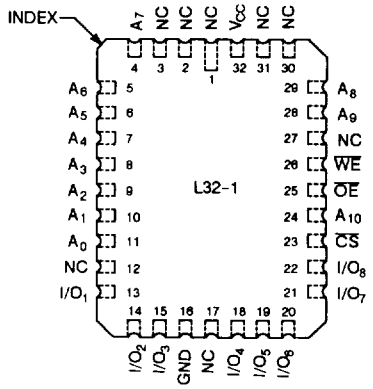
PIN CONFIGURATIONS



24-PIN LCC
TOP VIEW

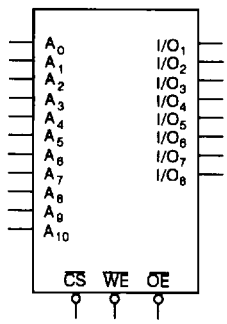


28-PIN LCC
TOP VIEW



32-PIN LCC
TOP VIEW

LOGIC SYMBOL



PIN NAMES

A_0- A_{10}	Address	$\overline{WE}$	Write Enable
I/O_1 - I/O_8	Data Input/Output	$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select	GND	Ground
V_{CC}	Power		

ABSOLUTE MAXIMUM RATINGS (1)

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	-0.5(1)	–	0.8	V
C_L	Output Load	–	–	30	pF

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%

SYMBOL	PARAMETER	TEST CONDITIONS		IDT6116SA MIN.	IDT6116SA TYP.(1)	IDT6116SA MAX.	IDT6116LA MIN.	IDT6116LA TYP.(1)	IDT6116LA MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	–	–	10	–	–	5	µA
			COM'L.	–	–	5	–	–	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.		–	–	0.4	–	–	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	–	–	2.4	–	–	V

NOTE:
1. Typical limits are at V_{CC} = 5.0V, +25°C ambient.

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DC ELECTRICAL CHARACTERISTICS (1)

V_{CC} = 5.0V ±10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	POWER	6116SA15(2)/19(2)/20(2) 6116LA15(2)/19(2)/20(2) COM'L.	6116SA15(2)/19(2)/20(2) 6116LA15(2)/19(2)/20(2) MIL.	6116SA25/30 6116LA25/30 COM'L.	6116SA25/30 6116LA25/30 MIL.	6116SA35 6116LA35 COM'L.	6116SA35 6116LA35 MIL.	6116SA45/55 6116LA45/55 COM'L.	6116SA45/55 6116LA45/55 MIL.	6116SA70/90 6116LA70/90 COM'L.	6116SA70/90 6116LA70/90 MIL.	6116SA120/150(3) 6116LA120/150(3) COM'L.	6116SA120/150(3) 6116LA120/150(3) MIL.	UNIT
I_{CC1}	Operating Power Supply Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = 0	SA	125/110	–	100/80	110	80	90	80/–	90	–	90	–	90	mA
		LA	115/100	–	90/75	105	75	85	75/–	85	–	85	–	85	
I_{CC2}	Dynamic Operating Current $\overline{CS}$ = V_{IL}, Outputs Open, V_{CC} = Max., f = f_{MAX} (4)	SA	150/130	–	120/110	135	100	115	100/–	100	–	100	–	100/90	mA
		LA	140/120	–	110/105	125	95	105	90/–	95/90	–	90/85	–	85	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., Outputs Open, f = f_{MAX} (4)	SA	40	–	40/35	45	25	35	25/–	25	–	25	–	25	mA
		LA	35	–	35/30	40	25	30	20/–	20	–	20/15	–	15	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS}$ ≥ V_{HC}, V_{CC} = Max., V_{IN} ≥ V_{HC} or V_{IN} ≤ V_{LC}, f = 0	SA	2	–	2	10	2	10	2/–	10	–	10	–	10	mA
		LA	0.1	–	0.1	0.9	0.1	0.9	0.1/–	0.9	–	0.9	–	0.9	

NOTES:
1. All values are maximum guaranteed values.
2. 0°C to +70°C temperature range only.
3. -55°C to +125°C temperature range only.
4. f_{MAX} = $1/t_{RC}$

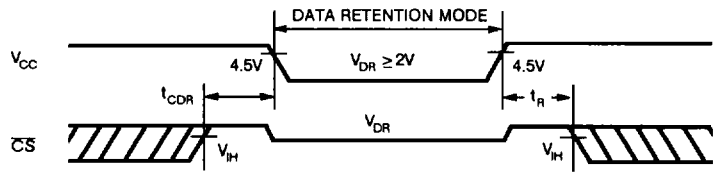
DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

(LA Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.(1) V_{CC} @ 2.0V	TYP.(1) V_{CC} @ 3.0V	MAX. V_{CC} @ 2.0V	MAX. V_{CC} @ 3.0V	UNIT
V_{DR}	V_{CC} for Data Retention	–		2.0	–	–	–	–	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$	MIL.	–	0.5	1.5	200	300	µA
			COM'L.	–	0.5	1.5	20	30	
t_{CDR}(3)	Chip Deselect to Data Retention Time			0	–		–		ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	–		–		ns
$\|I_{LI}\|$	Input Leakage Current			–	–		2		µA

NOTES:
1. T_A = +25°C
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed, but not tested.

LOW V_{CC} DATA RETENTION WAVEFORM



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

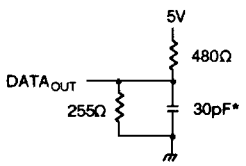


Figure 1. Output Load

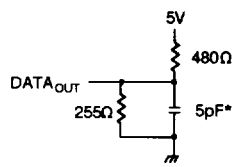


Figure 2. Output Load (for t_{OLZ}, t_{CLZ}, t_{OHZ}, t_{WHZ}, t_{CHZ}, t_{OW})

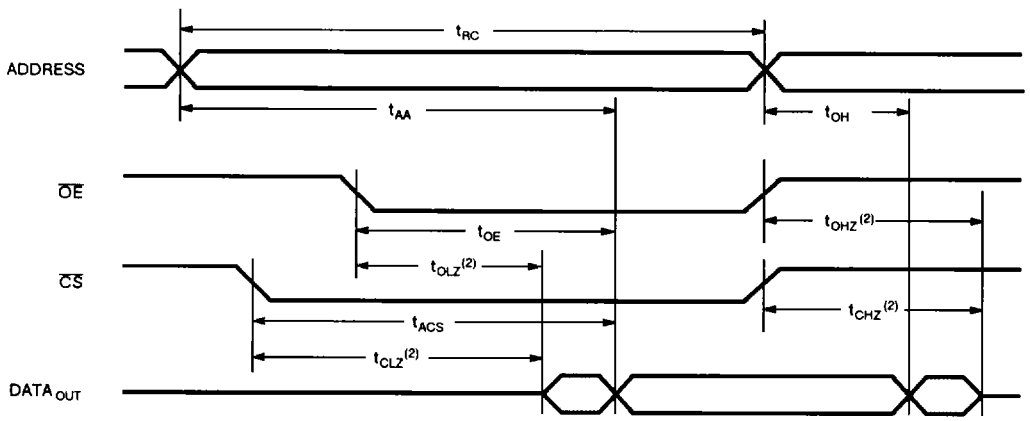
*Including scope and jig.

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6116SA15/19[1]/20[1] 6116LA15/19[1]/20[1] MIN.	MAX.	6116SA25/30 6116LA25/30 MIN.	MAX.	6116SA35/45 6116LA35/45 MIN.	MAX.	6116SA55[2] 6116LA55[2] MIN.	MAX.	6116SA70/90[2] 6116LA70/90[2] MIN.	MAX.	6116SA120/150[2] 6116LA120/150[2] MIN.	MAX.	UNIT
READ CYCLE														
t_{RC}	Read Cycle Time	15/19/20	–	25/30	–	35/45	–	55	–	70/90	–	120/150	–	ns
t_{AA}	Address Access Time	–	15/19/20	–	25/29	–	35/45	–	55	–	70/90	–	120/150	ns
t_{ACS}	Chip Select Access Time	–	15/20/20	–	25/30	–	35/45	–	50	–	65/90	–	120/150	ns
t_{CLZ}	Chip Select to Output in Low Z[3]	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	10	–	13/15	–	20/25	–	40	–	50/65	–	80/100	ns
t_{OLZ}	Output Enable to Output in Low Z[3]	0	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}	Chip Deselect to Output in High Z[3]	–	10/11/11	–	12/13	–	15/20	–	30	–	35/40	–	40	ns
t_{OHZ}	Output Disable to Output in High Z[3]	–	8/8/9	–	10/12	–	13/15	–	30	–	35/40	–	40	ns
t_{OH}	Output Hold from Address Change	3	–	5	–	5	–	5	–	5	–	5	–	ns

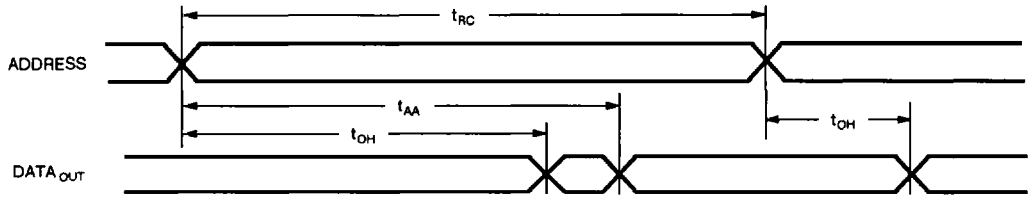
NOTES:
1. 0°C to +70°C temperature range only.
2. −55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.

TIMING WAVEFORM OF READ CYCLE NO. 1 [1]

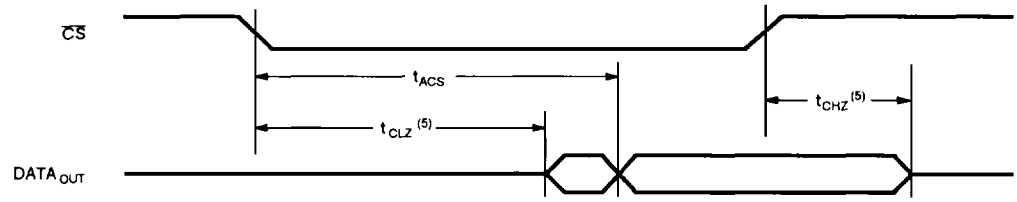


NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}
5. Transition is measured ±500mV from steady state with 5pF load (including scope and jig).

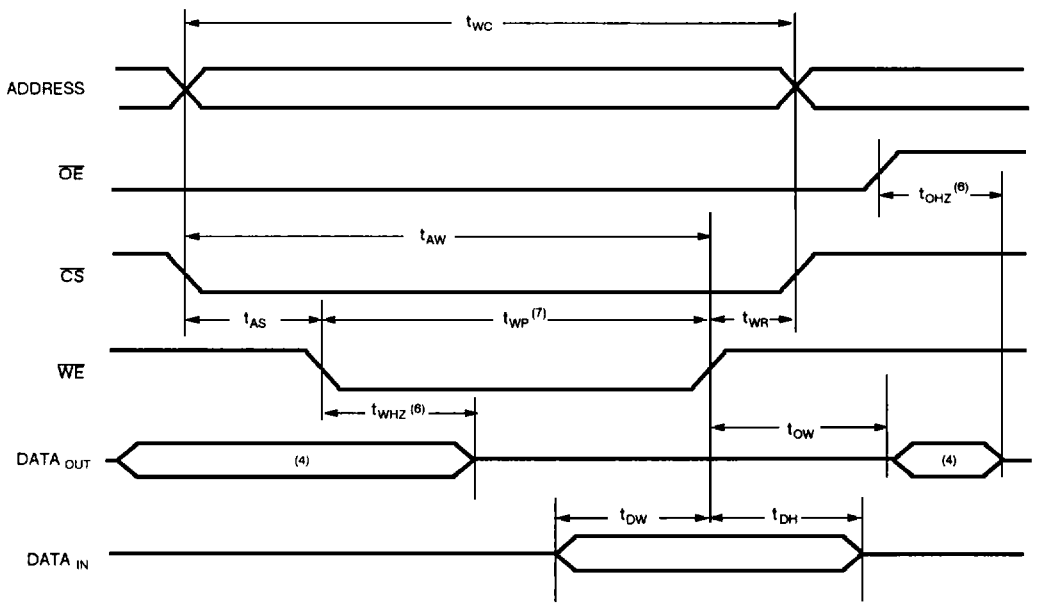
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ±10%, All Temperature Ranges)

SYMBOL	PARAMETER	6116SA15/19[1]/20[1] 6116LA15/19[1]/20[1] MIN.	MAX.	6116SA25/30 6116LA25/30 MIN.	MAX.	6116SA35/45 6116LA35/45 MIN.	MAX.	6116SA55[2] 6116LA55[2] MIN.	MAX.	6116SA70/90[2] 6116LA70/90[2] MIN.	MAX.	6116SA120/150[2] 6116LA120/150[2] MIN.	MAX.	UNIT
WRITE CYCLE														
t_{WC}	Write Cycle Time	15/19/20	–	25/30	–	35/45	–	55	–	70/90	–	120/150	–	ns
t_{CW}	Chip Select to End of Write	13/15/15	–	17/20	–	25/30	–	40	–	40/55	–	70/90	–	ns
t_{AW}	Address Valid to End of Write	14/15/15	–	17/20	–	25/30	–	45	–	65/80	–	105/120	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	5	–	15	–	20	–	ns
t_{WP}	Write Pulse Width	12/12/15	–	15	–	20/25	–	40	–	40/55	–	70/90	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	5	–	5	–	5/10	–	ns
t_{OHZ}	Output Disable to Output in High Z[3]	–	8/9/9	–	16/18	–	20/25	–	30	–	35/40	–	40	ns
t_{WHZ}	Write to Output in High Z[3]	–	7/8/8	–	16/18	–	20/25	–	30	–	35/40	–	40	ns
t_{DW}	Data to Write Time Overlap	12	–	13/14	–	15/20	–	25	–	30	–	35/40	–	ns
t_{DH}	Data Hold from Write Time[4]	0	–	0	–	0	–	5	–	5	–	5/10	–	ns
t_{OW}	Output Active from End of Write[3,4]	0	–	0	–	0	–	0	–	0	–	0	–	ns

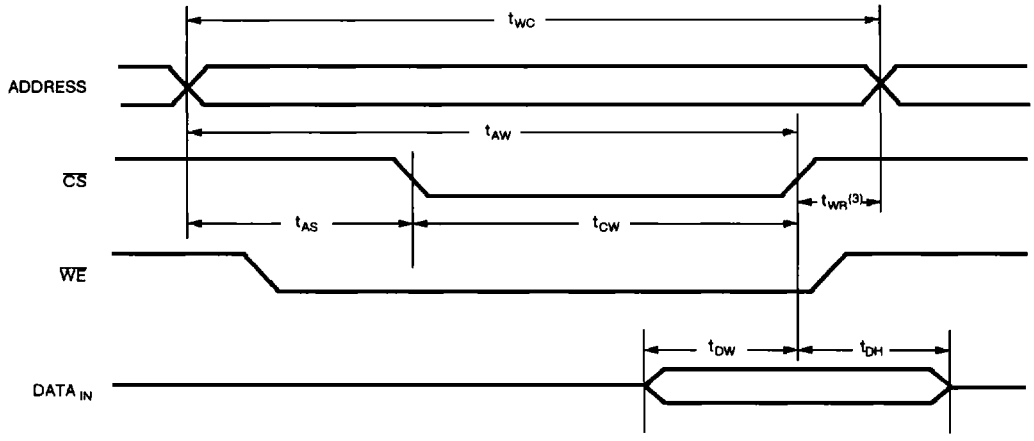
NOTES:

1. 0°C to +70°C temperature range only.
2. -55°C to +125°C temperature range only.
3. This parameter guaranteed but not tested.
4. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.

TIMING WAVEFORM OF WRITE CYCLE NO. 1, ($\overline{WE}$ CONTROLLED TIMING)[1, 2, 3, 7]



TIMING WAVEFORM OF WRITE CYCLE NO. 2, ($\overline{CS}$ CONTROLLED TIMING)[1, 2, 3, 5]

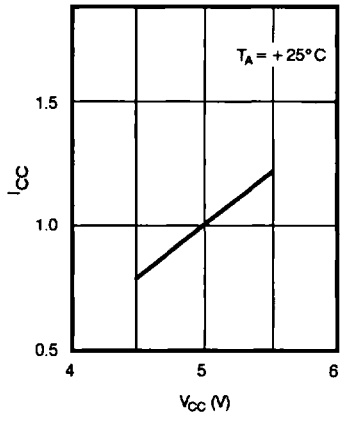


NOTES:

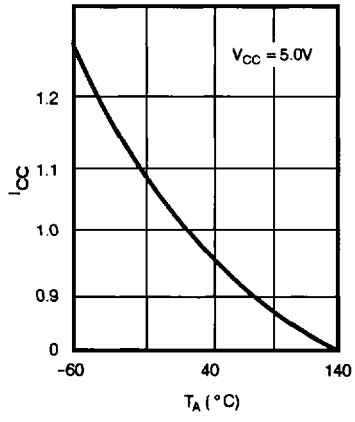
1. $\overline{WE}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{CW} or t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, the I/O pins are in the output state, and the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in the high impedance state.
6. Transition is measured ±500mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

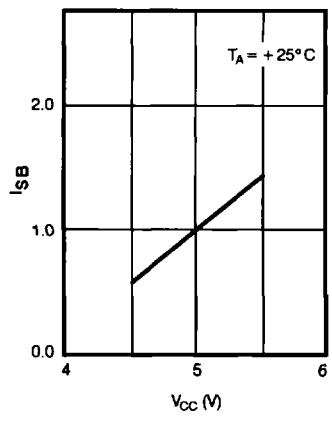
I_{CC} vs. Supply Voltage



I_{CC} vs. Temperature

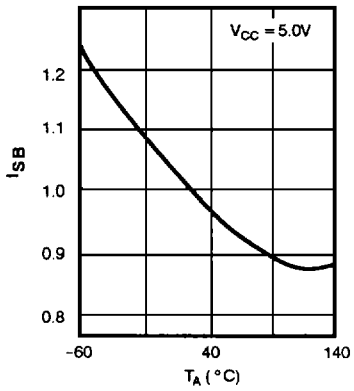


I_{SB} vs. Supply Voltage

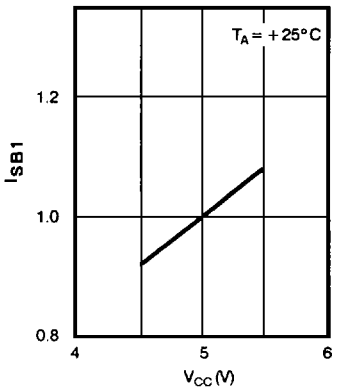


NORMALIZED TYPICAL DC AND AC CHARACTERISTICS

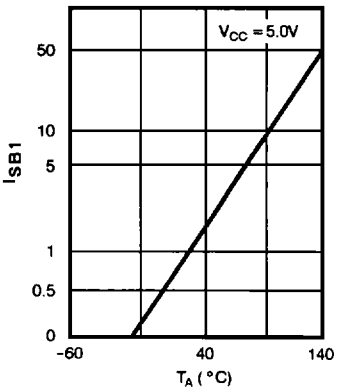
I_{SB} vs. Temperature



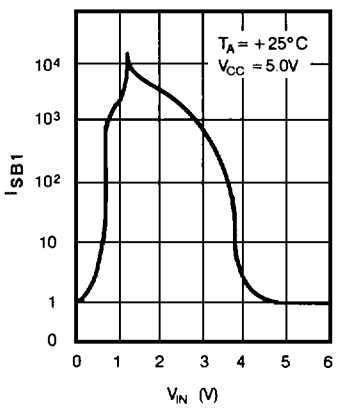
I_{SB1} vs. Supply Voltage



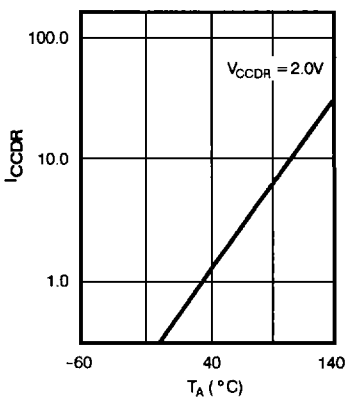
I_{SB1} vs. Temperature



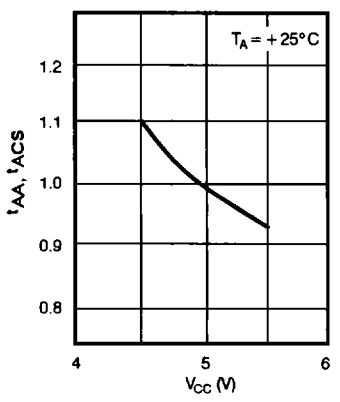
I_{SB1} vs. V_{IN}



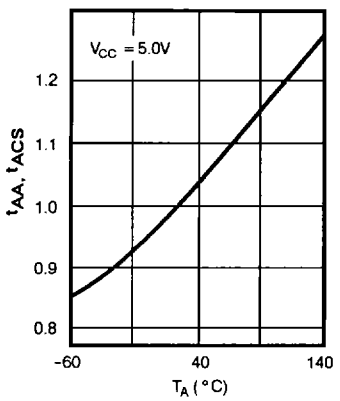
I_{CCDR} vs. Temperature



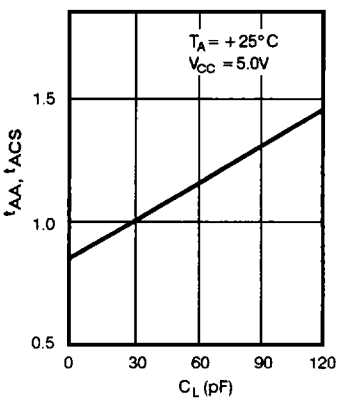
t_{AA}, t_{ACS} vs. Supply Voltage



t_{AA}, t_{ACS} vs. Temperature



t_{AA}, t_{ACS} vs. Output Loading



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TRUTH TABLE

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	I/O
Standby	H	X	X	High Z
Read	L	L	H	$DATA_{OUT}$
Read	L	H	H	High Z
Write	L	X	L	$DATA_{IN}$

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	8	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

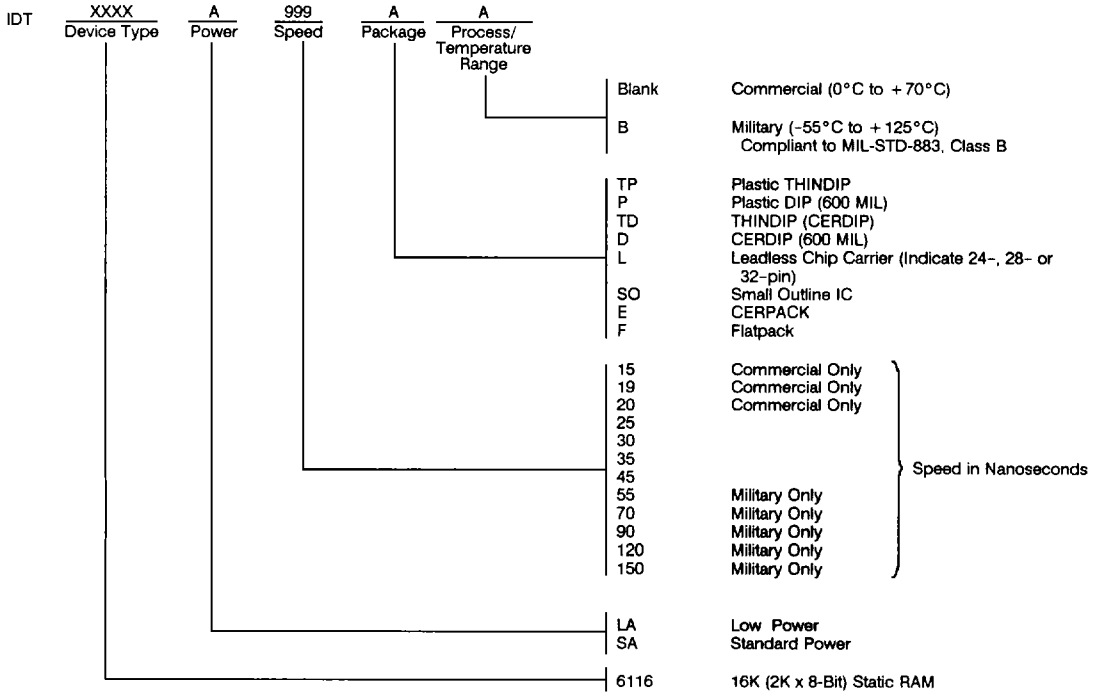
PINOUT CONFIGURATION
16K CMOS SRAM
IDT6116 (2K x 8)

FUNCTION	LOGIC SYMBOL	PIN NUMBER 24 DIP/ SOIC/ LCC/ FLATPACK	PIN NUMBER 28 LCC	PIN NUMBER 32 LCC
Address Line	A_7	1	1	4
Address Line	A_6	2	2	5
Address Line	A_5	3	3	6
Address Line	A_4	4	4	7
Address Line	A_3	5	5	8
Address Line	A_2	6	6	9
Address Line	A_1	7	9	10
Address Line	A_0	8	10	11
Input/Output	I/O_1	9	11	13
Input/Output	I/O_2	10	12	14
Input/Output	I/O_3	11	13	15
Power Ground	GND	12	14	16
Input/Output	I/O_4	13	15	18
Input/Output	I/O_5	14	16	19
Input/Output	I/O_6	15	17	20
Input/Output	I/O_7	16	18	21
Input/Output	I/O_8	17	19	22
Chip Select/ Data Retention	$\overline{CS}$	18	20	23
Address Line	A_{10}	19	23	24
Output Enable	$\overline{OE}$	20	24	25
Write Enable	$\overline{WE}$	21	25	26
Address Line	A_9	22	26	28
Address Line	A_8	23	27	29
Power Supply	V_{CC}	24	28	32

THERMAL RESISTANCE (Typical)

PACKAGE	PIN COUNT	θ_{JA}	θ_{JC}	UNIT
300 MIL PLASTIC DIP	24	54-58	28-32	°C/ WATT
600 MIL PLASTIC DIP	24	53-56	25-30	
300 MIL CERDIP	24	48-52	24-28	
600 MIL CERDIP	24	50-55	17-25	
FLATPACK	24	85-90	24-28	
LCC	24	85-110	30-45	
LCC	28	85-90	28-35	
LCC	32	80-90	25-35	
SOIC	24	45-70	25-30	

ORDERING INFORMATION



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