512Kx32 SRAM MODULE, SMD 5962-94611 *PRELIMINARY**

FEATURES

- Access Times of 17, 20, 25, 35, 45, 55ns
- Packaging
  - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400).
  - 66 pin, PGA Type, 1.385 inch square, Hermetic Ceramic HIP (Package 402).
  - 68 lead, 40mm Hermetic Low Profile CQFP, 3.5mm (0.140") (Package 502), Package to be developed.
  - 68 lead, Hermetic CQFP (G2T), 22.4mm (0.880 inch) square (Package 509) 4.57mm (0.180 inch) height. Designed to fit JEDEC 68 lead 0.990" CQFJ footprint (Fig. 3).
- Organized as 512Kx32, User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- TTL Compatible Inputs and Outputs
- 5 Volt Power Supply
- Low Power CMOS
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
  WS512K32-XH1X - 13 grams typical
  WS512K32-XH2X - 13 grams typical
  WS512K32-XG2TX - 13 grams typical
  WS512K32-XG4TX - 20 grams typical

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

FIG. 1 PIN CONFIGURATION FOR WS512K32N-XH1X AND WS512K32N-XH2X

TOP VIEW

1	12	23	34	45	56
I/O8	$\overline{WE}_2$	I/O15	I/O24	VCC	I/O31
I/O9	$\overline{CS}_2$	I/O14	I/O25	$\overline{CS}_4$	I/O30
I/O10	GND	I/O13	I/O26	$\overline{WE}_4$	I/O29
A13	I/O11	I/O12	A6	I/O27	I/O28
A14	A10	$\overline{OE}$	A7	A3	A0
A15	A11	A18	NC	A4	A1
A16	A12	$\overline{WE}_1$	A8	A5	A2
A17	VCC	I/O7	A9	$\overline{WE}_3$	I/O23
I/O0	$\overline{CS}_1$	I/O6	I/O16	$\overline{CS}_3$	I/O22
I/O1	NC	I/O5	I/O17	GND	I/O21
I/O2	I/O3	I/O4	I/O18	I/O19	I/O20
11	22	33	44	55	66

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

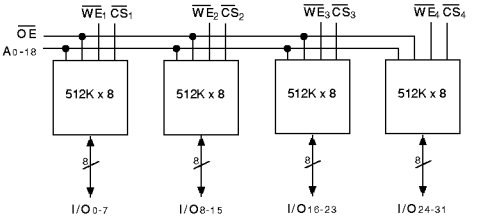
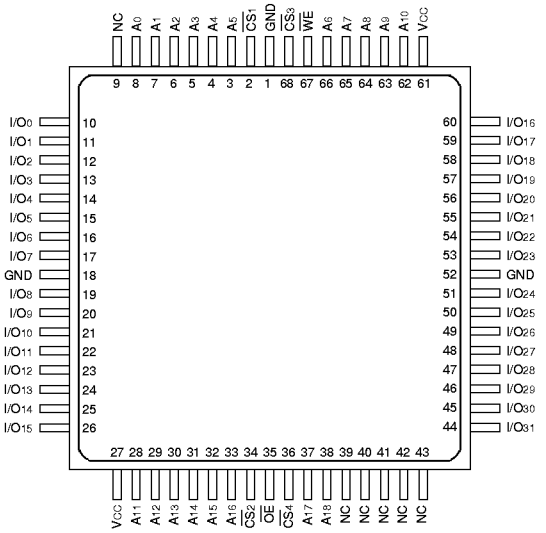


FIG. 2 PIN CONFIGURATION FOR WS512K32-XG4TX

TOP VIEW



PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM

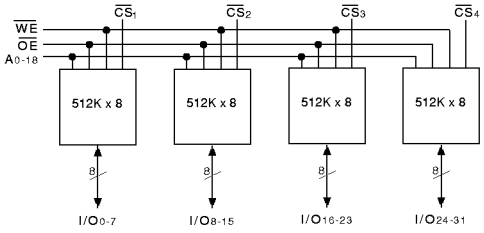
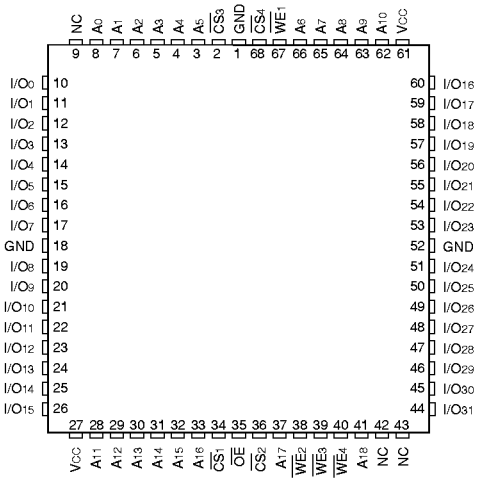
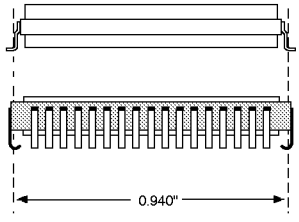


FIG. 3 PIN CONFIGURATION FOR WS512K32-XG2TX

TOP VIEW



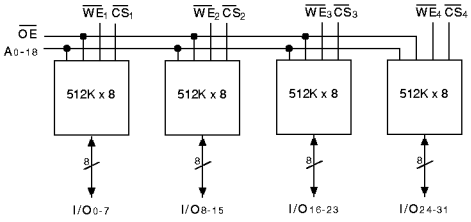


The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O0-31	Data Inputs/Outputs
A0-18	Address Inputs
$\overline{WE}_{1-4}$	Write Enables
$\overline{CS}_{1-4}$	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Signal Voltage Relative to GND	V_G	-0.5	Vcc+0.5	V
Junction Temperature	T_J		150	°C
Supply Voltage	V_{CC}	-0.5	7.0	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	4.5	5.5	V
Input High Voltage	V_{IH}	2.2	V_{CC} + 0.3	V
Input Low Voltage	V_{IL}	-0.5	+0.8	V
Operating Temp (Mil)	T_A	-55	+125	°C

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	H	H	Out Disable	High Z	Active
L	X	L	Write	Data In	Active

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz		pF
HIP (PGA)			20	
CQFP G4T			50	
CQFP G2T			20	
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Units
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = GND to V_{CC}		10	µA
Output Leakage Current	I_{LO}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, V_{OUT} = GND to V_{CC}		10	µA
Operating Supply Current x 32 Mode	$I_{CC\ x\ 32}$	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		540	mA
Standby Current	I_{SB}	$\overline{CS}$ = V_{IH}, $\overline{OE}$ = V_{IH}, f = 5MHz, V_{CC} = 5.5		60	mA
Output Low Voltage	V_{OL}	I_{OL} = 8mA for 17 - 35ns, I_{OL} = 2.1mA for 45 - 55ns, V_{CC} = 4.5		0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA for 17 - 35ns, I_{OH} = -1.0mA for 45 - 55ns, V_{CC} = 4.5	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} -0.3V, V_{IL} = 0.3V

DATA RETENTION CHARACTERISTICS

(T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Data Retention Supply Voltage	V_{DR}	$\overline{CS}$ ≥ V_{CC} -0.2V	2.0		5.5	V
Data Retention Current	I_{CCDR1}	V_{CC} = 3V		3.2	28*	mA

* Also available in Low Power version, please call factory for information.

AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
Read Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	17		20		25		35		45		55		ns
Address Access Time	t_{AA}		17		20		25		35		45		55	ns
Output Hold from Address Change	t_{OH}	0		0		0		0		0		0		ns
Chip Select Access Time	t_{ACS}		17		20		25		35		45		55	ns
Output Enable to Output Valid	t_{OE}		9		10		12		25		25		25	ns
Chip Select to Output in Low Z	t_{CLZ}[1]	2		2		2		4		4		4		ns
Output Enable to Output in Low Z	t_{OLZ}[1]	0		0		0		0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}[1]		12		12		12		15		20		20	ns
Output Disable to Output in High Z	t_{OHZ}[1]		12		12		12		15		20		20	ns

1. This parameter is guaranteed by design but not tested.

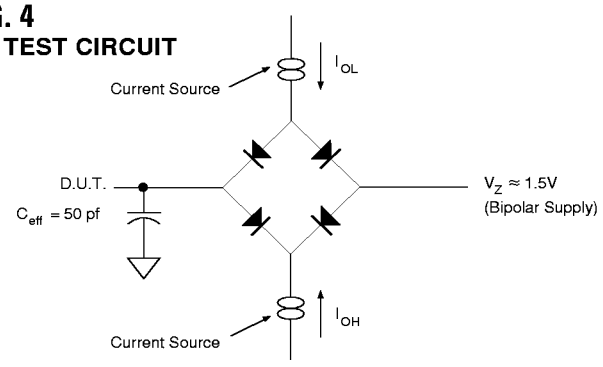
AC CHARACTERISTICS

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-17		-20		-25		-35		-45		-55		Units
Write Cycle		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	17		20		25		35		45		55		ns
Chip Select to End of Write	t_{CW}	15		15		17		25		35		50		ns
Address Valid to End of Write	t_{AW}	15		15		17		25		35		50		ns
Data Valid to End of Write	t_{DW}	11		12		13		20		25		25		ns
Write Pulse Width	t_{WP}	15		15		17		25		35		40		ns
Address Setup Time	t_{AS}	2		2		2		2		2		2		ns
Address Hold Time	t_{AH}	0		0		0		0		5		5		ns
Output Active from End of Write	t_{OW}[1]	2		3		4		4		5		5		ns
Write Enable to Output in High Z	t_{WHZ}[1]		9		11		13		15		20		20	ns
Data Hold Time	t_{DH}	0		0		0		0		0		0		ns

1. This parameter is guaranteed by design but not tested.
2. The Address Setup Time of minimum 2ns is for the G2 and H2 packages. t_{AS} minimum for G4 and G4T packages is 0ns.

FIG. 4
AC TEST CIRCUIT

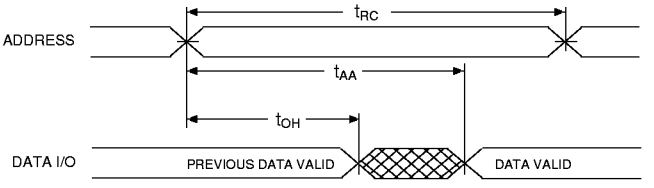


AC TEST CONDITIONS

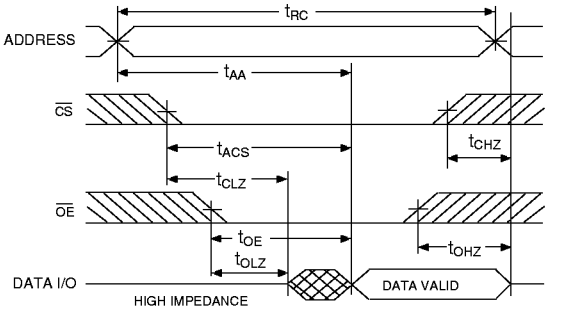
Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

FIG. 5
TIMING WAVEFORM - READ CYCLE

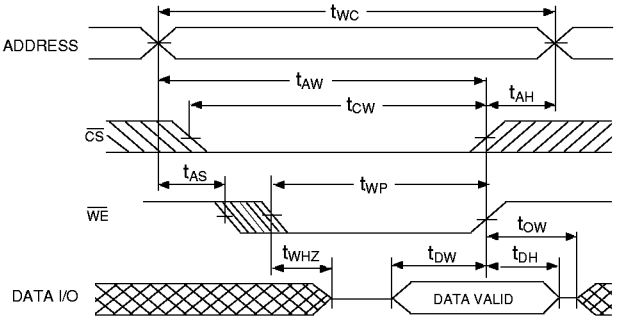


READ CYCLE 1 ($\overline{CS}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH})



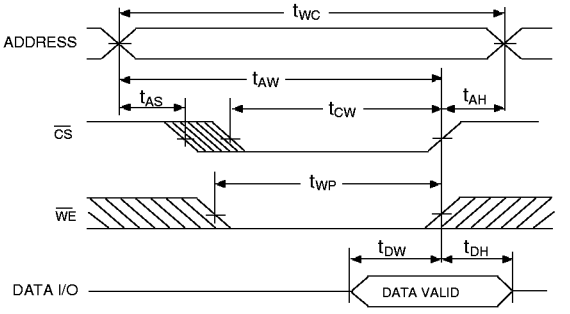
READ CYCLE 2 ($\overline{WE}$ = V_{IH})

FIG. 6
WRITE CYCLE - $\overline{WE}$ CONTROLLED



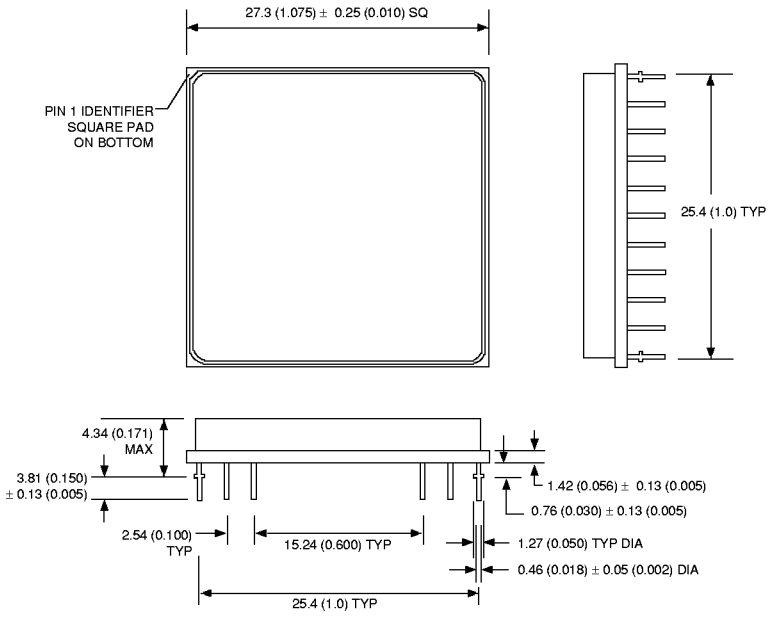
WRITE CYCLE 1, $\overline{WE}$ CONTROLLED

FIG. 7
WRITE CYCLE - $\overline{CS}$ CONTROLLED



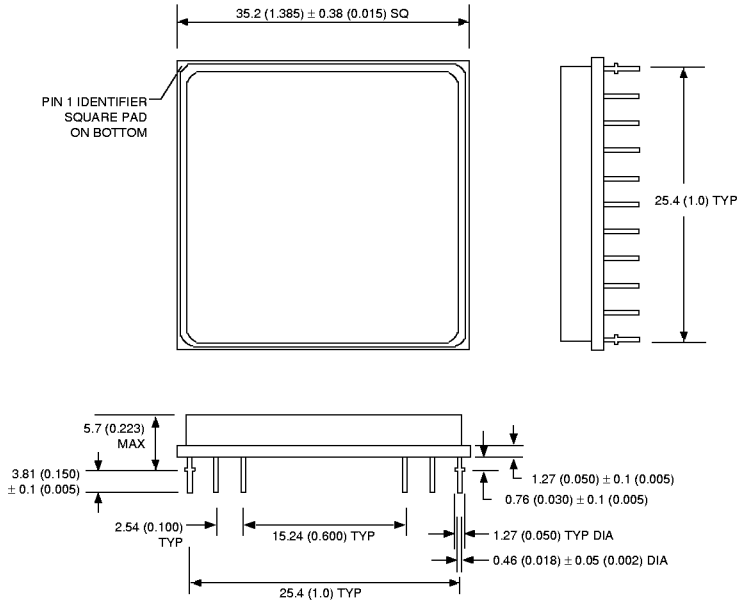
WRITE CYCLE 2, $\overline{CS}$ CONTROLLED

PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



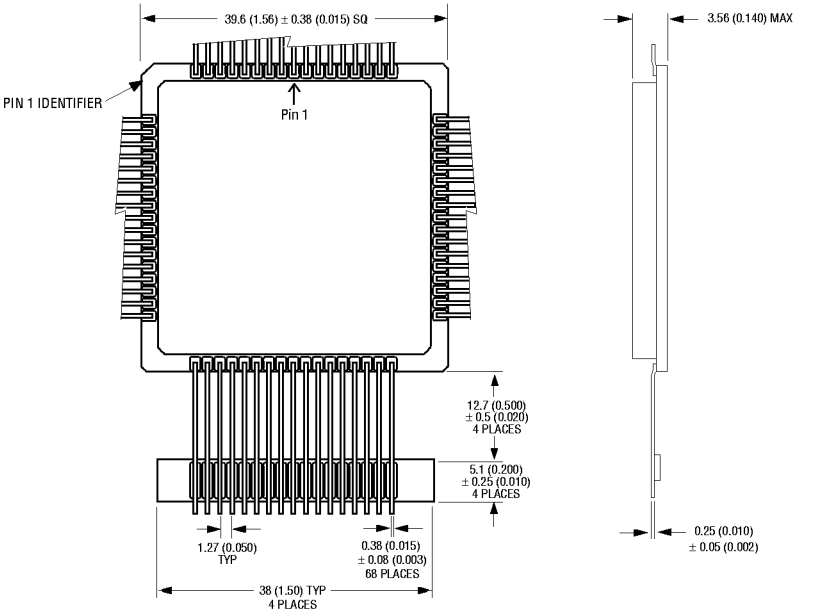
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)



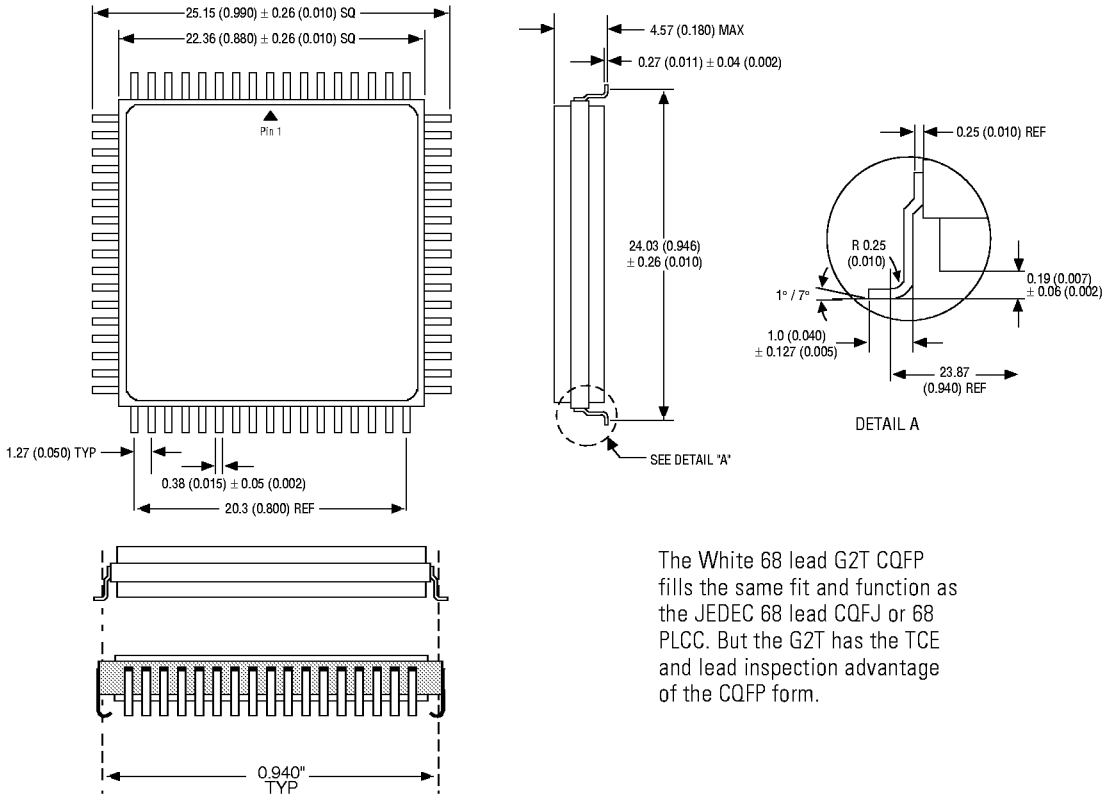
ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 502: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G4T)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

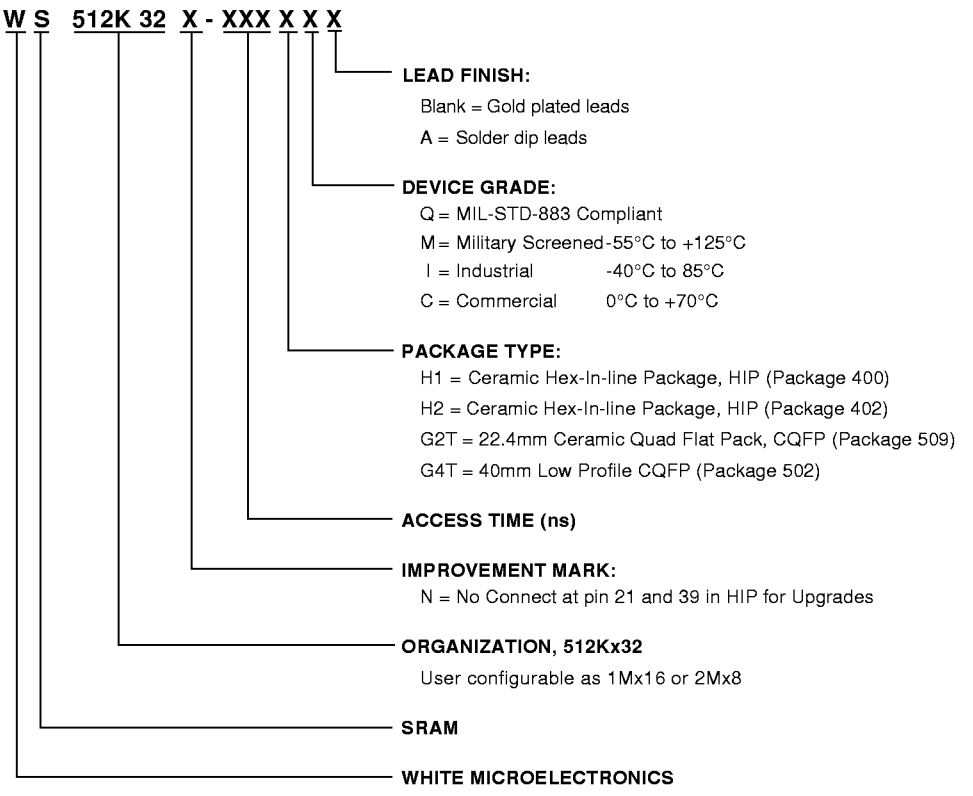
PACKAGE 509: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2T)



The White 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



DEVICE TYPE	SPEED	PACKAGE	SMD NO.
512K x 32 SRAM Module	55ns	66 pin HIP (H1)	5962-94611 05HTX
512K x 32 SRAM Module	45ns	66 pin HIP (H1)	5962-94611 06HTX
512K x 32 SRAM Module	35ns	66 pin HIP (H1)	5962-94611 07HTX
512K x 32 SRAM Module	25ns	66 pin HIP (H1)	5962-94611 08HTX
512K x 32 SRAM Module	20ns	66 pin HIP (H1)	5962-94611 09HTX
512K x 32 SRAM Module	17ns	66 pin HIP (H1)	5962-94611 10HTX
512K x 32 SRAM Module	55ns	66 pin HIP (H2)	5962-94611 05HXX
512K x 32 SRAM Module	45ns	66 pin HIP (H2)	5962-94611 06HXX
512K x 32 SRAM Module	35ns	66 pin HIP (H2)	5962-94611 07HXX
512K x 32 SRAM Module	25ns	66 pin HIP (H2)	5962-94611 08HXX
512K x 32 SRAM Module	20ns	66 pin HIP (H2)	5962-94611 09HXX
512K x 32 SRAM Module	17ns	66 pin HIP (H2)	5962-94611 10HXX
512K x 32 SRAM Module	55ns	68 lead CQFP Low Profile (G4T)	5962-94611 05HYX
512K x 32 SRAM Module	45ns	68 lead CQFP Low Profile (G4T)	5962-94611 06HYX
512K x 32 SRAM Module	35ns	68 lead CQFP Low Profile (G4T)	5962-94611 07HYX
512K x 32 SRAM Module	25ns	68 lead CQFP Low Profile (G4T)	5962-94611 08HYX
512K x 32 SRAM Module	20ns	68 lead CQFP Low Profile (G4T)	5962-94611 09HYX
512K x 32 SRAM Module	17ns	68 lead CQFP Low Profile (G4T)	5962-94611 10HYX
512K x 32 SRAM Module	55ns	68 lead CQFP/J (G2T)	5962-94611 05HMX
512K x 32 SRAM Module	45ns	68 lead CQFP/J (G2T)	5962-94611 06HMX
512K x 32 SRAM Module	35ns	68 lead CQFP/J (G2T)	5962-94611 07HMX
512K x 32 SRAM Module	25ns	68 lead CQFP/J (G2T)	5962-94611 08HMX
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