Advanced Power MOSFET

SFW/I9640

FEATURES

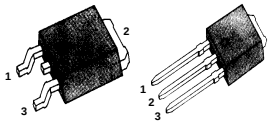
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- Extended Safe Operating Area
- Lower Leakage Current : 10 μA (Max.) @ V_{DS} = -200V
- Low $R_{DS(ON)}$: 0.344 Ω (Typ.)

BV_{DSS} = -200 V

$R_{DS(on)}$ = 0.5 Ω

I_D = -11 A

D²-PAK **I²-PAK**



1. Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V_{DSS}	Drain-to-Source Voltage	-200	V
I_D	Continuous Drain Current (T_C=25°C)	-11	A
	Continuous Drain Current (T_C=100°C)	-7.0	
I_{DM}	Drain Current-Pulsed ①	-44	A
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy ②	807	mJ
I_{AR}	Avalanche Current ①	-11	A
E_{AR}	Repetitive Avalanche Energy ①	12.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
P_D	Total Power Dissipation (T_A=25°C) *	3.1	W
	Total Power Dissipation (T_C=25°C)	123	W
	Linear Derating Factor	0.98	W/°C
T_J , T_{STG}	Operating Junction and Storage Temperature Range	- 55 to +150	°C
T_L	Maximum Lead Temp. for Soldering Purposes, 1/8 " from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	--	1.02	°C/W
$R_{\theta JA}$	Junction-to-Ambient *	--	40	
$R_{\theta JA}$	Junction-to-Ambient	--	62.5	

* When mounted on the minimum pad size recommended (PCB Mount).

FAIRCHILD SEMICONDUCTOR™

Electrical Characteristics (T_C=25°C unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	-200	--	--	V	V_{GS}=0V,I_D=-250μA
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	-0.16	--	V/°C	I_D=-250μA ***See Fig 7***
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	--	-4.0	V	V_{DS}=-5V,I_D=-250μA
I_{GSS}	Gate-Source Leakage , Forward	--	--	-100	nA	V_{GS}=-30V
	Gate-Source Leakage , Reverse	--	--	100		V_{GS}=30V
I_{DSS}	Drain-to-Source Leakage Current	--	--	-10	μA	V_{DS}=-200V
		--	--	-100		V_{DS}=-160V,T_C=125°C
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.5	Ω	V_{GS}=-10V,I_D=-5.5A ④
g_{fs}	Forward Transconductance	--	6.5	--	Ω	V_{DS}=-40V,I_D=-5.5A ④
C_{iss}	Input Capacitance	--	1220	1585	pF	V_{GS}=0V,V_{DS}=-25V,f =1MHz ***See Fig 5***
C_{oss}	Output Capacitance	--	207	310		
C_{rss}	Reverse Transfer Capacitance	--	81	120		
$t_{d(on)}$	Turn-On Delay Time	--	16	40	ns	V_{DD}=-100V,I_D=-11A, R_G=9.1Ω ***See Fig 13*** ④ ⑤
t_r	Rise Time	--	23	55		
$t_{d(off)}$	Turn-Off Delay Time	--	54	115		
t_f	Fall Time	--	19	50		
Q_g	Total Gate Charge	--	46	59	nC	V_{DS}=-160V,V_{GS}=-10V, I_D=-11A ***See Fig 6 & Fig 12*** ④ ⑤
Q_{gs}	Gate-Source Charge	--	9.2	--		
Q_{gd}	Gate-Drain(" Miller ") Charge	--	22.9	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	-11	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	-44		
V_{SD}	Diode Forward Voltage ④	--	--	-5.0	V	T_J=25°C,I_S=-11A,V_{GS}=0V
t_{rr}	Reverse Recovery Time	--	180	--	ns	T_J=25°C,I_F=-11A di_F/dt=100A/μs ④
Q_{rr}	Reverse Recovery Charge	--	1.24	--	μC	

Notes ;

① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

② L=10mH, I_{AS}=-11A, V_{DD}=-50V, R_G=27Ω*, Starting T_J=25°C

③ I_{SD} ≤-11A, di/dt ≤450A/μs, V_{DD} ≤BV_{DSS}, Starting T_J=25°C

④ Pulse Test : Pulse Width = 250 μs, Duty Cycle ≤2%

⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

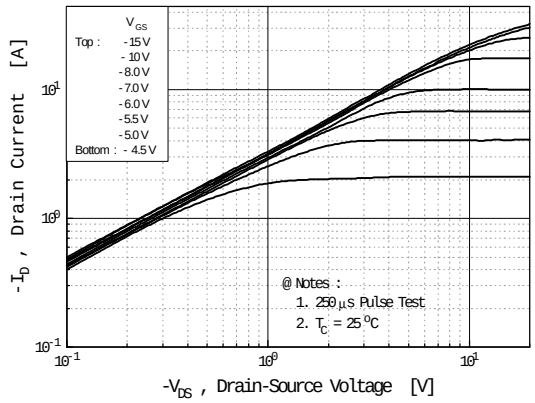


Fig 2. Transfer Characteristics

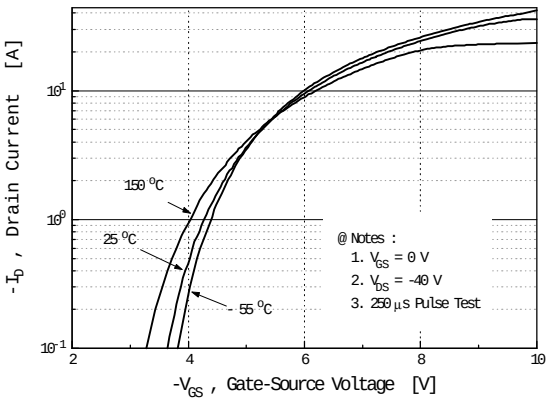


Fig 3. On-Resistance vs. Drain Current

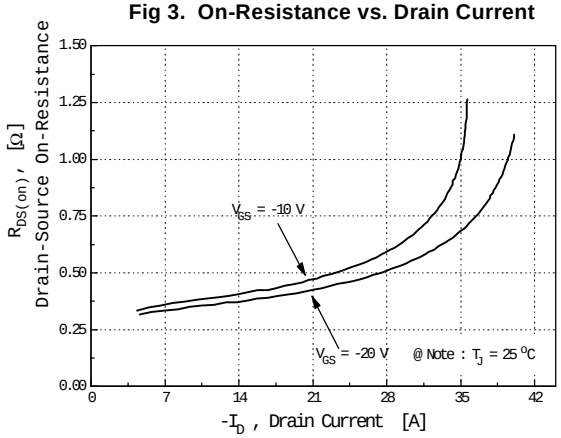


Fig 4. Source-Drain Diode Forward Voltage

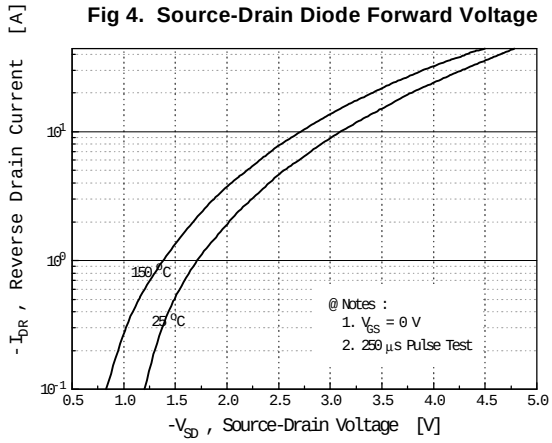


Fig 5. Capacitance vs. Drain-Source Voltage

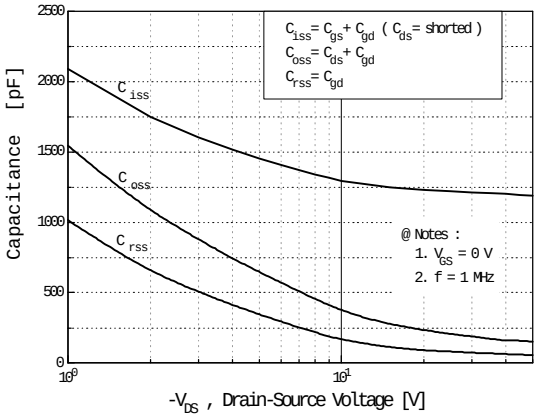


Fig 6. Gate Charge vs. Gate-Source Voltage

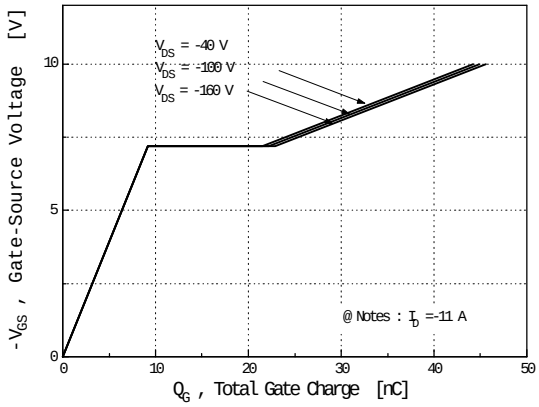


Fig 7. Breakdown Voltage vs. Temperature

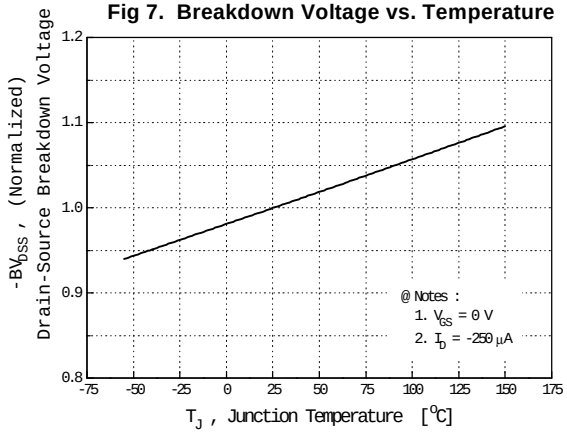


Fig 8. On-Resistance vs. Temperature

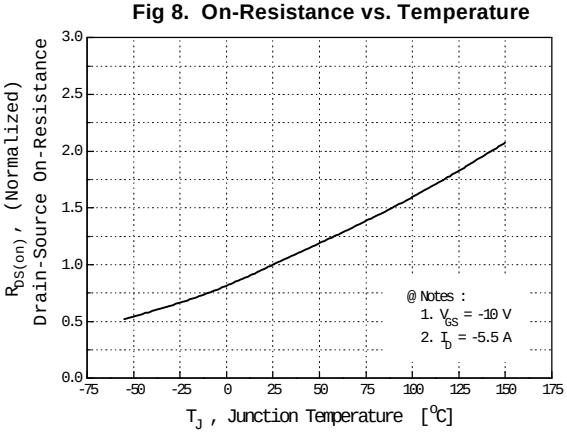


Fig 9. Max. Safe Operating Area

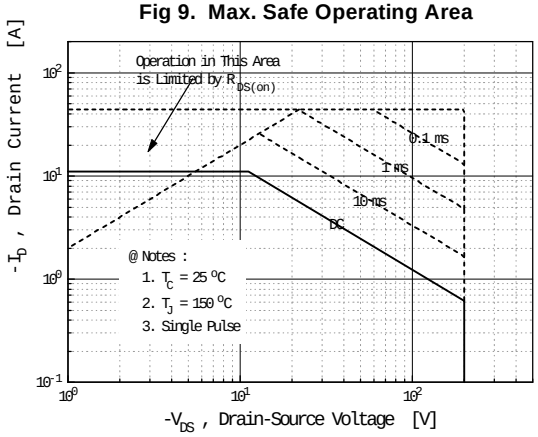


Fig 10. Max. Drain Current vs. Case Temperature

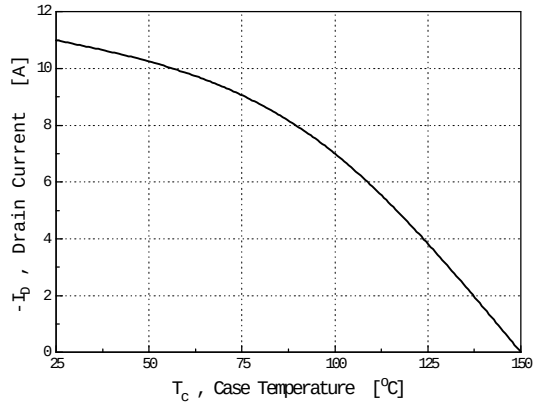


Fig 11. Thermal Response

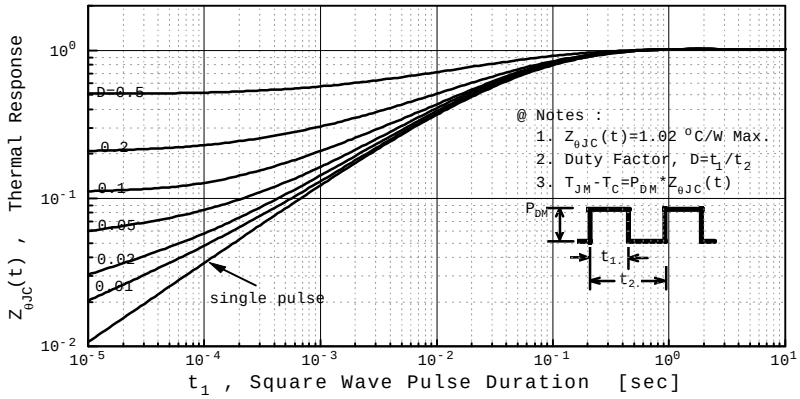


Fig 12. Gate Charge Test Circuit & Waveform

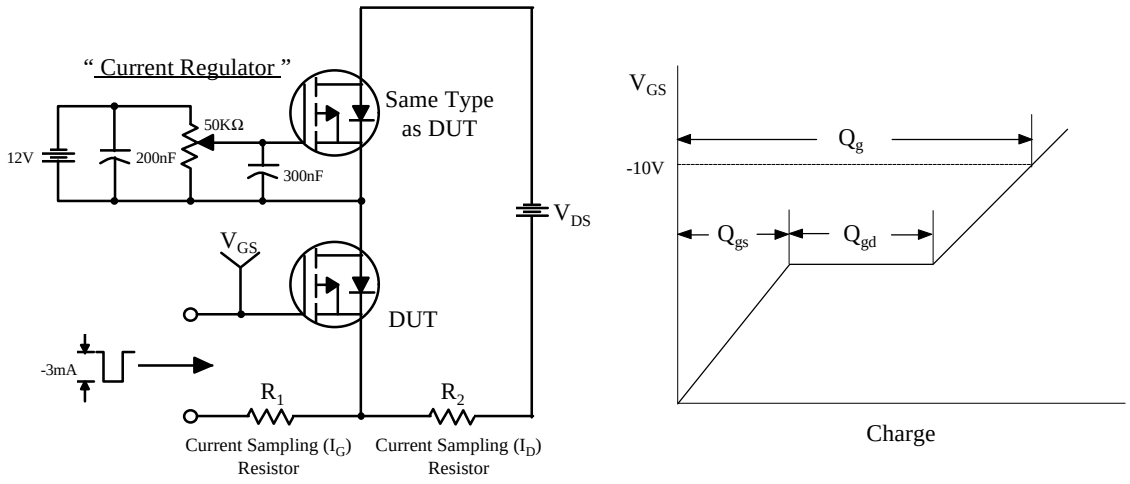


Fig 13. Resistive Switching Test Circuit & Waveforms

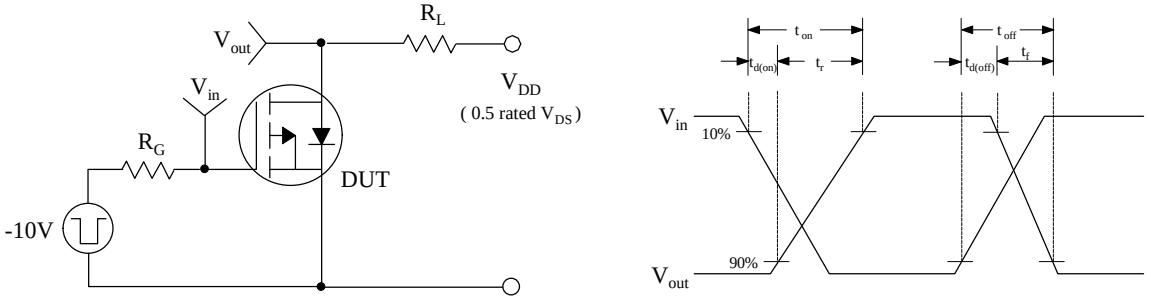


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

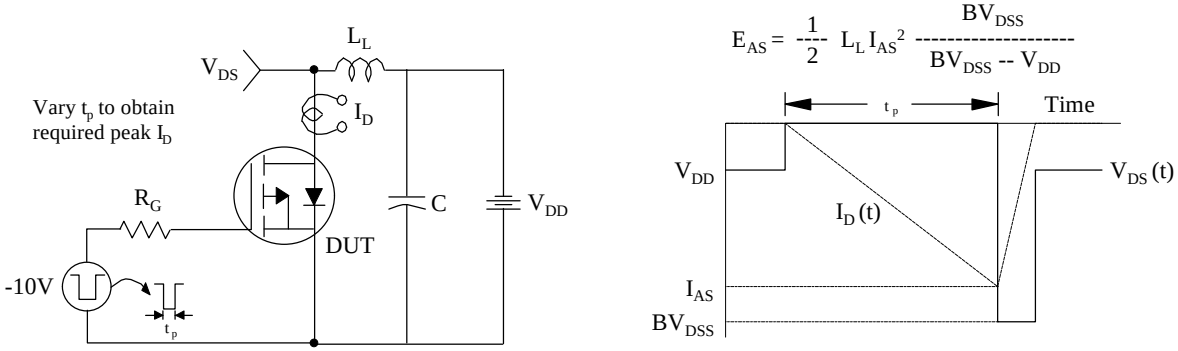
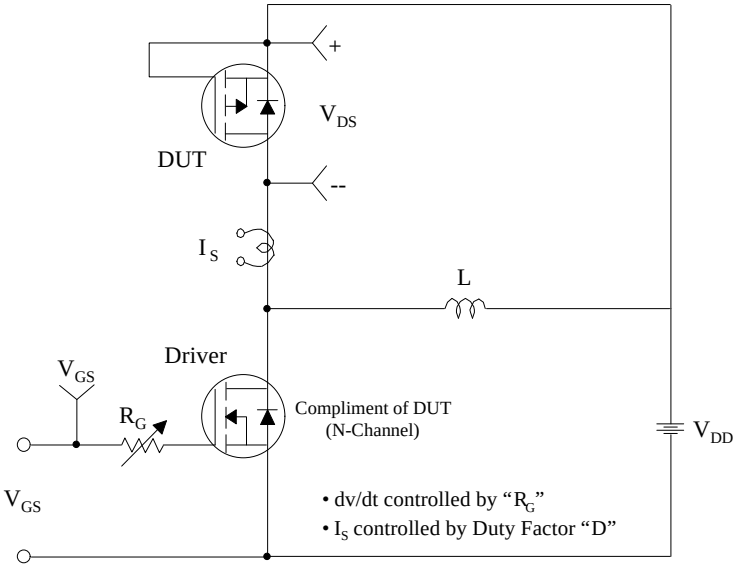
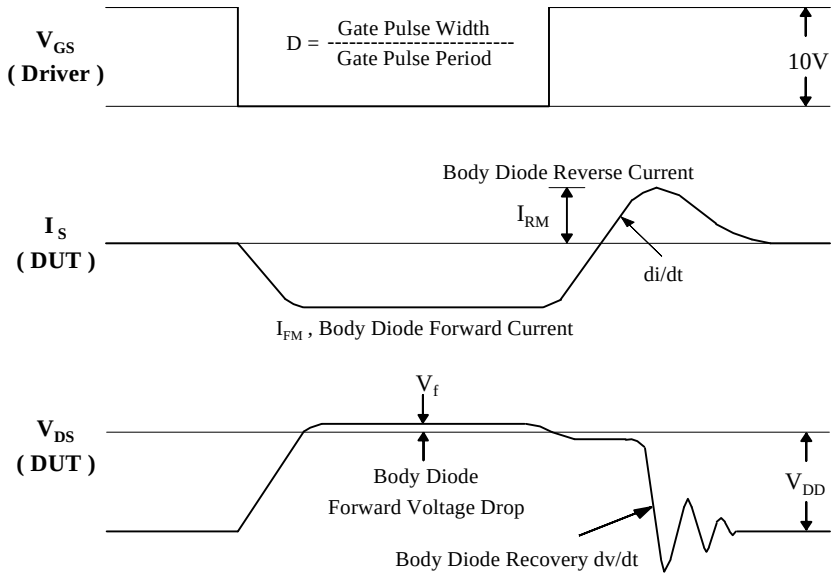


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





TRADEMARKS

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™
CoolFET™
CROSSVOLT™
E^2CMOS^{TM}
FACT™
FACT Quiet Series™
FAST®
FASTr™
GTO™
HiSeC™
ISOPLANAR™
MICROWIRE™
POP™
PowerTrench™
QS™
Quiet Series™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
TinyLogic™
UHC™
VCX™

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.
As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

SFW9640
200V P-Channel A-FET

Contents
Product status/pricing/packaging | Models

Datasheet
Download this datasheet
PDF

e-mail this datasheet
[E-

This page
Print version

Related Links

Request samples
How to order products
Product Change Notices (PCNs)
Support
Distributor and field sales representatives
Quality and reliability
Design tools

Product status/pricing/packaging

Product	Product status	Pricing*	Package type	Leads	Packing method
SFW9640TM	Full Production	$1.02	TO-263(D2PAK)	2	TAPE REEL

* 1,000 piece Budgetary Pricing

back to top

Models

Package & leads	Condition	Temperature range	Software version	Revision date
PSPICE				
TO-263(D2PAK)-2	Electrical	-55°C to 150°C	9.2	Mar 13, 2002

back to top

Home | Find products | Technical information | Buy products | Support | Company | Contact us | Site index | Privacy policy

SFI9640
200V P-Channel A-FET

Contents
Product status/pricing/packaging | Models

Datasheet
Download this datasheet

PDF

e-mail this datasheet

[E-

This page
Print version

Related Links

Request samples

Dotted line

How to order products

Dotted line

Product Change Notices (PCNs)

Dotted line

Support

Dotted line

Distributor and field sales representatives

Dotted line

Quality and reliability

Dotted line

Design tools

Product status/pricing/packaging

Product	Product status	Pricing*	Package type	Leads	Packing method
SFI9640TU	Full Production	$1.02	TO-262(I2PAK)	3	RAIL

* 1,000 piece Budgetary Pricing

back to top

Models

Package & leads	Condition	Temperature range	Software version	Revision date
PSPICE				
TO-262(I2PAK)-3	Electrical	-55°C to 150°C	9.2	Mar 13, 2002

back to top