193541 Rev. 040120

MOSEL 16K x 1 CMOS STATIC RAM MS 6167

January 1987

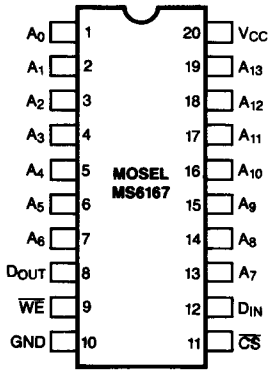
FEATURES

- High-speed—35/45/55/70ns
- Low Power dissipation
  150mW (Typ.) Operating
  100μW (Typ.) Standby
- Single 5V power supply
- Fully static operation
- Input and output directly TTL compatible
- Three state output
- Data retention supply voltage: 2.0–5.5V

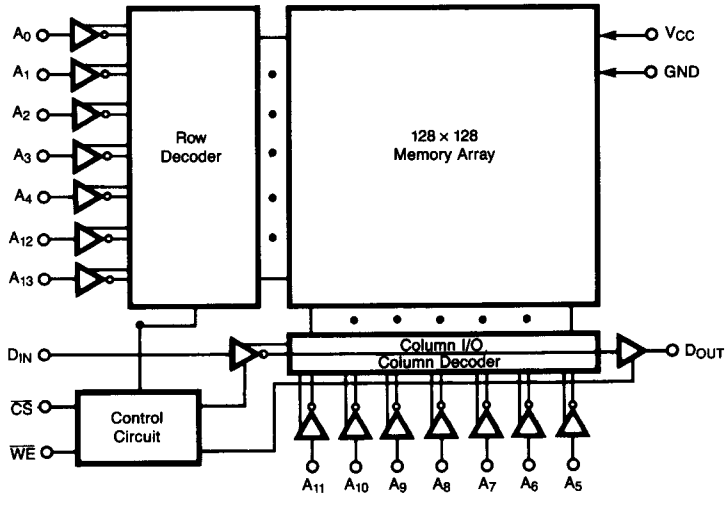
DESCRIPTION

The MOSEL MS6167 is a 16,384 bit static random access memory organized as 16,384 words by 1 bit and operates from a single 5 volt supply. It is built with MOSEL's high performance twin tub CMOS process. Input and three-state output are TTL compatible. The MS6167 is moulded in a standard 20-pin, 300 mil-DIP.

PIN CONFIGURATIONS



FUNCTIONAL BLOCK DIAGRAM



OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

PIN NAMES

A_0–A_{13}	ADDRESS INPUTS	D_{IN}	DATA IN
$\overline{CS}$	CHIP SELECT	D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE	GND	GROUND
V_{CC}	POWER		

S-RES Orig

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	VALUE	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	−0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	−10 to +125	°C
T_{STG}	Storage Temperature	−40 to +150	°C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS (T_A = 0 to +70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	−0.5	0	0.8	V

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MS6167 MIN.	MS6167 TYP.[1]	MS6167 MAX.	MS6167L MIN.	MS6167L TYP.[1]	MS6167L MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	—	2	—	—	2	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	—	2	—	—	2	µA
I_{CC1}	Operating Power Supply Current	$\overline{CS}$ = V_{IL}, $I_{I/O}$ = 0mA	—	25	45	—	25	45	mA
I_{CC2}	Dynamic Operating Current	Min. Duty Cycle = 100%	—	25	45	—	25	45	mA
I_{SB}	Standby Power Supply Current	$\overline{CS}$ ≥ V_{IH}	—	—	20	—	—	20	mA
I_{SB1}	Full Standby Power Supply Current	$\overline{CS}$ ≥ V_{CC}−0.2V V_{IN} ≥ V_{CC}−0.2V or V_{IN} ≤ 0.2V	—	0.02	2	—	0.002	0.05	mA
V_{OL}	Output Low Voltage	I_{OL} = 8mA	—	—	0.4	—	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = −4mA	2.4	—	—	2.4	—	—	V

1. V_{CC} = 5V, T_A = 25°C.

TRUTH TABLE

MODE	$\overline{CS}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	High Z	Standby
Read	L	H	D_{OUT}	Active
Write	L	L	High Z	Active

CAPACITANCE[1] (T_A = 25°C, f = 1.0MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

1. This parameter is sampled and not 100% tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

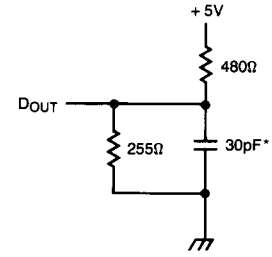


Figure 1. Output Load

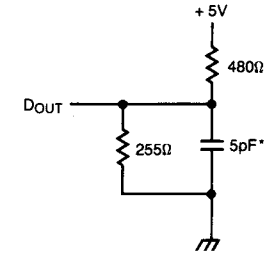


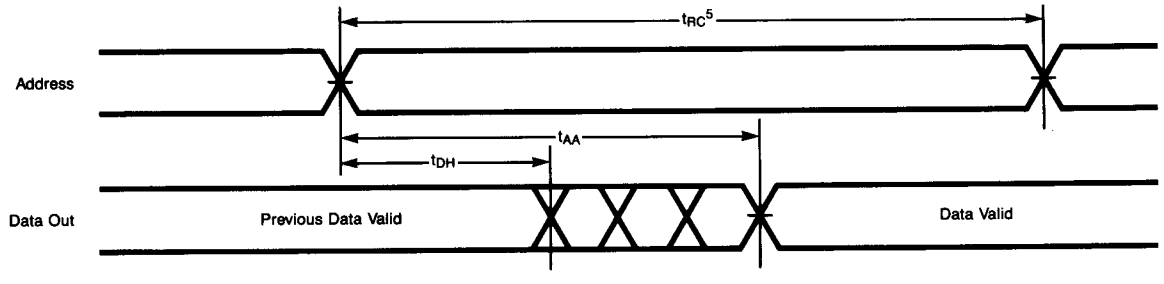
Figure 2. Output Load (for t_{HZ}, t_{LZ}, t_{WZ}, and t_{OW})

*Including scope and jig.

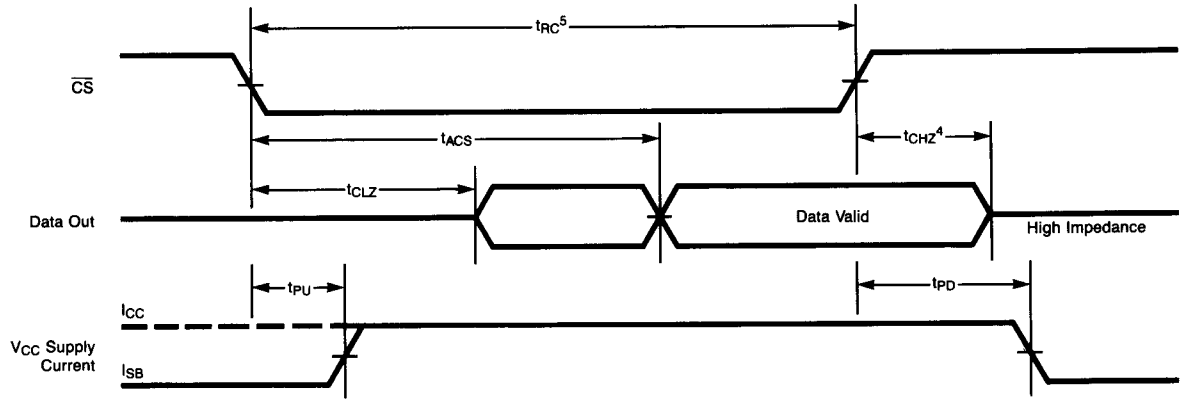
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5V ± 10%, T_A = 0 to +70°C, unless otherwise noted)

SYMBOL	PARAMETER	MS6167(L)-35 MIN.	MS6167(L)-35 MAX.	MS6167(L)-45 MIN.	MS6167(L)-45 MAX.	MS6167(L)-55 MIN.	MS6167(L)-55 MAX.	MS6167(L)-70 MIN.	MS6167(L)-70 MAX.	UNIT
READ CYCLE										
t_{RC}	Read Cycle Time	35	—	45	—	55	—	70	—	ns
t_{AA}	Address Access Time	—	35	—	45	—	55	—	70	ns
t_{ACS}	Chip Select Access Time	—	35	—	45	—	55	—	70	ns
t_{OH}	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
t_{CLZ}	Chip Selection to Output in Low Z	5	—	5	—	5	—	5	—	ns
t_{CHZ}	Chip Deselection to Output in High Z	0	25	0	30	0	30	0	35	ns
t_{PU}	Chip Selection to Power Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}	Chip Deselection to Power Down Time	—	25	—	35	—	35	—	40	ns
WRITE CYCLE										
t_{WC}	Write Cycle Time	35	—	45	—	55	—	70	—	ns
t_{CW}	Chip Selection to End of Write	35	—	40	—	45	—	55	—	ns
t_{AW}	Address Valid to End of Write	35	—	40	—	45	—	55	—	ns
t_{AS}	Address Setup Time	0	—	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	25	—	30	—	35	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End of Write	17	—	20	—	25	—	25	—	ns
t_{DH}	Data Hold Time	3	—	3	—	3	—	3	—	ns
t_{WHZ}	Write Enable to Output in High Z	0	13	0	20	0	25	0	25	ns
t_{OW}	Output Active from End of Write	0	30	0	35	0	35	0	35	ns

TIMING WAVEFORM OF READ CYCLE NO. 1[1,2]

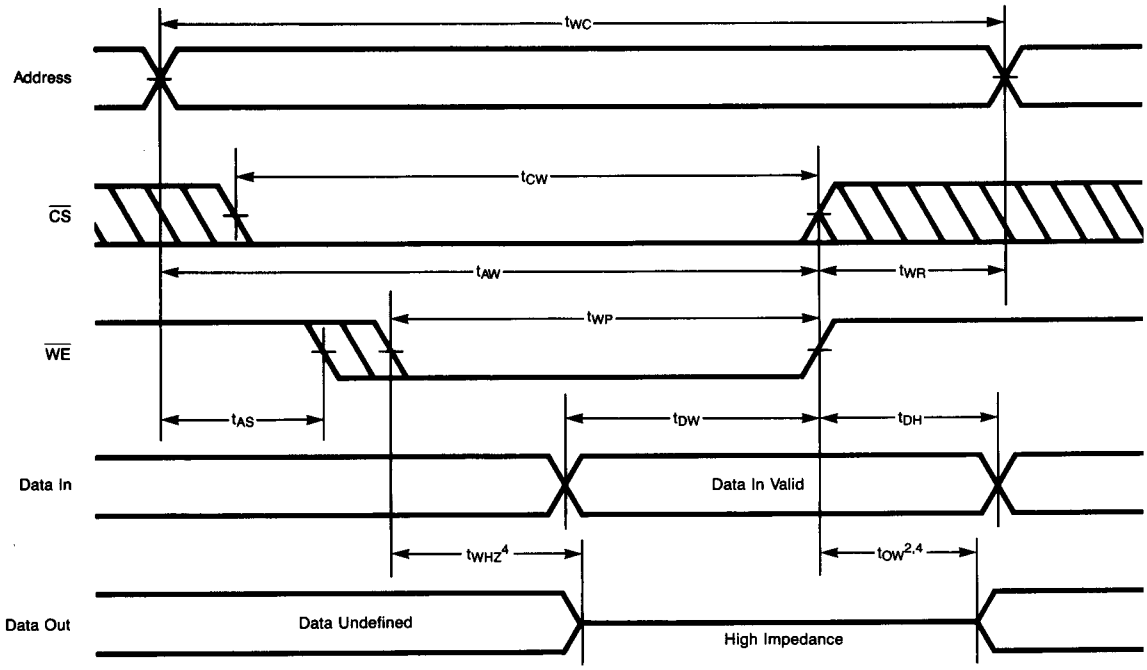


TIMING WAVEFORM OF READ CYCLE NO. 2[1,3]

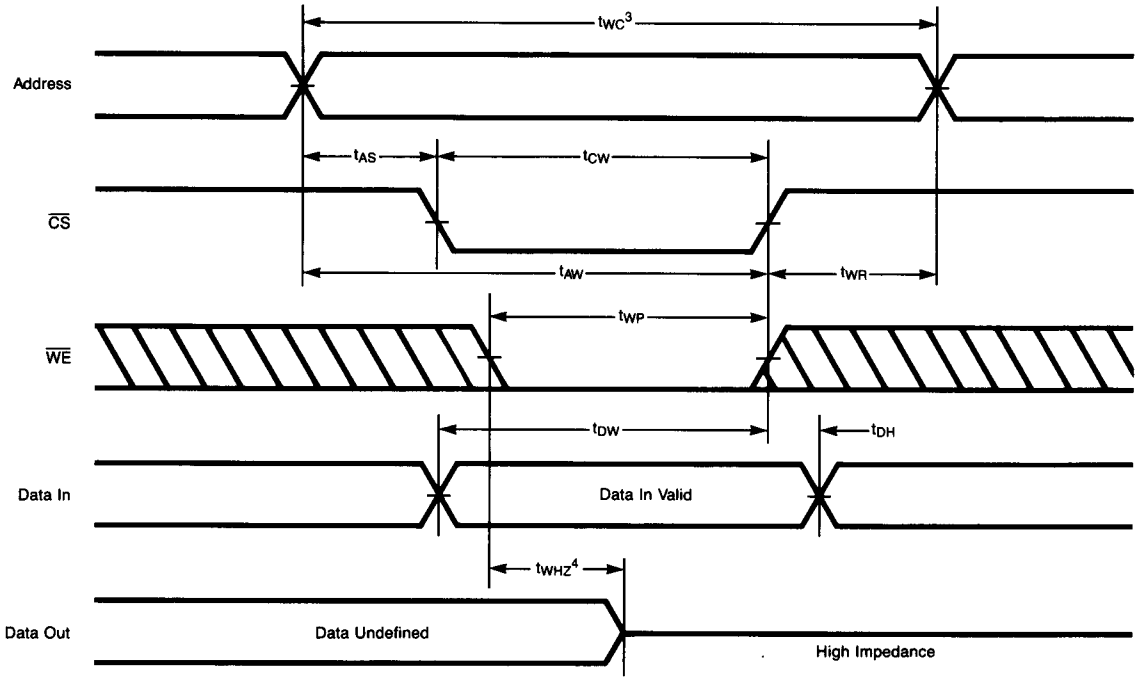


NOTES:
1. $\overline{WE}$ is high for READ cycle.
2. $\overline{CS}$ is low for READ cycle.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled, not 100% tested.
5. All READ cycle timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[1]



TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED)(1)



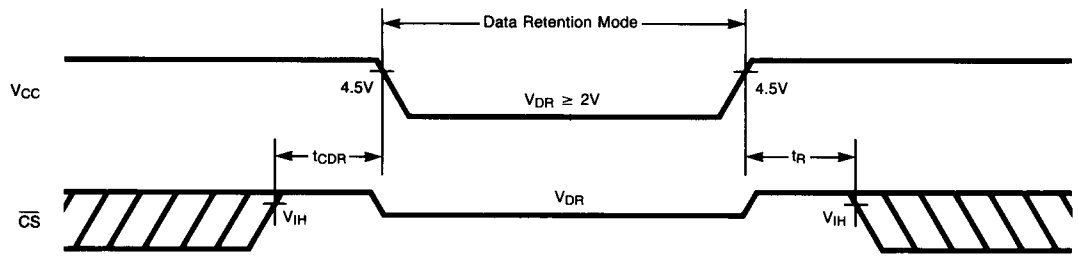
NOTES: 1. $\overline{CS}$ or $\overline{WE}$ must be high during address transitions.
2. If $\overline{CS}$ goes high simultaneously with $\overline{WE}$ high, the output remains in a high impedance state.
3. All write cycle timings are referenced from the last valid address to the first transitioning address.
4. Transition is measured ±500mV from steady state voltage with specified loading in Figure 2. This parameter is sampled and not 100% tested.

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.(1)	MAX.	UNIT
V_{DR}	V_{CC} for Data Retention		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	— —	0.5(2) 1.0(3)	20(2) 30(3)	µA
t_{CDR}	Chip Deselect to Data Retention Time		0	—	—	ns
t_R	Operation Recovery Time		t_{RC}(4)	—	—	ns

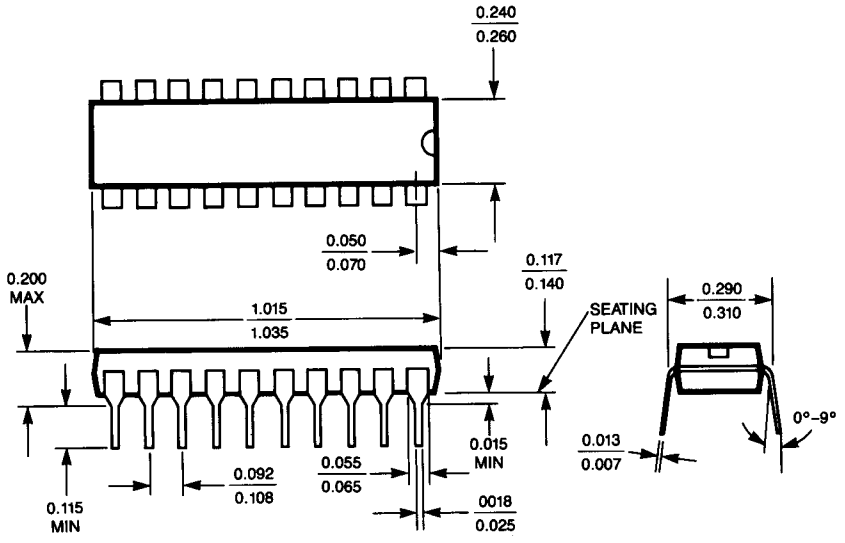
1. T_A = 25°C
2. at V_{CC} = 2V
3. at V_{CC} = 3V
4. t_{RC} = Read Cycle Time

LOW V_{CC} DATA RETENTION WAVEFORM



PACKAGE DIAGRAM

20 LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



ORDERING INFORMATION

SPEED (ns)	ORDERING CODE	PACKAGE	TEMP. RATING @
35	MS6167-35PDC	Plastic DIP	0°C to +70°C
35	MS6167L-35PDC	Plastic DIP	0°C to +70°C
45	MS6167-45PDC	Plastic DIP	0°C to +70°C
45	MS6167L-45PDC	Plastic DIP	0°C to +70°C
55	MS6167-55PDC	Plastic DIP	0°C to +70°C
55	MS6167L-55PDC	Plastic DIP	0°C to +70°C
70	MS6167-70PDC	Plastic DIP	0°C to +70°C
70	MS6167L-70PDC	Plastic DIP	0°C to +70°C
45	MS6167-45SDM	Sidebraze DIP	−55°C to +125°C
55	MS6167-55SDM	Sidebraze DIP	−55°C to +125°C
70	MS6167-70SDM	Sidebraze DIP	−55°C to +125°C

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