QUALITY SEMICONDUCTOR, INC.

# High Speed CMOS 3.3V 16-Bit Bus Register Transceiver

QS74FCT163952

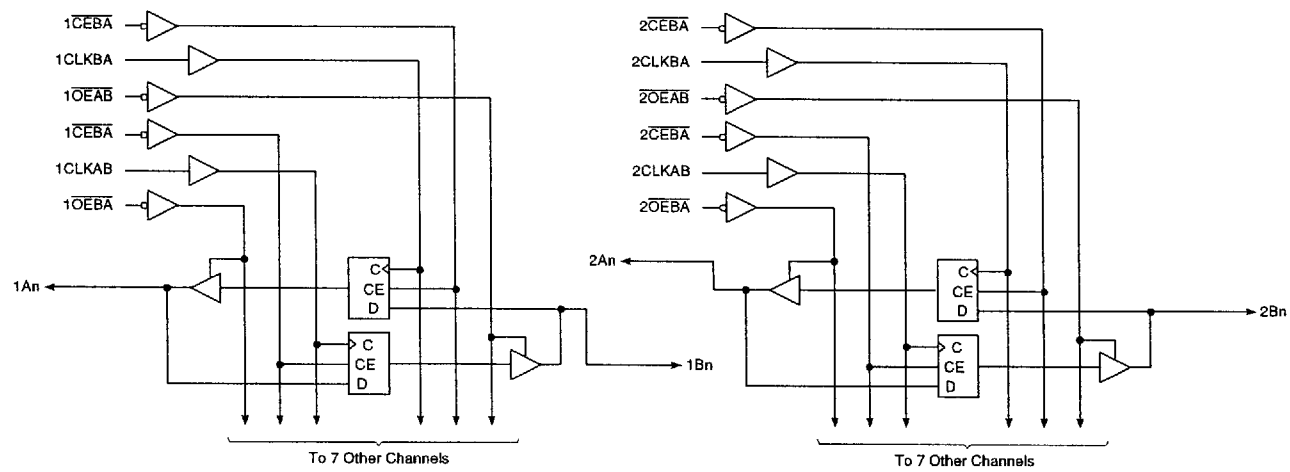
## FEATURES/BENEFITS

- Pin and function compatible with T.I. Widebus™ and IDT Double-Density™ families
- CMOS power levels: <1μW typical standby
- SSOP (PV) and TSSOP (PA) packages
- Low output skew: 0.5ns $t_{SK(O)}$
- Flow-through pinout for easy layout
- Extended commercial temperature: –40°C to +85°C
- Extended 3.3V supply range 2.7V to 3.6V
- JEDEC compatible LVTTL output levels for 3.3V
- Input hysteresis for noise immunity
- Multiple power and ground pins for low noise
- A and C speed grades: 6.3ns $t_{PD}$ for C
- 5V tolerant inputs for 5V to 3.3V translation

## DESCRIPTION

The FCT163952 is a 16-bit bus register transceiver with three-state outputs that is ideal for driving address and data buses. Two independent 8-bit registered transceivers are used to permit independent control of data flow in either direction. Easy board layout is facilitated by the use of flow-through pinouts and byte enable controls provide architectural flexibility for systems designers. All outputs have ground bounce suppression circuitry (See QSI Application Note AN-01). Multiple power and ground pins result in low ground and $V_{CC}$ bounce. This JEDEC LVTTL compliant 3.3V device is useful for 5V to 3.3V applications since all inputs will support 5V signals.

## Figure 1. Functional Block Diagram



## Figure 2. Pin Configuration

(All Pins Top View)

### SSOP, TSSOP

| | | | |
|---|---|---|---|
| $1\overline{OEAB}$ | 1 | 56 | $1\overline{OEBA}$ |
| 1CLKAB | 2 | 55 | 1CLKBA |
| $1\overline{CEAB}$ | 3 | 54 | $1\overline{CEBA}$ |
| GND | 4 | 53 | GND |
| 1A1 | 5 | 52 | 1B1 |
| 1A2 | 6 | 51 | 1B2 |
| $V_{CC}$ | 7 | 50 | $V_{CC}$ |
| 1A3 | 8 | 49 | 1B3 |
| 1A4 | 9 | 48 | 1B4 |
| 1A5 | 10 | 47 | 1B5 |
| GND | 11 | 46 | GND |
| 1A6 | 12 | 45 | 1B6 |
| 1A7 | 13 | 44 | 1B7 |
| 1A8 | 14 | 43 | 1B8 |
| 2A1 | 15 | 42 | 2B1 |
| 2A2 | 16 | 41 | 2B2 |
| 2A3 | 17 | 40 | 2B3 |
| GND | 18 | 39 | GND |
| 2A4 | 19 | 38 | 2B4 |
| 2A5 | 20 | 37 | 2B5 |
| 2A6 | 21 | 36 | 2B6 |
| $V_{CC}$ | 22 | 35 | $V_{CC}$ |
| 2A7 | 23 | 34 | 2B7 |
| 2A8 | 24 | 33 | 2B8 |
| GND | 25 | 32 | GND |
| $2\overline{CEAB}$ | 26 | 31 | $2\overline{CEBA}$ |
| 2CLKAB | 27 | 30 | 2CLKBA |
| $2\overline{OEAB}$ | 28 | 29 | $2\overline{OEBA}$ |

## Table 1. Pin Description

| Name | Description |
|---|---|
| $x\overline{OEAB}$ | A to B Output Enable Inputs (Active LOW) |
| $x\overline{OEBA}$ | B to A Output Enable Inputs (Active LOW) |
| $x\overline{CEAB}$ | A to B Enable Inputs (Active LOW) |
| $x\overline{CEBA}$ | B to A Enable Inputs (Active LOW) |
| xCLKAB | A to B Clock Inputs |
| xCLKBA | B to A Clock Inputs |
| xAx | A to B Data Inputs or B to A 3-State Outputs |
| xBx | B to A Data Inputs or A to B 3-State Outputs |

## Table 2. Function Table [1, 2]

| Inputs | | | | Outputs |
|---|---|---|---|---|
| $x\overline{CEAB}$ | xCLKAB | $x\overline{OEAB}$ | xAx | xBx |
| H | X | L | X | B[3] |
| X | L | L | X | B[3] |
| L | ↑ | L | L | L |
| L | ↑ | L | H | H |
| X | X | H | X | Z |

**Notes:**

1. ↑ = LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. A-to-B data flow shown: B-to-A flow control is the same, except using $x\overline{CEBA}$, xCLKBA, and $x\overline{OEBA}$.
3. Level of B before the indicated steady-state input conditions were established.

## Table 3. Capacitance

$T_A$ = 25°C, f = 1MHz, $V_{IN}$ = 0V, $V_{OUT}$ = 0V

| Symbol | Parameter | Typ | Unit |
|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 7.0 | pF |
| $C_{OUT}$ | Output Capacitance | 8.0 | pF |

**Note:** Capacitance is characterized but not production tested.

## Table 4. Absolute Maximum Ratings

Supply Voltage to Ground ..... –0.5V to +4.6V
DC Output Voltage $V_{OUT}$ ..... –0.5V to $V_{CC}$ +0.5V
DC Input Voltage $V_{IN}$ ..... –0.5V to +7.0V
AC Input Voltage (for a pulse width ≤ 20ns) ..... –3.0V
DC Input Diode Current with $V_{IN} < 0$ ..... –20mA
DC Output Diode Current with $V_{OUT} < 0$ ..... –50mA
DC Output Current Max. Sink Current/Pin ..... 120mA
$T_{STG}$ Storage Temperature ..... –65° to +150°C

**Note:** Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to this device resulting in functional or reliability type failures.

## Table 5. Recommended Operating Conditions

| Symbol | | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 2.7 | 3.6 | V |
| $V_{IN}$ | Input Voltage | –0.5 | 5.5 | V |
| $V_{OUT}$ | Voltage Applied to Output or I/O | 0 | $V_{CC}$ | V |
| $\Delta t/\Delta v$ | Input Transition Slew Rate | — | 10 | ns/V |
| $T_A$ | Operating Free Air Temperature | –40 | +85 | °C |

## Table 6. DC Electrical Characteristics Over Operating Range

Recommended Operating Ranges apply unless otherwise noted.

| Symbol | Parameter | Test Conditions[1] | | Min | Typ[2] | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Logic HIGH for All Inputs | | 2.0 | — | 5.5 | V |
| $V_{IL}$ | Input LOW Voltage | Logic LOW for All Inputs | | –0.5 | — | 0.8 | V |
| $\Delta V_T$ | Input Hysteresis[4] | $V_{TLH} - V_{THL}$ for All Inputs | | — | 150 | — | mV |
| $\lvert I_{IH} \rvert$ | Input HIGH Current (Input pins) | $V_{CC}$ = Max. | $V_I$ = 5.5V | — | — | 1 | µA |
| | Input HIGH Current (I/O pins) | | $V_I = V_{CC}$ | — | — | 1 | |
| $\lvert I_{IL} \rvert$ | Input LOW Current (Input pins) | $V_{CC}$ = Max. | $V_I$ = GND | — | — | 1 | µA |
| | Input LOW Current (I/O pins) | | $V_I$ = GND | — | — | 1 | |
| $\lvert I_{OZ} \rvert$ | Off-State Output Current (Hi-Z) | $V_{CC}$ = Max., $V_{OUT}$ = 0V, $V_{OUT}$ = VCC | | — | — | 1 | µA |
| $I_{OS}$ | Short Circuit Current[3,4] | $V_{CC}$ = Max., $V_{OUT}$ = GND | | –60 | –140 | –240 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = 2.7V<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –0.1mA<br>$I_{OH}$ = –3.0mA | $V_{CC}$ –0.2<br>2.4 | —<br>— | —<br>— | V |
| | | $V_{CC}$ = 3.0V<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –8mA | 2.4 | — | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = 2.7V<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 0.1mA<br>$I_{OL}$ = 16mA<br>$I_{OL}$ = 24mA | —<br>—<br>— | —<br>—<br>— | 0.2<br>0.4<br>0.55 | V |
| | | $V_{CC}$ = 3.0V<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 24mA | — | — | 0.5 | V |
| $V_{IK}$ | Input Clamp Voltage[4] | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |

**Notes:**

1. For conditions shown as Max or Min use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values indicate $V_{CC}$ = 3.3V and $T_A$ = 25°C.
3. Not more than one output should be shorted at one time. Duration of test should not exceed one second.
4. These parameters are guaranteed by design but not production tested.

## Table 7. Power Supply Characteristics

| Symbol | Parameter | Test Conditions[1] | | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power Supply Current | $V_{CC}$ = 3.6V, Freq = 0, $V_{IN}$ = GND or $V_{CC}$ | | 0.1 | 10 | µA |
| $\Delta I_{CC}$ | Supply Current per Input @ TTL HIGH | $V_{CC}$ = 3.6V, $V_{IN}$ = $V_{CC}$ –0.6V | | 2.0 | 30 | µA |
| $I_{CCD}$ | Supply Current per Input per MHz[4] | $V_{CC}$ = 3.6V, Outputs Open<br>One Bit Toggling<br>@ 50% Duty Cycling<br>x$\overline{OE}$ = GND | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | 65 | 100 | µA/ MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = 3.6V, Outputs Open<br>One Bit Toggling<br>@ 50% Duty Cycle<br>f = 5MHz,<br>$f_{CP}$ = 10MHz (xCLKAB)<br>x$\overline{OEAB}$ = x$\overline{CEAB}$ = GND<br>x$\overline{OEBA}$ = $V_{CC}$ | $V_{IN}$ = $V_{CC}$ –0.6V<br>$V_{IN}$ = GND | 0.4[5] | 0.6[5] | mA |
| | | $V_{CC}$ = 3.6V, Outputs Open<br>Sixteen Bits Toggling<br>@ 50% Duty Cycling<br>f = 2.5MHz,<br>$f_{CP}$ = 10MHz (xCLKAB)<br>x$\overline{OEAB}$ = x$\overline{CEAB}$ = GND<br>x$\overline{OEBA}$ = $V_{CC}$ | $V_{IN}$ = $V_{CC}$ –0.6V<br>$V_{IN}$ = GND | 2.1[5] | 3.4[5] | mA |

**Notes:**

1. For conditions shown as Min. or Max. use the appropriate value specified under Recommended Operating Conditions for the applicable device type.
2. Typical values are at $V_{CC}$ = 3.3V, +25°C ambient.
3. Per TTL driven input. All other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the $I_{CC}$ formula. These limits are guaranteed by design but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$.
   $I_C = I_{CCQ} + \Delta I_{CC} D_H N_T + I_{CCD} f N_O$.
   $I_{CCQ}$ = Quiescent Current ($I_{CCL}$, $I_{CCH}$, and $I_{CCZ}$).
   $\Delta I_{CC}$ = Power Supply Current for a TTL-High Input ($V_{IN}$ = $V_{CC}$ –0.6V).
   $D_H$ = Duty Cycle for TTL High Inputs.
   $N_T$ = Number of TTL High Inputs.
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL).
   f = Average Switching Frequency per Output.
   $N_O$ = Number of Outputs Switching.

**Note:** 1. Characterized but not production tested.

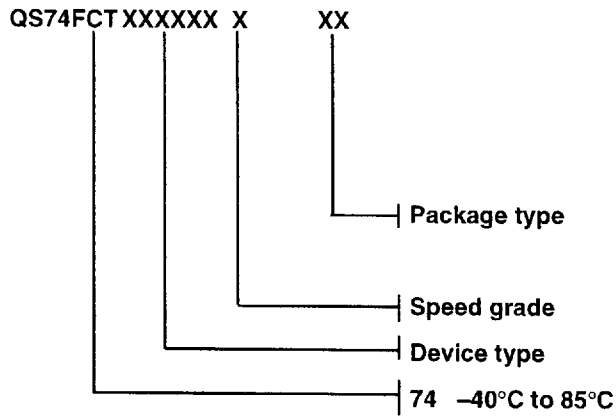
## Table 8. Switching Characteristics Over Operating Range

Recommende operating ranges apply unless otherwise noted.
$C_{LOAD}$ = 50pF, $R_{LOAD}$ = 500Ω unless otherwise noted.

| Symbol | Description[1] | FCT163952A | | FCT163952C | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{PHL}$<br>$t_{PLH}$ | Propagation Delay<br>xCLKAB, xCLKBA to xAx, xBx | 2.0 | 10.0 | 2.0 | 6.3 | ns |
| $t_{PZH}$<br>$t_{PZL}$ | Output Enable Time<br>x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx | 1.5 | 10.5 | 1.5 | 7.0 | ns |
| $t_{PHZ}$<br>$t_{PLZ}$ | Output Disable Time[2]<br>x$\overline{OEBA}$, x$\overline{OEAB}$ to xAx, xBx | 1.5 | 10.0 | 1.5 | 6.5 | ns |
| $t_{SU}$ | Setup Time HIGH or LOW<br>xAx, xBx to xCKLAB, xCKLBA | 2.5 | — | 2.5 | — | ns |
| $t_H$ | Hold Time HIGH or LOW<br>xAx, xBx to xCLKAB, xCLKBA | 2.0 | — | 1.5 | — | ns |
| $t_{SU}$ | Setup Time HIGH or LOW<br>x$\overline{CEBA}$, x$\overline{CEAB}$ to xCLKAB, xCLKBA | 3.0 | — | 3.0 | — | ns |
| $t_H$ | Setup Time HIGH or LOW<br>x$\overline{CEBA}$, x$\overline{CEAB}$ to xCLKAB, xCLKBA | 2.0 | — | 2.0 | — | ns |
| $t_W$ | Pulse Width LOW<br>xCLKAB to xCLKBA[2] | 3.0 | — | 3.0 | — | ns |
| $t_{SK(O)}$ | Output Skew[3] | — | 0.5 | — | 0.5 | ns |

**Notes:**
1. Minimums guaranteed but not tested on propagation delays. See Test Circuit and Waveforms.
2. Switching characteristics are with $V_{CC}$ = 3.3V ± 0.3V. For 2.7V $V_{CC}$ operation, parameters should be degraded by 20%.
3. Guaranteed by design, but not production tested.
4. Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by characterization but not production tested.

## ORDERING INFORMATION



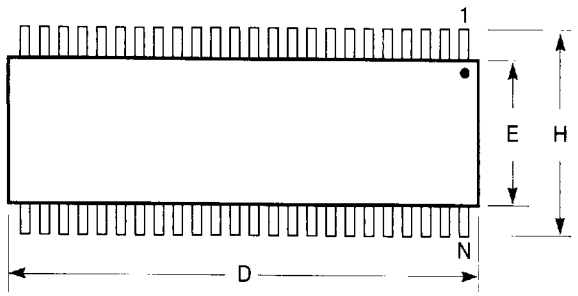

**Device Type:**
163952

**Speed Grades:**
A
C

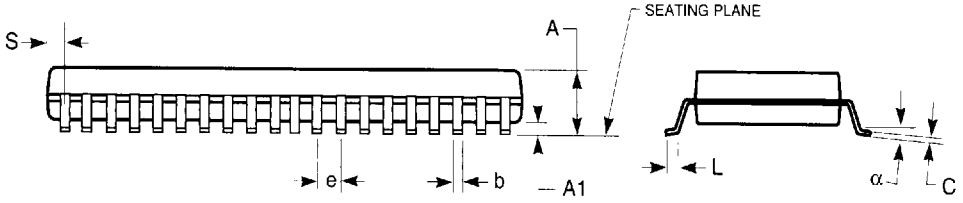
**Package Type:**
PV – SSOP, 300 mil
PA – TSSOP, 240 mil

## 300-MIL SSOP - Package Code PV

**Shrink Small Outline Package**
**Plastic Small Outline Gull-Wing**




**Notes:**
1. Refer to applicable symbol list.
2. All dimensions are in inches.
3. N is the number of lead positions.
4. Dimensions D and E are to be measured at maximum material condition but do not include mold flash. Allowable mold flash is 0.006 in. per side.
5. Lead coplanarity is 0.004 in. maximum.




| JEDEC# | MO-118AA | | | MO-118AB | | |
|---|---|---|---|---|---|---|
| DWG# | PSS-48B | | | PSS-56B | | |
| Symbol | Min | Nom | Max | Min | Nom | Max |
| A | 0.095 | 0.102 | 0.110 | 0.095 | 0.102 | 0.110 |
| A1 | 0.008 | 0.012 | 0.016 | 0.008 | 0.012 | 0.016 |
| b | 0.008 | 0.010 | 0.0135 | 0.008 | 0.010 | 0.0135 |
| C | 0.005 | 0.008 | 0.010 | 0.005 | 0.008 | 0.010 |
| D | 0.620 | 0.625 | 0.630 | 0.720 | 0.725 | 0.730 |
| E | 0.291 | 0.295 | 0.299 | 0.291 | 0.295 | 0.299 |
| e | 0.025 BSC | | | 0.025 BSC | | |
| H | 0.395 | 0.410 | 0.420 | 0.395 | 0.410 | 0.420 |
| L | 0.020 | 0.030 | 0.040 | 0.020 | 0.030 | 0.040 |
| N | 48 | | | 56 | | |
| α | 0° | 5° | 8° | 0° | 5° | 8° |
| S | 0.022 | 0.025 | 0.028 | 0.022 | 0.025 | 0.028 |