

## 128Kx8 Bit Low Voltage Operating Static RAM

### FEATURES

- Fast Access Time : 70,100ns(max.)
- Low Power Dissipation
  - Standby(CMOS) : 132 $\mu$ W(max.)L-Version
  - : 33 $\mu$ W(max.)LL-Version
  - Operating : 132mW(max.)
- Single 2.7V ~ 3.3V Power Supply
- TTL compatible inputs and outputs
- Fully Static Operation
  - No clock or refresh required
- Three State Output
- Battery Back-up Operation
  - 2V(min.) Data Retention
- Standard Pin Configuration
  - KM68U1000BLG/BLG-L: 32 pin-SOP (525mil)
  - KM68U1000BLT/BLT-L : 32 pin-TSOP (Standard Type)
  - KM68U1000BLR/BLR-L: 32 pin-TSOP (Reverse Type)

### GENERAL DESCRIPTION

The KM68U1000BL/BL-L is a 1,048,576-bit high speed Static Random Access Memory organized as 131,072 words by 8 bits.

The device is fabricated using Samsung's advanced CMOS process.

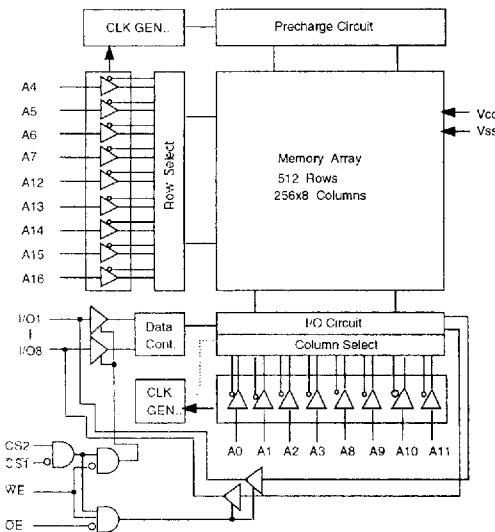
The KM68U1000BL/BL-L has an output enable input for precise control of the data outputs.

It also has chip enable inputs for the minimum current power down mode.

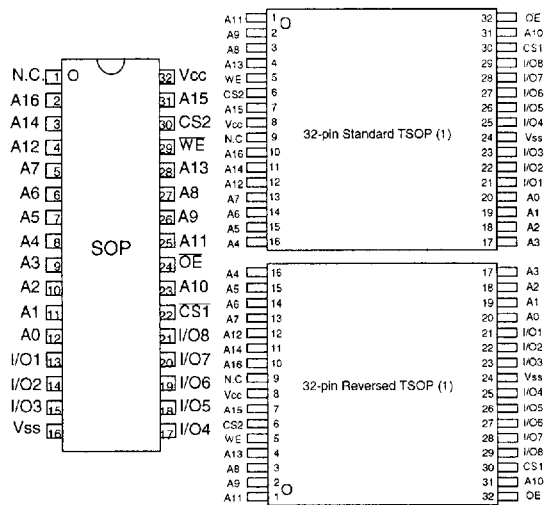
The KM68U1000BL/BL-L has been designed for high speed and low power applications.

It is particularly well suited for low voltage(2.7 ~ 3.3V) operation and battery back-up application.

### FUNCTIONAL BLOCK DIAGRAM



### PIN CONFIGURATION(TOP VIEW)



Pin Name	Pin Function
A0-A16	Address Inputs
WE	Write Enable Input
CS1, CS2	Chip Select Input
OE	Output Enable Input
I/O1-I/O8	Data Inputs/Outputs
Vcc	Power(2.7 ~ 3.3V)
Vss	Ground
N.C	No Connection

**ABSOLUTE MAXIMUM RATINGS \***

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss	V <sub>IN,OUT</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Voltage on Vcc Supply Relative to Vss	V <sub>CC</sub>	-0.5 to 4.6	V
Power Dissipation	P <sub>D</sub>	0.7	W
Storage Temperature	T <sub>stg</sub>	-55 to 150	°C
Operating Temperature	T <sub>A</sub>	0 to 70	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS** (T<sub>A</sub>= 0 to 70 °C)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V <sub>CC</sub>	2.7	3.0	3.3	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.2	-	V <sub>CC</sub> +0.3	V
Input Low Voltage	V <sub>IL</sub>	-0.3*	-	0.4	V

\* V<sub>IL</sub>(Min.)= -3.0V for ≤50 ns Pulse

**DC AND OPERATING CHARACTERISTICS**

(T<sub>A</sub>= 0 to 70°C, V<sub>CC</sub>=2.7 ~ 3.3V, unless otherwise specified)

Item	Symbol	Test Condition	Min.	* Typ	Max.	Unit	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Output Leakage Current	I <sub>LO</sub>	$\overline{CS1}=V_{IH}$ or CS2=V <sub>IL</sub> or WE=V <sub>IL</sub> , V <sub>IO</sub> =V <sub>SS</sub> to V <sub>CC</sub>	-1	-	1	μA	
Operating Power Supply Current	I <sub>CC</sub>	$\overline{CS1}=V_{IL}$ , CS2= V <sub>IH</sub> V <sub>IN</sub> =V <sub>IL</sub> or V <sub>IH</sub> , I <sub>IO</sub> =0mA	-	2	5	mA	
Average Operating Current	I <sub>CC 1</sub>	Cycle Time=1μs, 100% Duty, $\overline{CS1} \leq 0.2V$ , CS2≥V <sub>CC</sub> -0.2V, I <sub>IO</sub> =0mA	-	3	5	mA	
	I <sub>CC 2</sub>	Min. Cycle, 100% Duty $\overline{CS1}=V_{IL}$ , CS2=V <sub>IH</sub> , I <sub>IO</sub> =0mA	-	30	40	mA	
Standby Power Supply Current	I <sub>SB</sub>	$\overline{CS1}=V_{IH}$ or CS2=V <sub>IL</sub>	-	-	0.3	mA	
	I <sub>SB1</sub>	$\overline{CS1} \geq V_{CC}-0.2V$ CS2≥V <sub>CC</sub> -0.2V or CS2≤0.2V	L	-	1	50	μA
			L-L	-	0.5	15	μA
Output Low Voltage	V <sub>OL</sub>	I <sub>ol</sub> =2.1 mA	-	-	0.4	V	
Output High Voltage	V <sub>OH</sub>	I <sub>oh</sub> =-1.0 mA	2.2	-	-	V	

\* Typ; V<sub>CC</sub>=3.0V, T<sub>A</sub>=25°C



**CAPACITANCE** \* (f=1MHz, TA=25 °C)

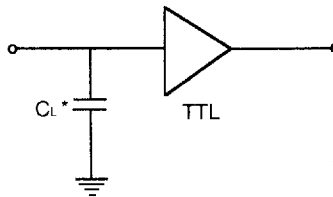
Item	Symbol	Test Condition	Min.	Max.	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	-	8	pF

\* Note: Capacitance is sampled and not 100% tested.

**TEST CONDITIONS**

(TA= 0 to 70°C, V<sub>CC</sub>=2.7 ~ 3.3V, unless otherwise specified.)

Parameter	Value
Input Pulse Level	0.4 to 2.2V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> =100pF+1TTL Load



\* Including Scope and Jig Capacitance

**READ CYCLE**

Parameter	Symbol	KM68U1000BL-7 KM68U1000BL-7L		KM68U1000BL-10 KM68U1000BL-10L		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	t <sub>RC</sub>	70	-	100	-	ns
Address Access Time	t <sub>AA</sub>	-	70	-	100	ns
Chip Select to Output	t <sub>CO1</sub> , t <sub>CO2</sub>	-	70	-	100	ns
Output Enable to Valid Output	t <sub>OE</sub>	-	35	-	50	ns
Chip Select to Low-Z Output	t <sub>LZ1</sub> , t <sub>LZ2</sub>	10	-	10	-	ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	5	-	5	-	ns
Chip Disable to High-Z Output	t <sub>HZ1</sub> , t <sub>HZ2</sub>	0	25	0	30	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	25	0	30	ns
Output Hold from Address Change	t <sub>OH</sub>	10	-	15	-	ns

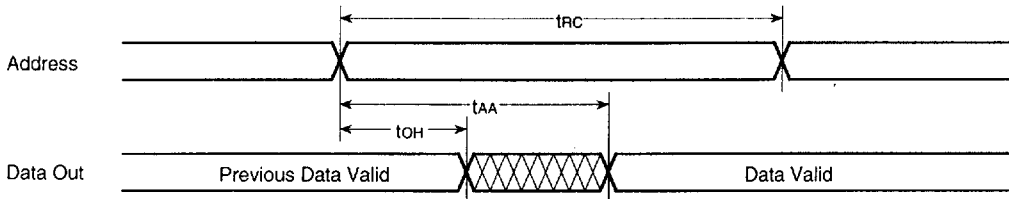
**WRITE CYCLE**

Farameter	Symbol	KM68U1000BL-7 KM68U1000BL-7L		KM68U1000BL-10 KM68U1000BL-10L		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	t <sub>wc</sub>	70	-	100	-	ns
Chip Select to End of Write	t <sub>cw</sub>	60	-	80	-	ns
Address Set-up Time	t <sub>as</sub>	0	-	0	-	ns
Address Valid to End of Write	t <sub>aw</sub>	60	-	80	-	ns
Write Pulse Width	t <sub>wp</sub>	55	-	70	-	ns
Write Recovery Time	t <sub>wr</sub>	0	-	0	-	ns
Write to Output High-Z	t <sub>whz</sub>	0	25	0	30	ns
Data to Write Time Overlap	t <sub>dw</sub>	30	-	40	-	ns
Data Hold from Write Time	t <sub>dh</sub>	0	-	0	-	ns
End Write to Output Low-Z	t <sub>ow</sub>	5	-	5	-	ns

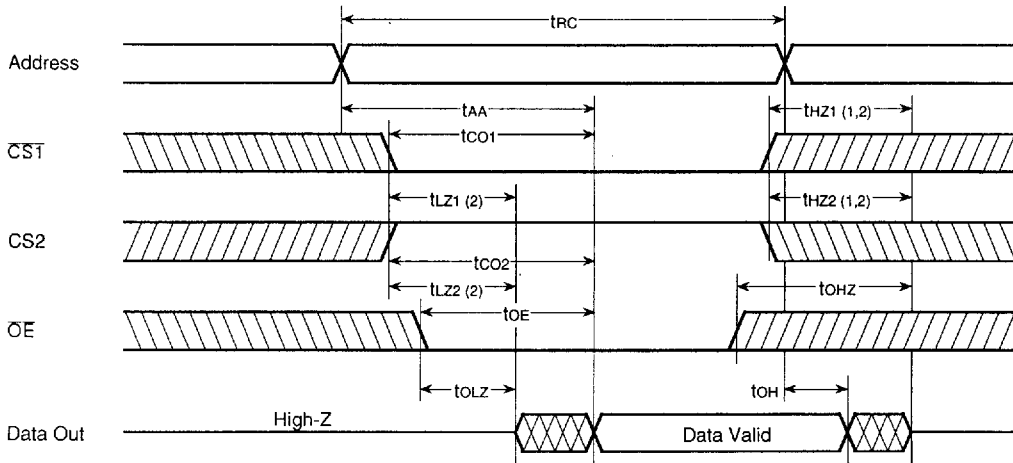
**TIMING DIAGRAMS**

**TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled)**

(CS1=OE=VIL, CS2=WE=VIH)



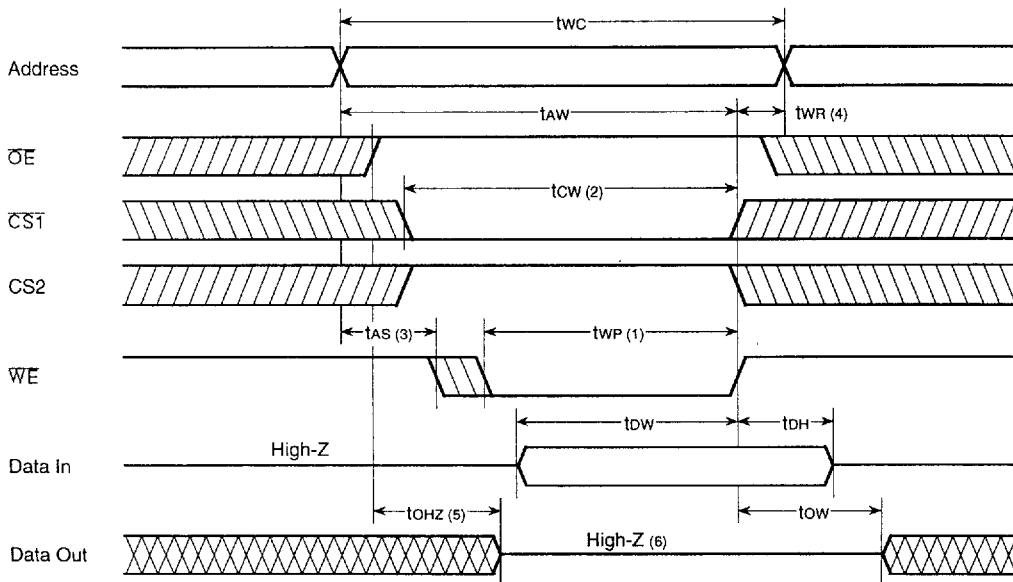
**TIMING WAVEFORM OF READ CYCLE(2) ( $WE=V_{IH}$ )**



**NOTES (READ CYCLE)**

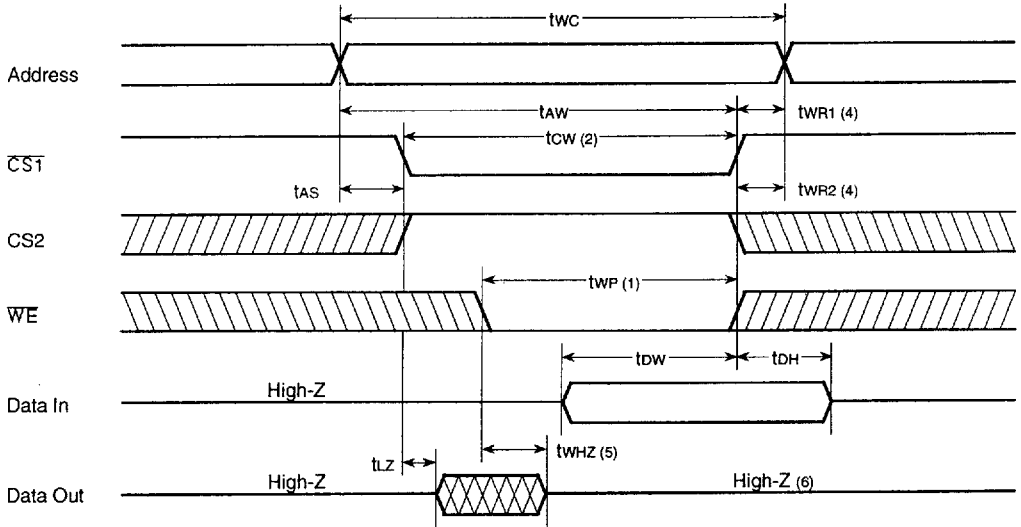
1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are referenced to the  $V_{OH}$  or  $V_{OL}$ .
2. At any given temperature and voltage condition  $t_{HZ}(\max)$  is less than  $t_{LZ}(\min)$  both for a given device and from device to device.
3.  $WE$  is high for read cycle.

**TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}$  Clock)**

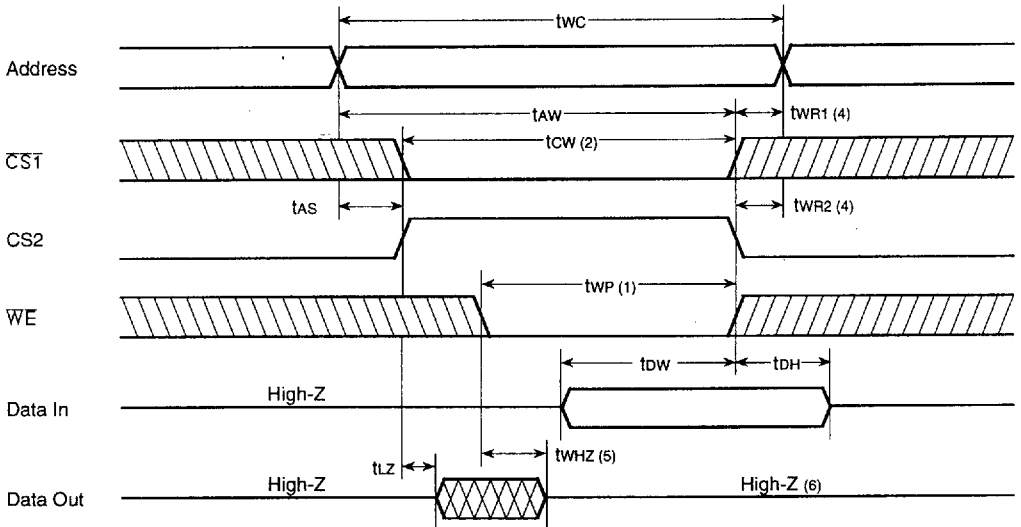


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**TIMING WAVEFORM OF WRITE CYCLE(2) (CS1 Controlled)**



**TIMING WAVEFORM OF WRITE CYCLE(3) (CS2 Controlled)**



**NOTES (WRITE CYCLE)**

1. A write occurs during the overlap of a low  $\overline{CS1}$ , a high CS2 and a low  $\overline{WE}$ . A write begins at the latest transition among  $\overline{CS1}$  going low, CS2 going high and  $\overline{WE}$  going low: A write ends at the earliest transition among  $\overline{CS1}$  going high, CS2 going low and  $\overline{WE}$  going high,  $t_{WR}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of  $\overline{CS1}$  going low or CS2 going high to the end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR1}$  applied in case a write ends at  $\overline{CS1}$ , or  $\overline{WE}$  going high,  $t_{WR2}$  applied in case a write ends at CS2 going to low.
5. If  $\overline{OE}$ , CS2 and  $\overline{WE}$  are in the read mode during in this period, the I/O pins are in the Low-Z state, inputs of opposite phase of the output must not be applied because bus contention can occur.
6. If  $\overline{CS1}$  goes low simultaneously with  $\overline{WE}$  going low or after  $\overline{WE}$  going low, the outputs remain in high impedance state.

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**FUNCTIONAL DESCRIPTION**

$\overline{CS}$	CS2	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Vcc Current
H	X	X	X	Power down	High-Z	$I_{SB}, I_{SB1}$
X	L	X	X	Power down	High-Z	$I_{SB}, I_{SB1}$
L	H	H	H	Output Disable	High-Z	$I_{CC}$
L	H	H	L	Read	DOUT	$I_{CC}$
L	H	L	X	Write	DIN	$I_{CC}$

Note : X means Don't Care.

**DATA RETENTION CHARACTERISTICS** (Ta= 0 to 70°C)

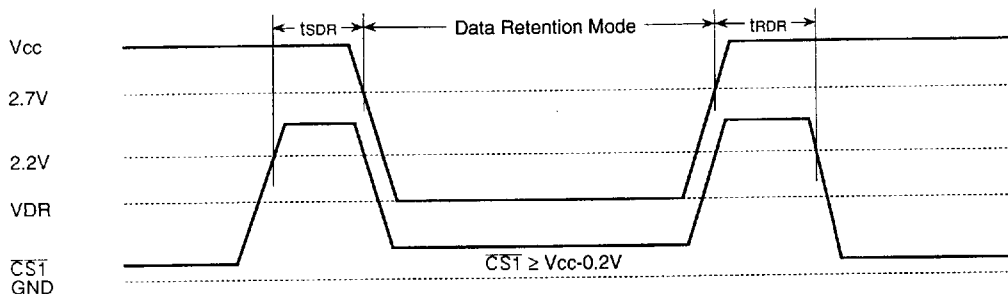
PARAMETER	SYMBOL	TEST CONDITION	MIN	Typ	MAX	UNIT
Vcc for Data Retention	Vdr	(1) $\overline{CS}1 \geq V_{cc} - 0.2V$	2.0		3.3	V
Data Retention Current	Idr	$V_{cc} = 3.0V$ $\overline{CS}1 \geq V_{cc} - 0.2V$	L	1.0	40(2)	$\mu A$
			LL	0.5	10(3)	$\mu A$
Data Retention Set-up Time	tSDR	See Data Retention Waveforms (below)	0			ns
Recovery Time	tRDR		5			ms

(1)  $\overline{CS}1 \geq V_{cc} - 0.2, CS2 \geq V_{cc} - 0.2$  ( $\overline{CS}1$  Controlled) or  $CS2 \leq 0.2$  ( $CS2$  Controlled)

(2) 20  $\mu A$  (max.) at 0 °C to 40 °C

(3) 3  $\mu A$  (max.) at 0 °C to 40 °C

**DATA RETENTION WAVEFORM 1** ( $\overline{CS}1$  Controlled)



**DATA RETENTION WAVEFORM 2** ( $CS2$  Controlled)

