# Am2946/Am2947

Octal Three-State Bidirectional Bus Transceivers

## DISTINCTIVE CHARACTERISTICS

- 8-bit bidirectional data flow reduces system package count
- 3-state inputs/outputs for interfacing with bus-oriented systems; PNP inputs reduce input loading
- $V_{CC}$ – 1.15$V_{OH}$ interfaces with TTL, MOS and CMOS
- 48mA, 300pF bus drive capability; Low power – 8mA per bidirectional bit
- Am2946 inverting transceivers; Am2947 noninverting transceivers; Transmit/$\overline{\text{Receive}}$ and Chip Disable simplify control logic
- Bus port stays in hi-impedance state during power up/down

## GENERAL DESCRIPTION

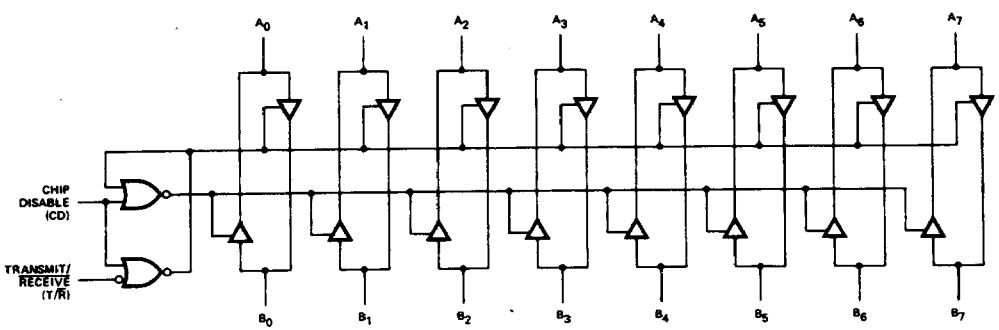
The Am2946 and Am2947 are 8-bit state Schottky transceivers. They provide bidirectional drive for bus-oriented microprocessor and digital communications systems. Straight through bidirectional transceivers are featured, with 24mA drive capability on the A ports and 48mA bus drive capability on the B ports. PNP inputs are incorporated to reduce input loading.

One input, Transmit/$\overline{\text{Receive}}$, determines the direction of logic signals through the bidirectional transceiver. The Chip Disable input disables both A and B ports by placing them in a 3-state condition. Chip Disable is functionally the same as an active LOW chip select.

The output high voltage ($V_{OH}$) is specified at $V_{CC}$ – 1.15V minimum to allow interfacing with MOS, CMOS, TTL, ROM, RAM, or microprocessors.

## BLOCK DIAGRAM

**Am2947**




BD002530

Am2946 has inverting transceivers.

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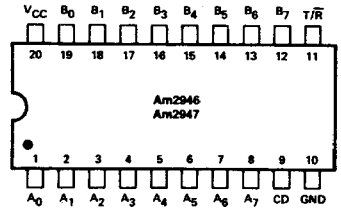
Refer to Page 13-1 for Essential Information on Military Devices

## CONNECTION DIAGRAM
### Top View

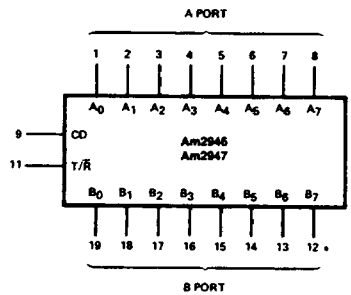
**D-20-1**




CD004760

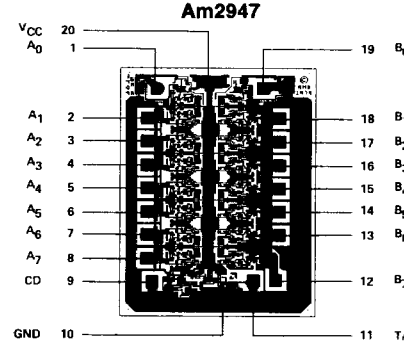
Note: Pin 1 is marked for orientation

## LOGIC SYMBOL




LS001060

## METALLIZATION AND PAD LAYOUT
### Am2947




**DIE SIZE .069" x .089"**
**Note: The Am2946 has inverting transceivers**

## ORDERING INFORMATION

AMD products are available in several packages and operating ranges. The order number is formed by a combination of the following: Device number, speed option (if applicable), package type, operating range and screening option (if desired).

**Am2946/2947** **D** **C** **B**

- **B** — Screening Option
  - Blank – Standard processing
  - B – Burn-in
- **C** — Temperature (See Operating Range)
  - C – Commercial (0°C to +70°C)
  - M – Military (–55°C to +125°C)
- **D** — Package
  - D– 20-pin CERDIP
  - X– Dice
- **Am2946/2947** — Device type
  - Bidirectional Bus Transceivers

| Valid Combinations | |
|---|---|
| Am2946<br>Am2947 | PC<br>DC, DCB, DM, DMB<br>XC |

**Valid Combinations**

Consult the AMD sales office in your area to determine if a device is currently available in the combination you wish.

## PIN DESCRIPTION

| Pin No. | Name | I/O | Description |
|---|---|---|---|
| | $A_0$-$A_7$ | I/O | A port inputs/outputs are receiver output drivers when T/$\overline{R}$ is LOW and are transmit inputs when T/$\overline{R}$ is HIGH. |
| | $B_0$-$B_7$ | I/O | B port inputs/outputs are transmit output drivers when T/$\overline{R}$ is HIGH and receiver inputs when T/$\overline{R}$ is LOW. |
| 9 | CD | I | Chip Disable forces all output drivers into 3-state when HIGH (same function as active LOW chip select, $\overline{CS}$). |
| 11 | T/$\overline{R}$ | I | Transmit/$\overline{Receive}$ direction control determines whether A port or B port drivers are in 3-state. With T/$\overline{R}$ HIGH A port is the input and B port is the output. With T/$\overline{R}$ LOW A port is the output and B port is the input. |

## FUNCTION TABLE

| Inputs | Conditions | | |
|---|---|---|---|
| Chip Disable | L | L | H |
| Transmit/$\overline{Receive}$ | L | H | X |
| A Port | Out | In | HI-Z |
| B Port | In | Out | HI-Z |



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Refer to Page 13-1 for Essential Information on Military Devices

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C
Supply Voltage ..... 7.0V
Input Voltage ..... 5.5V
Output Voltage ..... 5.5V
Lead Temperature (Solder, 10 seconds) ..... 300°C

*Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.*

## OPERATING RANGES

Commercial (C) Devices
Temperature ..... 0°C to +70°C
Supply Voltage ..... +4.75V to +5.25V

Military (M) Devices
Temperature ..... −55°C to +125°C
Supply Voltage ..... +4.5V to +5.5V

*Operating ranges define those limits over which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over operating range unless otherwise specified

| Parameters | Description | Test Conditions | | Min | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|---|---|
| **A PORT ($A_0$-$A_7$)** | | | | | | | |
| $V_{IH}$ | Logical "1" Input Voltage | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = 2.0V$ | | 2.0 | | | Volts |
| $V_{IL}$ | Logical "0" Input Voltage | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = 2.0V$ | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| $V_{OH}$ | Logical "1" Output Voltage | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = 0.8V$ | $I_{OH} = -0.4mA$ | $V_{CC} - 1.15$ | $V_{CC} - 0.7$ | | Volts |
| | | | $I_{OH} = -3.0mA$ | 2.7 | 3.95 | | |
| $V_{OL}$ | Logical "0" Output Voltage | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = 0.8V$ | $I_{OL} = 12mA$ | | 0.3 | 0.4 | Volts |
| | | | COM'L $I_{OL} = 24mA$ | | 0.35 | 0.50 | |
| $I_{OS}$ | Output Short Circuit Current | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = 0.8V$, $V_O = 0V$, $V_{CC}$ = MAX, Note 2 | | −10 | −38 | −75 | mA |
| $I_{IH}$ | Logical "1" Input Current | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = 2.0V$, $V_I = 2.7V$ | | | 0.1 | 80 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | $\overline{CD} = 2.0V$, $V_{CC}$ MAX, $V_I = V_{CC}$ MAX | | | | 1 | mA |
| $I_{IL}$ | Logical "0" Input Current | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = 2.0V$, $V_I = 0.4V$ | | | −70 | −200 | μA |
| $V_C$ | Input Clamp Voltage | $\overline{CD} = 2.0V$, $I_{IN} = -12mA$ | | | −0.7 | −1.5 | Volts |
| $I_{OD}$ | Output/Input 3-State Current | $\overline{CD} = 2.0V$ | $V_O = 0.4V$ | | | −200 | μA |
| | | | $V_O = 4.0V$ | | | 80 | |
| **B PORT ($B_0$-$B_7$)** | | | | | | | |
| $V_{IH}$ | Logical "1" Input Voltage | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = V_{IL}$ MAX | | 2.0 | | | Volts |
| $V_{IL}$ | Logical "0" Input Voltage | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = V_{IL}$ MAX | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| $V_{OH}$ | Logical "1" Output Voltage | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = 2.0V$ | $I_{OH} = -0.4mA$ | $V_{CC} - 1.15$ | $V_{CC} - 0.8$ | | Volts |
| | | | $I_{OH} = -5.0mA$ | 2.7 | 3.9 | | |
| | | | $I_{OH} = -10mA$ | 2.4 | 3.6 | | |
| $V_{OL}$ | Logical "0" Output Voltage | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = 2.0V$ | $I_{OL} = 20mA$ | | 0.3 | 0.4 | Volts |
| | | | $I_{OL} = 48mA$ | | 0.4 | 0.5 | |
| $I_{OS}$ | Output Short Circuit Current | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = 2.0V$, $V_O = 0V$ $V_{CC}$ = MAX, Note 2 | | −25 | −50 | −150 | mA |
| $I_{IH}$ | Logical "1" Input Current | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = V_{IL}$ MAX, $V_I = 2.7V$ | | | 0.1 | 80 | μA |
| $I_I$ | Input Current at Minimum Input Voltage | $\overline{CD} = 2.0V$, $V_{CC}$ = MAX, $V_I = V_{CC}$ MAX | | | | 1 | mA |
| $I_{IL}$ | Logical "0" Input Current | $\overline{CD} = V_{IL}$ MAX, $T/\overline{R} = V_{IL}$ MAX, $V_I = 0.4V$ | | | −70 | −200 | μA |
| $V_C$ | Input Clamp Voltage | $\overline{CD} = 2.0V$, $I_{IN} = -12mA$ | | | −0.7 | −1.5 | Volts |
| $I_{CO}$ | Output/Input 3-State Current | $\overline{CD} = 2.0V$ | $V_O = 0.4V$ | | | −200 | μA |
| | | | $V_O = 4.0V$ | | | 200 | |
| **CONTROL INPUTS CD, $T/\overline{R}$** | | | | | | | |
| $V_{IH}$ | Logical "1" Input Voltage | | | 2.0 | | | Volts |
| $V_{IL}$ | Logical "0" Input Voltage | | COM'L | | | 0.8 | Volts |
| | | | MIL | | | 0.7 | |
| $I_{IH}$ | Logical "1" Input Current | $V_I = 2.7V$ | | | 0.5 | 20 | μA |
| $I_I$ | Input Current at Maximum Input Voltage | $V_{CC}$ = MAX, $V_I = V_{CC}$ MAX | | | | 1.0 | mA |
| $I_{IL}$ | Logical "0" Input Current | $V_I = 0.4V$ | $T/\overline{R}$ | | −0.1 | −0.25 | mA |
| | | | CD | | −0.1 | −0.25 | |
| $V_C$ | Input Clamp Voltage | $I_{IN} = -12mA$ | | | −0.8 | −1.5 | Volts |
| **POWER SUPPLY CURRENT** | | | | | | | |
| $I_{CC}$ | Power Supply Current | Am2946 | $\overline{CD} = V_I = 2.0V$, $V_{CC}$ = MAX | | 70 | 100 | mA |
| | | | $\overline{CD} = 0.4V$, $V_{INA} = T/\overline{R} = 2.0V$, $V_{CC}$ = MAX | | 100 | 150 | |
| | | Am2947B | $\overline{CD} = 2.0V$, $V_I = 0.4V$, $V_{CC}$ = MAX | | 70 | 100 | |
| | | | $\overline{CD} = V_{INA} = 0.4V$, $T/\overline{R} = 2.0V$, $V_{CC}$ = MAX | | 90 | 140 | |

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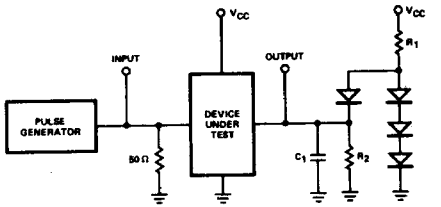
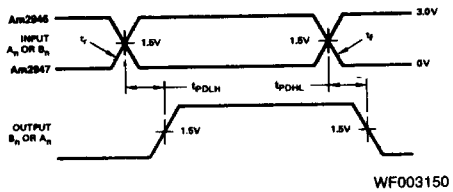
Refer to Page 13-1 for Essential Information on Military Devices

## SWITCHING TEST CIRCUIT



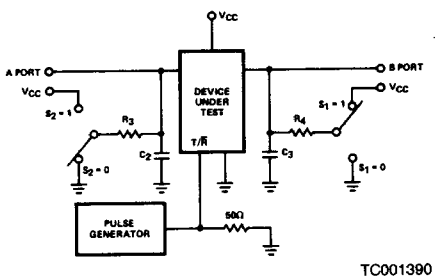

Note: $C_1$ includes test fixture capacitance.

## SWITCHING TIME WAVEFORM

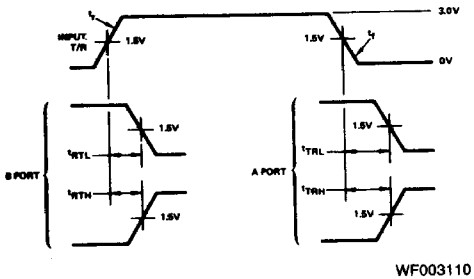



$t_r = t_f < 10ns$ 10% to 90%

**Figure 1. Propagation Delay from A Port to B Port or from B Port to A Port.**

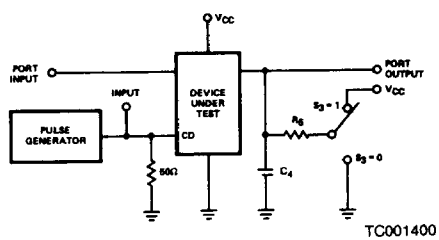



Note: $C_2$ and $C_3$ include test fixture capacitance.

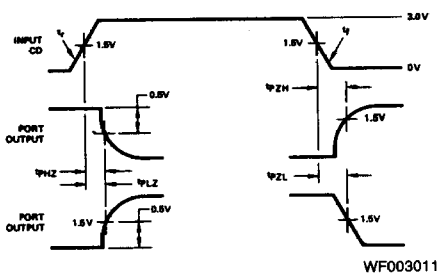



$t_r = t_f < 10ns$ 10% to 90%

**Figure 2. Propagation Delay from T/$\overline{R}$ to A Port or B Port.**




Note: $C_4$ includes test fixture capacitance. Port input is in a fixed logical condition.




$t_r = t_f < 10ns$ 10% to 90%

**Figure 3. Propagation Delay from CD to A Port or B Port.**

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## SWITCHING CHARACTERISTICS ($T_A$ = +25°C, $V_{CC}$ = 5.0V)
## Am2946

| Parameter | Description | Test Conditions | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|
| **A PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLA}$ | Propagation Delay to a Logical "0" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 8 | 12 | ns |
| $t_{PDLHA}$ | Propagation Delay to a Logical "1" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 11 | 16 | ns |
| $t_{PLZA}$ | Propagation Delay from a Logical "0" to 3-State from CD to A Port | $B_0$ to $B_7$ = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 10 | 15 | ns |
| $t_{PHZA}$ | Propagation Delay from a Logical "1" to 3-State from CD to A Port | $B_0$ to $B_7$ = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 8 | 15 | ns |
| $t_{PZLA}$ | Propagation Delay from 3-State to a Logical "0" from CD to A Port | $B_0$ to $B_7$ = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 30pF | 19 | 25 | ns |
| $t_{PZHA}$ | Propagation Delay from 3-State to a Logical "1" from CD to A Port | $B_0$ to $B_7$ = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 5k, $C_4$ = 30pF | 19 | 25 | ns |
| **B PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLB}$ | Propagation Delay to a Logical "0" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 12 | 18 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 7 | 12 | ns |
| $t_{PDLHB}$ | Propagation Delay to a Logical "1" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 15 | 20 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 9 | 14 | ns |
| $t_{PLZB}$ | Propagation Delay from a Logical "0" to 3-State from CD to B Port | $A_0$ to $A_7$ = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 13 | 18 | ns |
| $t_{PHZB}$ | Propagation Delay from a Logical "1" to 3-State from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 8 | 15 | ns |
| $t_{PZLB}$ | Propagation Delay from 3-State to a Logical "0" from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 100Ω, $C_4$ = 300pF | 25 | 35 | ns |
| | | $S_3$ = 1, $R_5$ = 667Ω, $C_1$ = 45pF | 16 | 22 | ns |
| $t_{PZHB}$ | Propagation Delay from 3-State to a Logical "1" from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 300pF | 22 | 35 | ns |
| | | $S_3$ = 0, $R_5$ = 5k, $C_1$ = 45pF | 14 | 22 | ns |
| **TRANSMIT RECEIVE MODE SPECIFICATIONS** | | | | | |
| $t_{TRL}$ | Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 100Ω, $C_3$ = 5pF<br>$S_2$ = 1, $R_3$ = 1k, $C_2$ = 30pF | 23 | 33 | ns |
| $t_{TRH}$ | Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>$S_1$ = 0, $R_4$ = 100Ω, $C_3$ = 5pF<br>$S_2$ = 0, $R_3$ = 5k, $C_2$ = 30pF | 22 | 33 | ns |
| $t_{RTL}$ | Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 100Ω, $C_3$ = 300pF<br>$S_2$ = 1, $R_3$ = 300Ω, $C_2$ = 5pF | 26 | 35 | ns |
| $t_{RTH}$ | Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>$S_1$ = 0, $R_4$ = 1k, $C_3$ = 300pF<br>$S_2$ = 0, $R_3$ = 300Ω, $C_2$ = 5pF | 27 | 35 | ns |

Note: 1. All typical values given are for $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Only one output at a time should be shorted.

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified
**Am2946**

| Parameter | Description | Test Conditions | COMMERCIAL Am2946 Max | MILITARY Am2946 Max | Units |
|---|---|---|---|---|---|
| **A PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLA}$ | Propagation Delay to a Logical "0" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 16 | 19 | ns |
| $t_{PDLHA}$ | Propagation Delay to a Logical "1" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 20 | 23 | ns |
| $t_{PLZA}$ | Propagation Delay from a Logical "0" to 3-State from CD to A Port | $B_0$ to $B_7$ = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 18 | 21 | ns |
| $t_{PHZA}$ | Propagation Delay from a Logical "1" to 3-State from CD to A Port | $B_0$ to $B_7$ = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 18 | 21 | ns |
| $t_{PZLA}$ | Propagation Delay from 3-State to a Logical "0" from CD to A Port | $B_0$ to $B_7$ = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 30pF | 28 | 33 | ns |
| $t_{PZHA}$ | Propagation Delay from 3-State to a Logical "1" from CD to A Port | $B_0$ to $B_7$ = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 5k, $C_4$ = 30pF | 28 | 33 | ns |
| **B PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLB}$ | Propagation Delay to a Logical "0" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 24 | 29 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 16 | 19 | ns |
| $t_{PDLHB}$ | Propagation Delay to a Logical "1" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 25 | 30 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 19 | 22 | ns |
| $t_{PLZB}$ | Propagation Delay from a Logical "0" to 3-State from CD to B Port | $A_0$ to $A_7$ = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 23 | 26 | ns |
| $t_{PHZB}$ | Propagation Delay from a Logical "1" to 3-State from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 18 | 21 | ns |
| $t_{PZLB}$ | Propagation Delay from 3-State to a Logical "0" from CD to B Port | $A_0$ to $A_7$ = 2.4V, T/$\overline{R}$ = 2.4V(Figure 3)<br>$S_3$ = 1, $R_5$ = 100Ω, $C_4$ = 300pF | 38 | 43 | ns |
| | | $S_3$ = 1, $R_5$ = 667Ω, $C_4$ = 45pF | 26 | 30 | ns |
| $t_{PZHB}$ | Propagation Delay from 3-State to a Logical "1" from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V(Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 300pF | 38 | 43 | ns |
| | | $S_3$ = 0, $R_5$ = 5k, $C_4$ = 45pF | 26 | 30 | ns |
| **TRANSMIT RECEIVE MODE SPECIFICATIONS** | | | | | |
| $t_{TRL}$ | Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 100Ω, $C_3$ = 5pF<br>$S_2$ = 1, $R_3$ = 1k, $C_2$ = 30pF | 38 | 43 | ns |
| $t_{TRH}$ | Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>$S_1$ = 0, $R_4$ = 100Ω, $C_3$ = 5pF<br>$S_2$ = 0, $R_3$ = 5k, $C_2$ = 30pF | 38 | 43 | ns |
| $t_{RTL}$ | Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 100Ω, $C_3$ = 300pF<br>$S_2$ = 1, $R_3$ = 300Ω, $C_2$ = 5pF | 41 | 47 | ns |
| $t_{RTH}$ | Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>$S_1$ = 0, $R_4$ = 1k, $C_3$ = 300pF<br>$S_2$ = 0, $R_3$ = 300Ω, $C_2$ = 5pF | 41 | 47 | ns |

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Refer to Page 13-1 for Essential Information on Military Devices

## SWITCHING CHARACTERISTICS ($T_A$ = +25°C, $V_{CC}$ = 5.0V)
## Am2947

| Parameter | Description | Test Conditions | Typ (Note 1) | Max | Units |
|---|---|---|---|---|---|
| **A PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLA}$ | Propagation Delay to a Logical "0" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 14 | 18 | ns |
| $t_{PDLHA}$ | Propagation Delay to a Logical "1" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 13 | 18 | ns |
| $t_{PLZA}$ | Propagation Delay from a Logical "0" to 3-State from CD to A Port | $B_0$ to $B_7$ = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 11 | 15 | ns |
| $t_{PHZA}$ | Propagation Delay from a Logical "1" to 3-State from CD to A Port | $B_0$ to $B_7$ = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 8 | 15 | ns |
| $t_{PZLA}$ | Propagation Delay from 3-State to a Logical "0" from CD to A Port | $B_0$ to $B_7$ = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 30pF | 19 | 25 | ns |
| $t_{PZHA}$ | Propagation Delay from 3-State to a Logical "1" from CD to A Port | $B_0$ to $B_7$ = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 5k, $C_4$ = 30pF | 19 | 25 | ns |
| **B PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLB}$ | Propagation Delay to a Logical "0" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) | | | |
| | | $R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 18 | 23 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 11 | 18 | ns |
| $t_{PDLHB}$ | Propagation Delay to a Logical "1" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1) | | | |
| | | $R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 16 | 23 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 11 | 18 | ns |
| $t_{PLZB}$ | Propagation Delay from a Logical "0" to 3-State from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 13 | 18 | ns |
| $t_{PHZB}$ | Propagation Delay from a Logical "1" to 3-State from CD to B Port | $A_0$ to $A_7$ = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 8 | 15 | ns |
| $t_{PZLB}$ | Propagation Delay from 3-State to a Logical "0" from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3) | | | |
| | | $S_3$ = 1, $R_5$ = 100Ω, $C_4$ = 300pF | 25 | 35 | ns |
| | | $R_3$ = 1, $R_5$ = 667Ω, $C_1$ = 45pF | 16 | 22 | ns |
| $t_{PZHB}$ | Propagation Delay from 3-State to a Logical "1" from CD to B Port | $A_0$ to $A_7$ = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3) | | | |
| | | $S_3$ = 0, $R_5$ = 1k, $C_4$ = 300pF | 26 | 35 | ns |
| | | $S_3$ = 0, $R_5$ = 5k, $C_1$ = 45pF | 14 | 22 | ns |
| **TRANSMIT RECEIVE MODE SPECIFICATIONS** | | | | | |
| $t_{TRL}$ | Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 100Ω, $C_3$ = 5pF<br>$S_2$ = 1, $R_3$ = 1k, $C_2$ = 30pF | 28 | 38 | ns |
| $t_{TRH}$ | Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 100Ω, $C_3$ = 5pF<br>$S_2$ = 0, $R_3$ = 5k, $C_2$ = 30pF | 28 | 38 | ns |
| $t_{RTL}$ | Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 100Ω, $C_3$ = 300pF<br>$S_2$ = 0, $R_3$ = 300Ω, $C_2$ = 5pF | 31 | 40 | ns |
| $t_{RTH}$ | Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>$S_1$ = 0, $R_4$ = 1k, $C_3$ = 300pF<br>$S_2$ = 1, $R_3$ = 300Ω, $C_2$ = 5pF | 31 | 40 | ns |

Note: 1. All typical values given are for $V_{CC}$ = 5.0V and $T_A$ = 25°C.
2. Only one output at a time should be shorted.

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Refer to Page 13-1 for Essential Information on Military Devices

## SWITCHING CHARACTERISTICS over operating range unless otherwise specified
**Am2947**

| Parameter | Description | Test Conditions | COMMERCIAL Am2947 Max | MILITARY Am2947 Max | Units |
|---|---|---|---|---|---|
| **A PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLA}$ | Propagation Delay to a Logical "0" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 21 | 24 | ns |
| $t_{PDLHA}$ | Propagation Delay to a Logical "1" from B Port to A Port | CD = 0.4V, T/$\overline{R}$ = 0.4V (Figure 1)<br>$R_1$ = 1k, $R_2$ = 5k, $C_1$ = 30pF | 21 | 24 | ns |
| $t_{PLZA}$ | Propagation Delay from a Logical "0" to 3-State from CD to A Port | $B_0$ to $B_7$ = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 18 | 21 | ns |
| $t_{PHZA}$ | Propagation Delay from a Logical "1" to 3-State from CD to A Port | $B_0$ to $B_7$ = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 18 | 21 | ns |
| $t_{PZLA}$ | Propagation Delay from 3-State to a Logical "0" from CD to A Port | $B_0$ to $B_7$ = 0.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 30pF | 28 | 33 | ns |
| $t_{PZHA}$ | Propagation Delay from 3-State to a Logical "1" from CD to A Port | $B_0$ to $B_7$ = 2.4V, T/$\overline{R}$ = 0.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 5k, $C_4$ = 30pF | 28 | 33 | ns |
| **B PORT DATA/MODE SPECIFICATIONS** | | | | | |
| $t_{PDHLB}$ | Propagation Delay to a Logical "0" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 28 | 34 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 22 | 25 | ns |
| $t_{PDLHB}$ | Propagation Delay to a Logical "1" from A Port to B Port | CD = 0.4V, T/$\overline{R}$ = 2.4V (Figure 1)<br>$R_1$ = 100Ω, $R_2$ = 1k, $C_1$ = 300pF | 28 | 34 | ns |
| | | $R_1$ = 667Ω, $R_2$ = 5k, $C_1$ = 45pF | 22 | 25 | ns |
| $t_{PLZB}$ | Propagation Delay from a Logical "0" to 3-State from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 1k, $C_4$ = 15pF | 23 | 26 | ns |
| $t_{PHZB}$ | Propagation Delay from a Logical "1" to 3-State from CD to B Port | $A_0$ to $A_7$ = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 15pF | 18 | 21 | ns |
| $t_{PZLB}$ | Propagation Delay from 3-State to a Logical "0" from CD to B Port | $A_0$ to $A_7$ = 0.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 1, $R_5$ = 100Ω, $C_4$ = 300pF | 38 | 43 | ns |
| | | $S_3$ = 1, $R_5$ = 667Ω, $C_4$ = 45pF | 26 | 30 | ns |
| $t_{PZHB}$ | Propagation Delay from 3-State to a Logical "1" from CD to B Port | $A_0$ to $A_7$ = 2.4V, T/$\overline{R}$ = 2.4V (Figure 3)<br>$S_3$ = 0, $R_5$ = 1k, $C_4$ = 300pF | 38 | 43 | ns |
| | | $S_3$ = 0, $R_5$ = 5k, $C_4$ = 45pF | 26 | 30 | ns |
| **TRANSMIT RECEIVE MODE SPECIFICATIONS** | | | | | |
| $t_{TRL}$ | Propagation Delay from Transmit Mode to Receive a Logical "0", T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>$S_1$ = 0, $R_4$ = 100Ω, $C_3$ = 5pF<br>$S_2$ = 1, $R_3$ = 1k, $C_2$ = 30pF | 42 | 48 | ns |
| $t_{TRH}$ | Propagation Delay from Transmit Mode to Receive a Logical "1", T/$\overline{R}$ to A Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 100Ω, $C_3$ = 5pF<br>$S_2$ = 0, $R_3$ = 5k, $C_2$ = 30pF | 42 | 48 | ns |
| $t_{RTL}$ | Propagation Delay from Receive Mode to Transmit a Logical "0", T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>$S_1$ = 1, $R_4$ = 100Ω, $C_3$ = 300pF<br>$S_2$ = 1, $R_3$ = 300Ω, $C_2$ = 5pF | 45 | 51 | ns |
| $t_{RTH}$ | Propagation Delay from Receive Mode to Transmit a Logical "1", T/$\overline{R}$ to B Port | CD = 0.4V (Figure 2)<br>$S_1$ = 0, $R_4$ = 1k, $C_3$ = 300pF<br>$S_2$ = 1, $R_3$ = 300Ω, $C_2$ = 5pF | 45 | 51 | ns |

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Refer to Page 13-1 for Essential Information on Military Devices