mosaic

Mosaic Semiconductor Inc.

512Kx 8 CMOS SRAM

MSM8512-70/85/10

Issue 1.1 : November 1992

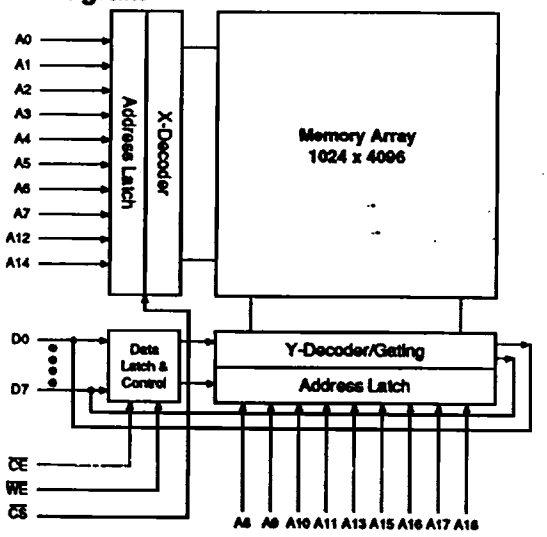
ADVANCE PRODUCT INFORMATION

524,288 x 8 CMOS High Speed Static RAM

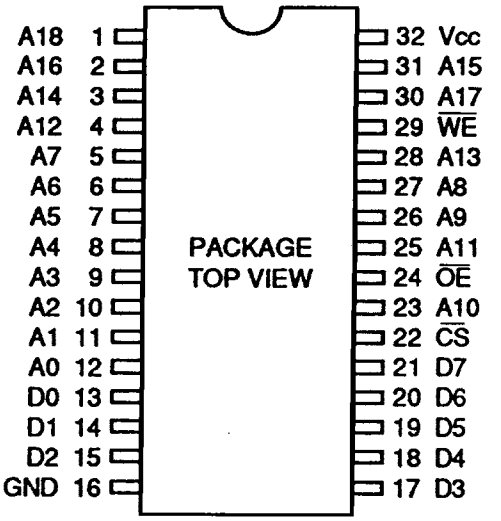
Features

Very Fast Access Times of 70/85/100 ns.
JEDEC Standard 32 pin Footprint.
VIL™ High Density Package.
Operating Power 275 mW(typ.)
Low Power Standby 10 µW (typ.)-L Version.
2.0V Data Retention Mode.
Completely Static Operation.
Equal Access and Cycle Times.
Battery Back-up Capability.
Directly TTL Compatible.
May be Processed to MIL-STD 883, non-compliant.

Block Diagram



Pin Definition



Pin Functions

A0-A18	Address Inputs
D0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (+5V)
GND	Ground

Package Details

Pin Count	Description	Package Type	Material	Pin Out
32	0.6" Dual-in-Line (DIL)	S	Ceramic	JEDEC
32	0.4" Dual-in-Line (DIL)	K	Ceramic	JEDEC
32	0.1" Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
32	Bottom Brazed Flatpack	G	Ceramic	JEDEC
32	Extended Leadless Chip Carrier (LCC)	TBD	Ceramic	TBD
32	J-Leaded Chip Carrier (JLCC)	TBD	Ceramic	TBD

See pages 6,7 for Package dimensions and outlines.

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-0.5 to +7	V
Power Dissipation	P_T	1.0	W
Storage Temperature	T_{STG}	-55 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) Pulse width:- 3.0V for less than 30ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.5	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AI}	-40	-	85	°C (suffix I)
	T_{AM}	-55	-	125	°C (suffix M, MB)

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=0°C to +70°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-	-	2	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	-	-	2	µA
Operating Supply Current	I_{CC}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA	-	15	35	mA
	I_{CC1}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, Min. Cycle, Duty=100%	-	55	90	mA
Standby Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, I/P's static	-	1	3	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V	-	0.02	2	mA
-L Version	I_{SB2}	As above	-	2	100	µA
Output Voltage	V_{OL}	I_{OL}=2.1mA	-	-	0.4	V
	V_{OH}	I_{OH}=-1.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

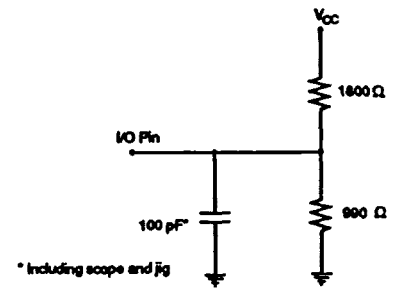
Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN}=0V	-	8	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$=0V	-	10	pF

Note: This parameter is sampled and not 100% tested

AC Test Conditions

* Input pulse levels: GND to 3.0V
* Input rise and fall times: 5ns
* Input and Output timing reference levels: 1.5V
* Output load: See Diagram
* V_{CC}=5V±10%

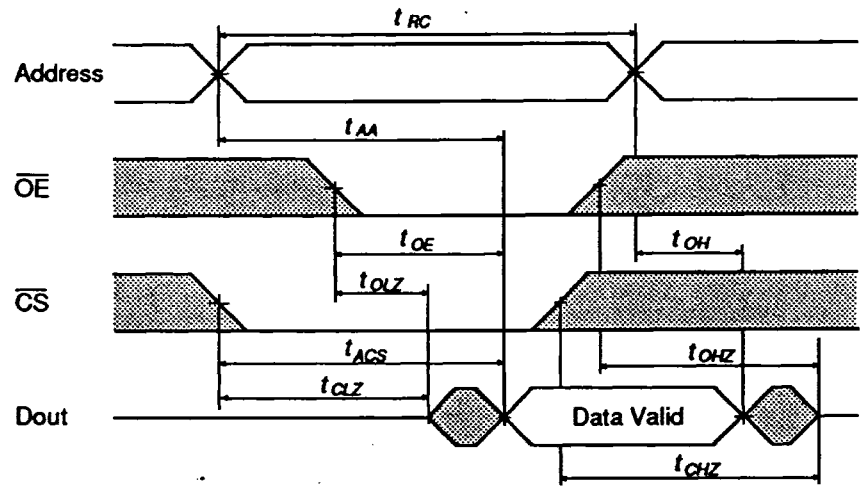
Output Load Circuit



Read Cycle Timing

Parameter	Symbol	-70 min	-70 max	-85 min	-85 max	-10 min	-10 max	Unit	Note
Read Cycle Time	t_{RC}	70	-	85	-	100	-	ns	
Address Access Time	t_{AA}	-	70	-	85	-	100	ns	
Chip Select Access Time	t_{ACS}	-	70	-	85	-	100	ns	
Output Enable to Output Valid	t_{OE}	-	35	-	45	-	50	ns	
Output Hold from Address Change	t_{OH}	10	-	10	-	10	-	ns	
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	ns	1
Output Enable to Output in Low Z	t_{OLZ}	5	-	5	-	5	-	ns	1
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	30	0	35	ns	1

Read Cycle Timing Waveform(1) (1,2)



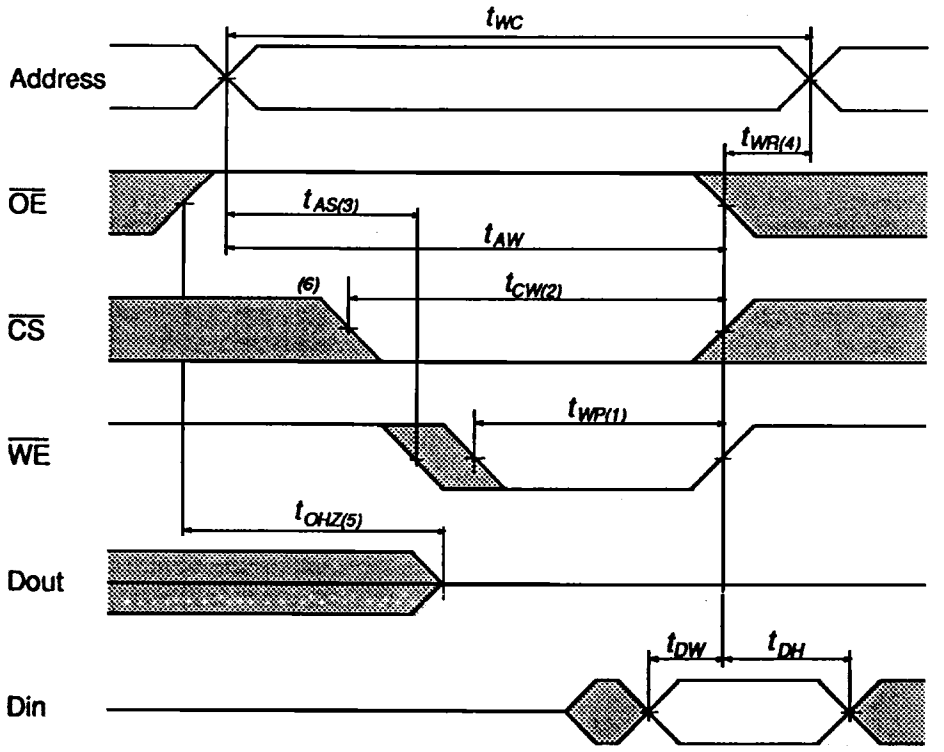
Notes: 1. This parameter is sampled and not 100% tested.
2. $\overline{WE}$ is High for Read Cycle.

Write Cycle Timing

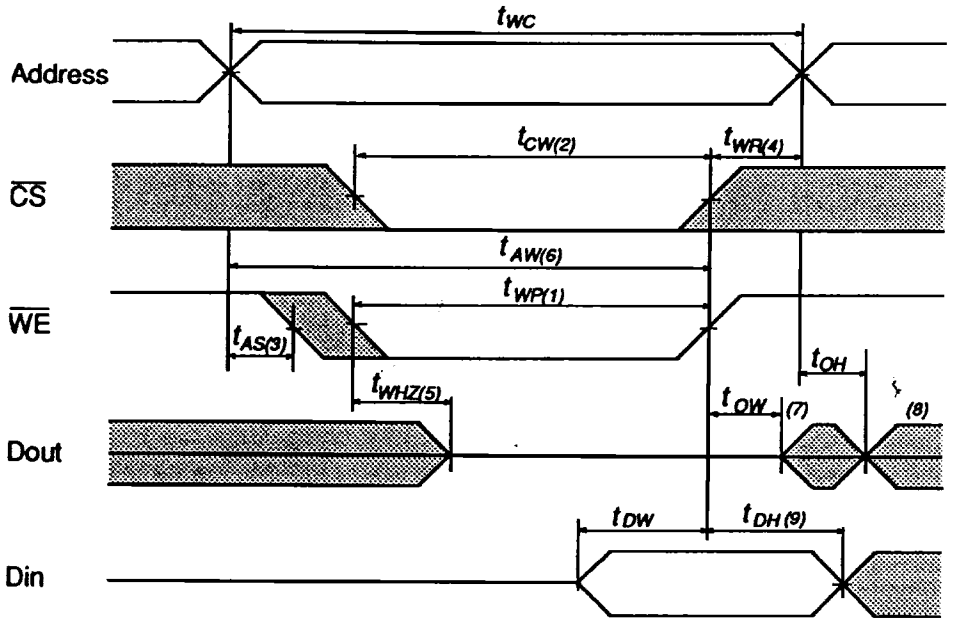
Parameter	Symbol	-70 min	-70 max	85 min	85 max	-100 min	-100 max	Unit	Note
Write Cycle Time	t_{RC}	70	-	85	-	100	-	ns	
Chip Selection to End of Write	t_{CW}	60	-	75	-	80	-	ns	
Address Valid to End of Write	t_{AW}	60	-	75	-	80	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	55	-	65	-	70	-	ns	
Write Recovery Time	t_{WR}	5	-	5	-	5	-	ns	
Write to Output in High Z	t_{WHZ}	0	30	0	30	0	35	ns	1
Data to Write Time Overlap	t_{DW}	35		55	-	55	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
Output Active from End of Write	t_{OW}	5	-	5	-	5	-	ns	1

Notes: 1. This parameter is sampled and not 100% tested.

Write Cycle No.1 Timing Waveform



Write Cycle No.2 Timing Waveform $\overline{OE}$ Low



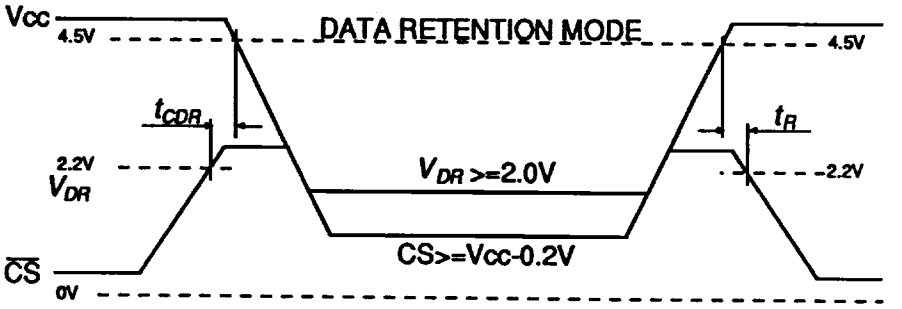
Notes:

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
2. t_{CW} is measured from $\overline{CS}$ going low to the end of write.
3. t_{AS} is measured from $\overline{CS}$ going low to the end of write.
4. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
5. During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
6. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, O/P's remain in a high impedance state.
7. Dout is in the same phase as written data of this write cycle.
8. Dout is the read data of next address.
9. If $\overline{CS}$ is low during this period, I/O pins are in the output state. I/P signals out of phase must not be applied to I/O pins.
10. This parameter is sampled not 100% tested

Low V_{cc} Data Retention Characteristics - L Version Only (T_A= 0°C to +70°C)

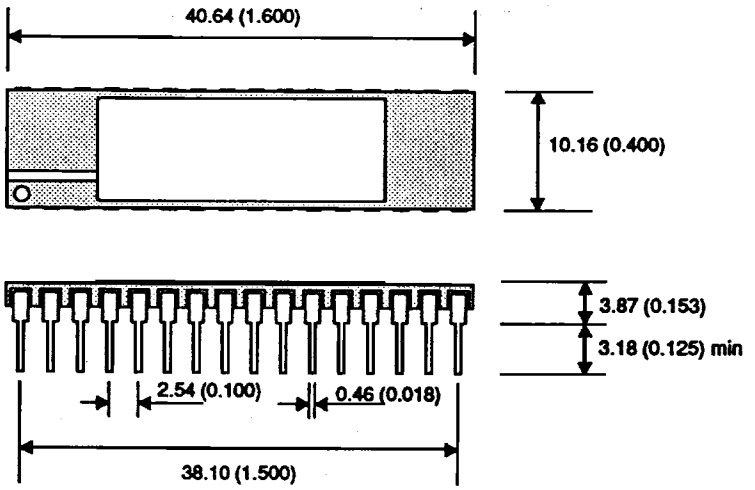
Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS}$>=V_{CC}-0.2V	2.0	-	-	V
Data Retention Current	I_{CCDR}	V_{CC}=3.0V, $\overline{CS}$≥V_{CC}-0.2	-	1	50	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	5	-	-	ms

Low V_{CC} Data Retention Timing Waveform

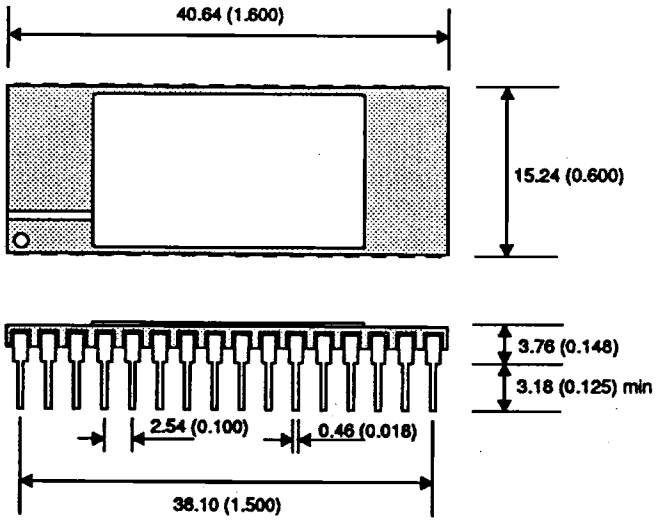


Package Details Dimensions in mm (inches). Tolerance on all dimensions ± 0.254 (0.010)

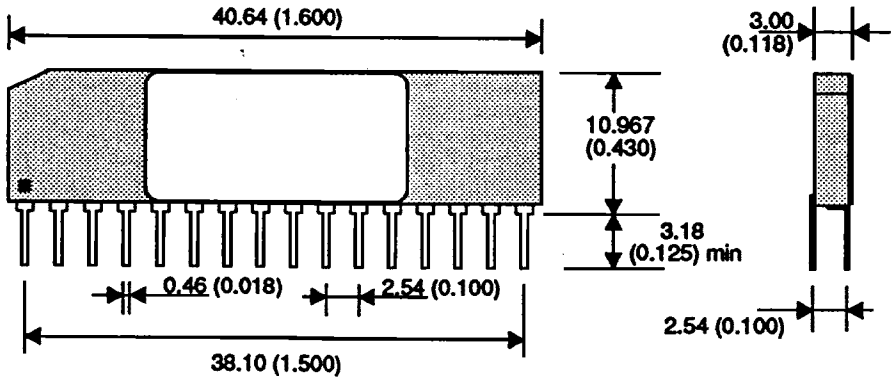
32 pin 0.4" Dual-In-Line (DIL) - 'K' Package Details



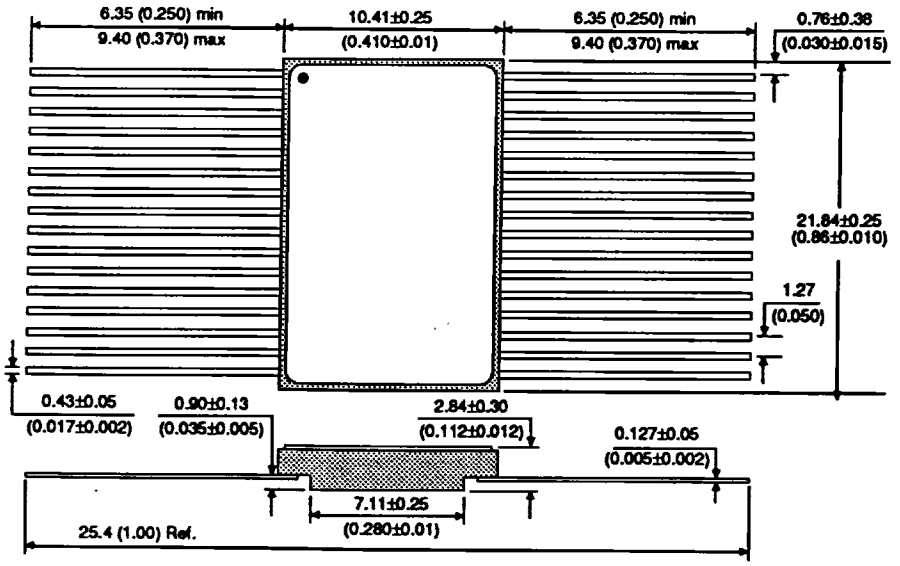
32 pin 0.6" Dual-In-Line (DIL) - 'S' Package



32 pin 0.1" Vertical-In-Line (VIL™) - 'V' Package



32 pin Bottom Brazed Ceramic Flatpack 'G' Package



Ordering Information

MSM8512KLMB-70

Speed	70	= 70 ns
	85	= 85 ns
	10	= 100 ns
Temp. range/screening	Blank	= Commercial Temp.
	I	= Industrial Temp.
	M	= Military Temp.
	MB	= Processed to MIL-STD 883 Method 5004, non-compliant.
	MC	= MIL-STD 883 Compliant, (Pending)
Power Consumption	Blank	= Standard Part
	L	= Low Power Part
Package	S	= 32 Pin 0.6" DIP
	K	= 32 Pin 0.4" DIP
	V	= 32 Pin 0.1" VIL
	W	= 32 Pad LCC
	J	= 32 Pad JLCC

Notes: For more information regarding screening flows contact Mosaic Semiconductor Inc. for a 'Volatile Monolithic Screening Level Applications Note.'

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