Preliminary Information

CAT24C21

1K (128 x 8) -Bit Dual Mode Serial EEPROM for VESA™ "Plug-and-Play"

FEATURES

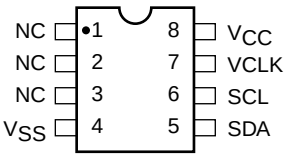
- 400 kHz I²C bus compatible*
- DDC1™/DDC2™ interface compliant for monitor identification
- 2.5 to 5.5 volt operation
- Low power CMOS technology
- Write protect feature
  — Entire array protected when VCLK at V_{IL}
- 16-byte page write buffer
- Self-timed write cycle with auto-clear
- 1,000,000 program/erase cycles
- 100 year data retention
- 8-pin DIP, SOIC, TSSOP or MSOP packages
- Industrial and extended temperature ranges

DESCRIPTION

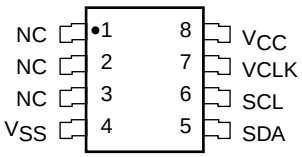
The CAT24C21 is a 1k-bit Serial CMOS EEPROM internally organized as 128 words of 8 bits each. The CAT24C21 can operate in two modes compliant to the VESA™, DDC1™ and DDC2™ standards for "Plug-and- Play" monitors. The Transmit-only Mode controlled by the VCLK input and the bi-directional Mode where the memories content is controlled by the I²C bus, SCL input. Catalyst's advanced CMOS technology substantially reduces device power requirements. The CAT24C21 features a 16-byte page write buffer. The device operates via the I²C bus serial interface, has a special write protection feature, and is available in 8-pin DIP, SOIC, TSSOP and MSOP packages.

PIN CONFIGURATION

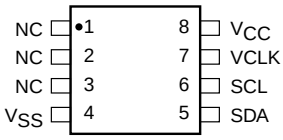
DIP Package (P, L)



SOIC Package (J, W)

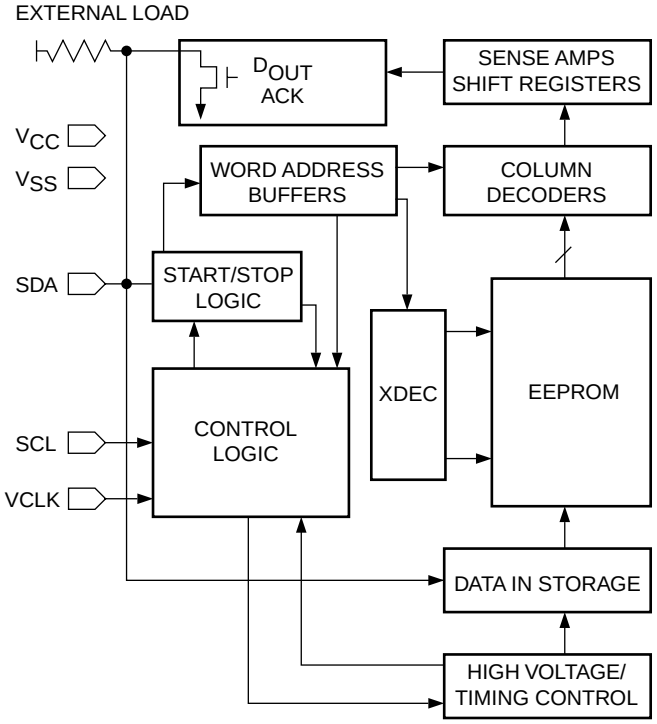


MSOP Package (R, Z)



TSSOP Package (U, Y)

BLOCK DIAGRAM



PIN FUNCTIONS

Pin Name	Function
NC	No Connect
SDA	Serial Data/Address
SCL	Serial Clock (Bidirectional Mode)
VCLK	Serial Clock (Transmit only Mode)
V_{CC}	+2.5V to +5.5V Power Supply
V_{SS}	Ground

* Catalyst Semiconductor is licensed by Philips Corporation to carry the I²C Bus Protocol.

© 2003 by Catalyst Semiconductor, Inc.
Characteristics subject to change without notice

Doc. No. 1032, Rev. G

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

Voltage on Any Pin with Respect to Ground(1) ..... -2.0V to +V_{CC} + 2.0V

V_{CC} with Respect to Ground ..... -2.0V to +7.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Lead Soldering Temperature (10 secs) ..... 300°C

Output Short Circuit Current(2) 100mA

*COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Reference Test Method	Min	Max	Units
N_{END}(3)	Endurance	MIL-STD-883, Test Method 1033	1,000,000		Cycles/Byte
T_{DR}(3)	Data Retention	MIL-STD-883, Test Method 1008	100		Years
V_{ZAP}(3)	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000		Volts
I_{LTH}(3)(4)	Latch-up	JEDEC Standard 17	100		mA

D.C. OPERATING CHARACTERISTICS

V_{CC} = +2.5V to +5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
I_{CC}	Power Supply Current	f_{SCL} = 100 KHz			3	mA
I_{SB}(5)	Standby Current (V_{CC} = 5.0V)	V_{IN} = GND or V_{CC}			0	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}			10	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}			10	µA
V_{IL}	Input Low Voltage (SCL & SDA)		–1		V_{CC} x 0.3	V
V_{IH}	Input High Voltage (SCL & SDA)		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage (V_{CC} = 3.0V)	I_{OL} = 3 mA			0.4	V
V_{OL2}	Output Low Voltage (V_{CC} = 1.8V)	I_{OL} = 1.5 mA			0.5	V
V_{IL}	Input Low Voltage (VCLK)				V_{CC} x 0.2	V
V_{IH}	Input High Voltage (VCLK)		2.0		0.8	V

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$C_{I/O}$(3)	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V			8	pF
C_{IN}(3)	Input Capacitance (VCLK, SCL)	V_{IN} = 0V			6	pF

Note:

(1) The minimum DC input voltage is –0.5V. During transitions, inputs may undershoot to –2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5V, which may overshoot to V_{CC} + 2.0V for periods of less than 20ns.

(2) Output shorted for no more than one second. No more than one output shorted at a time.

(3) This parameter is tested initially and after a design or process change that affects the parameter.

(4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from –1V to V_{CC} +1V.

(5) Standby Current (I_{SB}) = 0µA (<900nA).

A.C. CHARACTERISTICS

V_{CC} = +2.5V to +5.5V, unless otherwise specified.

Transmit-only Mode

Symbol	Parameter	2.5V to 5.5V			Units
		Min	Typ	Max	
TVAA	Output valid from VCLK			0.5	µs
TVHIGH	VCLK high	0.6			µs
TVLOW	VCLK low	1.3			µs
TVHZ	Mode transition			0.5	µs
TUPV	Transmit-only power-up	0			ns

Read & Write Cycle Limits

Symbol	Parameter	2.5V to 5.5V			Units
		Min	Typ	Max	
F_{SCL}	Clock Frequency			400	kHz
T_I (1)	Noise Suppression Time Constant at SCL, SDA Inputs			200	ns
t_{AA}	SCL Low to SDA Data Out and ACK Out			1	µs
t_{BUF} (1)	Time the Bus Must be Free Before a New Transmission Can Start	1.2			µs
$t_{HD:STA}$	Start Condition Hold Time	0.6			µs
t_{LOW}	Clock Low Period	1.2			µs
t_{HIGH}	Clock High Period	0.6			µs
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	0.6			µs
$t_{HD:DAT}$	Data In Hold Time	0			ns
$t_{SU:DAT}$	Data In Setup Time	50			ns
t_R (1)	SDA and SCL Rise Time			0.3	µs
t_F (1)	SDA and SCL Fall Time			300	ns
$t_{SU:STO}$	Stop Condition Setup Time	0.6			µs
t_{DH}	Data Out Hold Time	100			ns

Note:
(1) This parameter is tested initially and after a design or process change that affects the parameter.
(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Power-Up Timing[1][2]

Symbol	Parameter	Min	Typ	Max	Units
t_{PUR}	Power-up to Read Operation			1	ms
t_{PUW}	Power-up to Write Operation			1	ms

Write Cycle Limits

Symbol	Parameter	Min	Typ	Max	Units
t_{WR}	Write Cycle Time			10	ms

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal program/ erase cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high, and the device does not respond to its slave address.

FUNCTIONAL DESCRIPTION

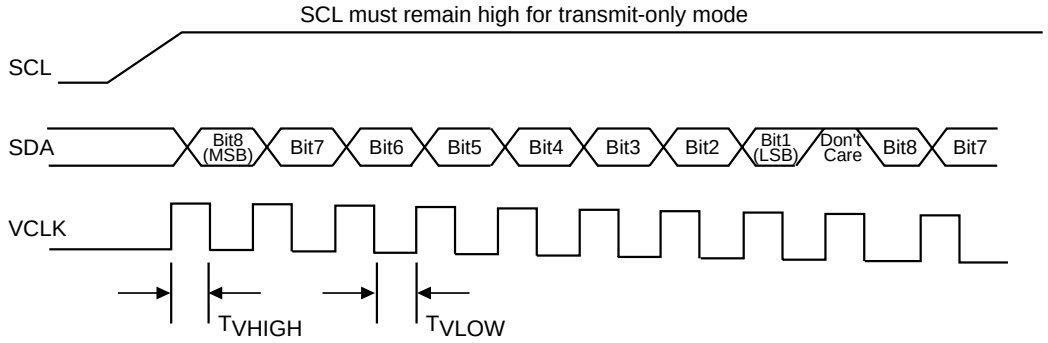
The CAT24C21 has two modes of operation: the Transmit-only Mode and the Bi-directional Mode. There is a separate 2-wire protocol to support each mode; each having a separate clock input (SCL and VCLK) and both modes sharing a common Bi-directional data line (SDA). The CAT24C21 enters the transmit-only mode upon power up and begins outputting data on the SDA pin with each clock signal on the VCLK pin. The device will remain in the transmit-only mode until there is a valid high to low transition on the SCL pin. The device will switch into the bi-directional mode when there is a valid transition on the SCL pin. Once in the bi-directinal mode, the only way to return to the transmit-only mode is by powering down the device.

Transmit-only Mode: (DDC1)

The CAT24C21 will power up in the Transmit-only mode and output one bit of data on the SDA pin for each rising edge of the VCLK pin. Data is transmitted in 8 bit words with the most significant bit first followed by a 9th "don't care" bit which will be in the high impedance state. The CAT24C21 will continuously sequence through the entire memory array as long as VCLK is present and no falling edges on SCL are received. When the maximum address (7FH) is reached, the output will wrap around to the zero location (00H) and continue. The bi-directional mode clock (SCL) pin must be held high for the device to remain in the transmit-only mode.

Upon power-up, the CAT24C21 will output valid data only after it has been initialized. During initialization, data will not be available until after the first nine clocks are sent to the device. The starting address for the transmit-only mode can be determined during initialization. If the SDA pin is high during the first eight clocks, the starting address will be 7FH. If the SDA pin

Figure 1. Transmit-only Mode



is low during the first eight clocks, the starting address will be 00H. During the ninth clock, SDA will be in the high impedance state.

PIN DESCRIPTIONS

SCL: Serial Clock
The CAT24C21 serial clock input pin is used to clock all data transfers into or out of the device when in the bi-directional mode.

SDA: Serial Data/Address
The CAT24C21 bi-directional serial data/address pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-ORed with other open drain or open collector outputs.

VCLK: Serial Clock
The VCLK serial clock input pin is used to clock data out of the device when in transmit-only mode.

BI-DIRECTIONAL MODE (DDC2)

The following defines the features of the I^2C bus protocol when in the bi-directional mode:

(1) Data transfer may be initiated only when the bus is not busy.

(2) During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock line is high will be interpreted as a START or STOP condition.

When in the Bi-directional mode, all inputs to the VCLK pin are ignored, except when a logic high is required to enable write capability.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT24C21 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

DEVICE ADDRESSING

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. The four most significant bits of the 8-bit slave address are fixed

Figure 2. Device Initialization for Transmit-only Mode

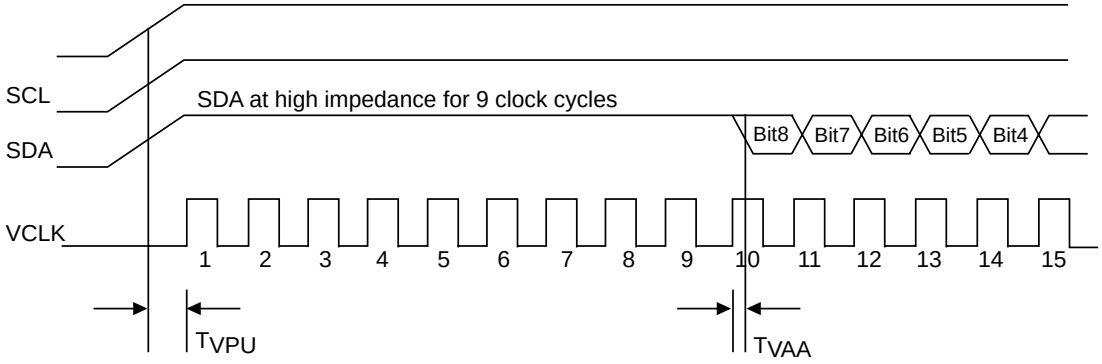
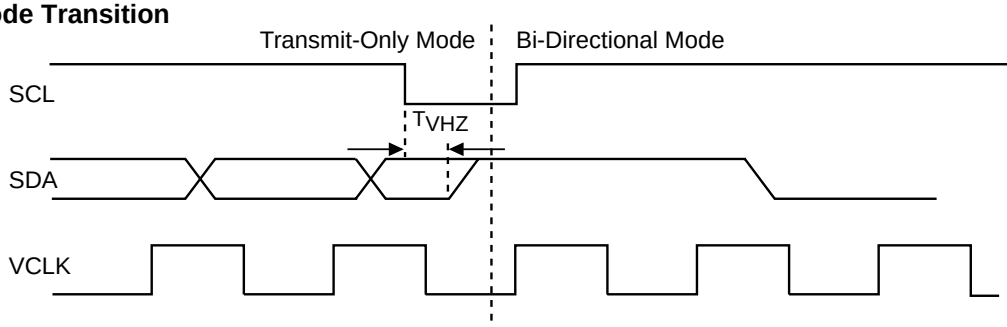


Figure 3. Mode Transition



as 1010 for the CAT24C21 (see Fig. 8). The next three significant bits are "don't care". The last bit of the slave address specifies whether a Read or Write operation is to be performed. When this bit is set to 1, a Read operation is selected, and when set to 0, a Write operation is selected.

After the Master sends a START condition and the slave address byte, the CAT24C21 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address. The CAT24C21 then performs a Read or Write operation depending on the state of the R/$\overline{W}$ bit.

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

The CAT24C21 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT24C21 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT24C21 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

Figure 4. Bus Timing

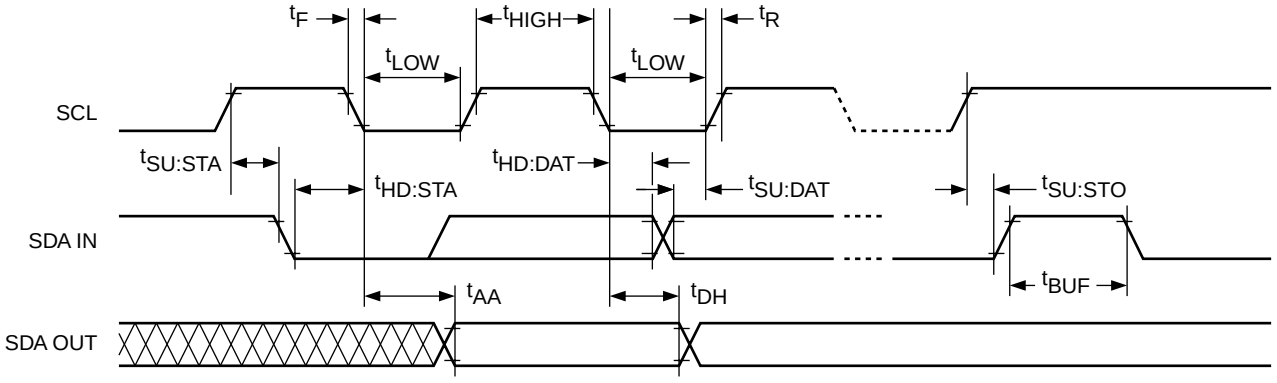
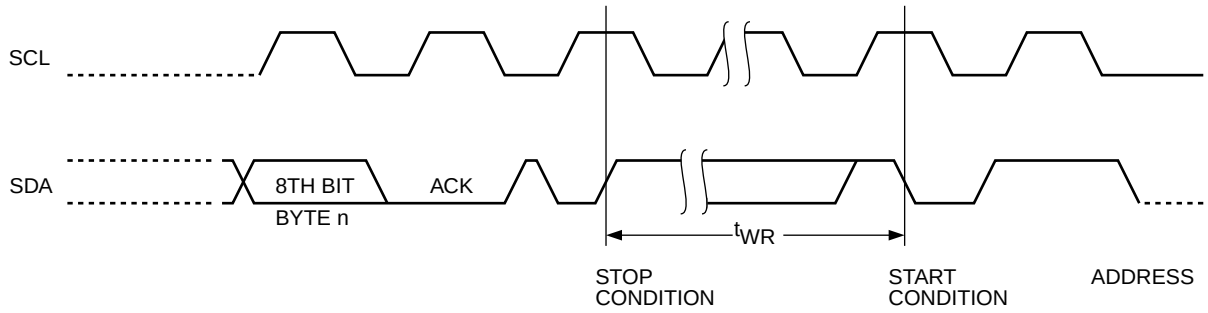


Figure 5. Write Cycle Timing



WRITE OPERATIONS

VCLK must be held high in order to program the device. This applies to byte write and page write operation. Once the device is in its self-timed program cycle, VCLK can go low and not affect programming.

Byte Write

In the Byte Write mode, the Master device sends the START condition and the slave address information (with the R/$\overline{W}$ bit set to zero) to the Slave device. After the Slave generates an acknowledge, the Master sends the byte address that is to be written into the address pointer of the CAT24C21. After receiving another acknowledge from the Slave, the Master device transmits the data byte to be written into the addressed memory location. The CAT24C21 acknowledge once more and the Master generates the STOP condition, at which time the device begins its internal programming cycle to nonvolatile memory. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Page Write

The CAT24C21 writes up to 16 bytes of data in a single write cycle, using the Page Write operation. The Page Write operation is initiated in the same manner as the Byte Write operation, however instead of terminating after the initial word is transmitted, the Master is allowed to send up to fifteen additional bytes. After each byte has been transmitted the CAT24C21 will respond with an acknowledge, and internally increment the low order address bits by one. The high order bits remain unchanged.

If the Master transmits more than sixteen bytes prior to sending the STOP condition, the address counter 'wraps around', and previously transmitted data will be overwritten.

Once all sixteen bytes are received and the STOP condition has been sent by the Master, the internal programming cycle begins. At this point all received data is written to the CAT24C21 in a single write cycle.

Figure 6. Start/Stop Timing

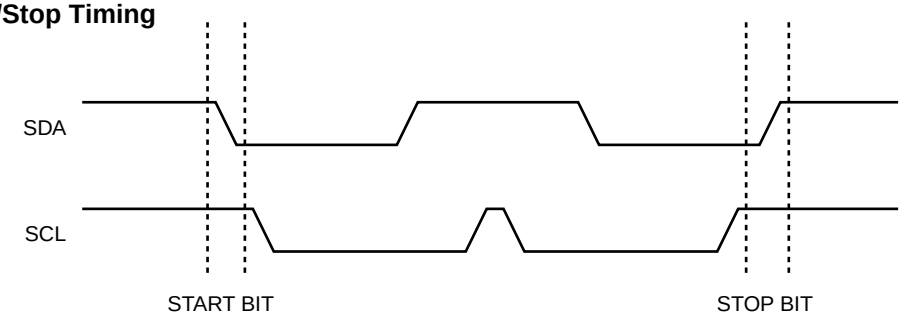


Figure 7. Acknowledge Timing

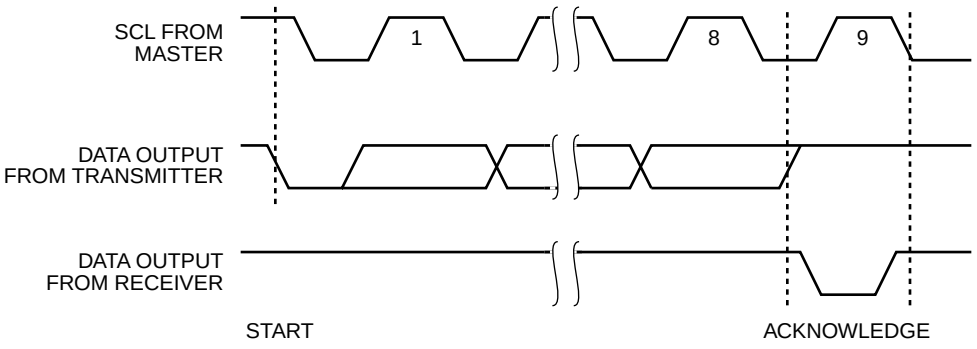


Figure 8. Slave Address Bits

CAT24C21

1	0	1	0	X	X	X	R/$\overline{W}$

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT24C21 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address for a write operation. If the CAT24C21 is still busy with the write operation, no ACK will be returned. If the CAT24C21 has completed the write operation, an ACK will be returned and the host can then proceed with the next read or write operation.

WRITE PROTECTION

When the VCLK pin is connected to GND and the CAT24C21 is in the bi-directional mode, the entire memory is protected and becomes "read only".

READ OPERATIONS

The READ operation for the CAT24C21 is initiated in the same manner as the write operation with the one exception that the R/$\overline{W}$ bit is set to a one. Three different READ operations are possible: Immediate Address READ, Selective READ and Sequential READ.

Immediate Address Read

The CAT24C21's address counter contains the address of the last byte accessed, incremented by one. In other words, if the last READ or WRITE access was to address N, the READ immediately following would access data from address N+1. If N=127, then the counter will 'wrap around' to address 0 and continue to clock out data.

Figure 9. Byte Write Timing

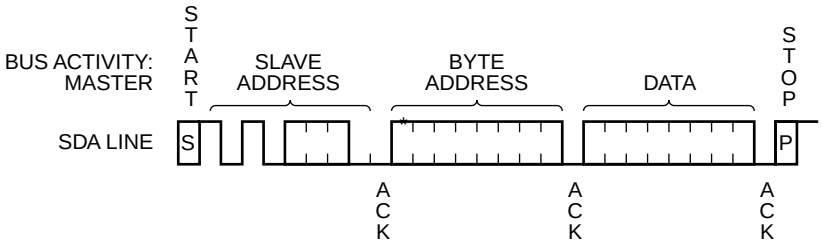
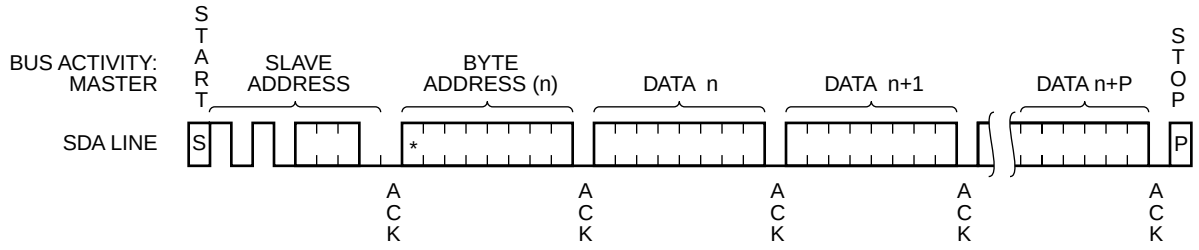


Figure 10. Page Write Timing



NOTE: IN THIS EXAMPLE n = XXXX 0000(B); X = 1 or 0

P=7 for CAT24WC01 and P=15 for CAT24WC02/04/08/16
* = Don't care for CAT24WC01

Selective Read

Selective READ operations allow the Master device to select at random any memory location for a READ operation. The Master device first performs a 'dummy' write operation by sending the START condition, slave address and byte address of the location it wishes to read. After the CAT24C21 acknowledge the word address, the Master device resends the START condition and the slave address, this time with the R/$\overline{W}$ bit set to one. The CAT24C21 then responds with its acknowledge and sends the 8-bit byte requested. The master device does not send an acknowledge but will generate a STOP condition.

Sequential Read

The Sequential READ operation can be initiated by either the immediate Address READ or Selective READ operations. After the 24WC01/02/04/08/16 sends initial 8-bit byte requested, the Master will respond with an acknowledge which tells the device it requires more data. The CAT24C21 will continue to output an 8-bit byte for each acknowledge sent by the Master. The operation is terminated when the Master fails to respond with an acknowledge, thus sending the STOP condition.

The data being transmitted from the CAT24C21 is outputted sequentially with data from address N followed by data from address N+1. The READ operation address counter increments all of the CAT24C21 address bits so that the entire memory array can be read during one operation. If more than the 128 bytes are read out, the counter will "wrap around" and continue to clock out data bytes.

Figure 11. Immediate Address Read Timing

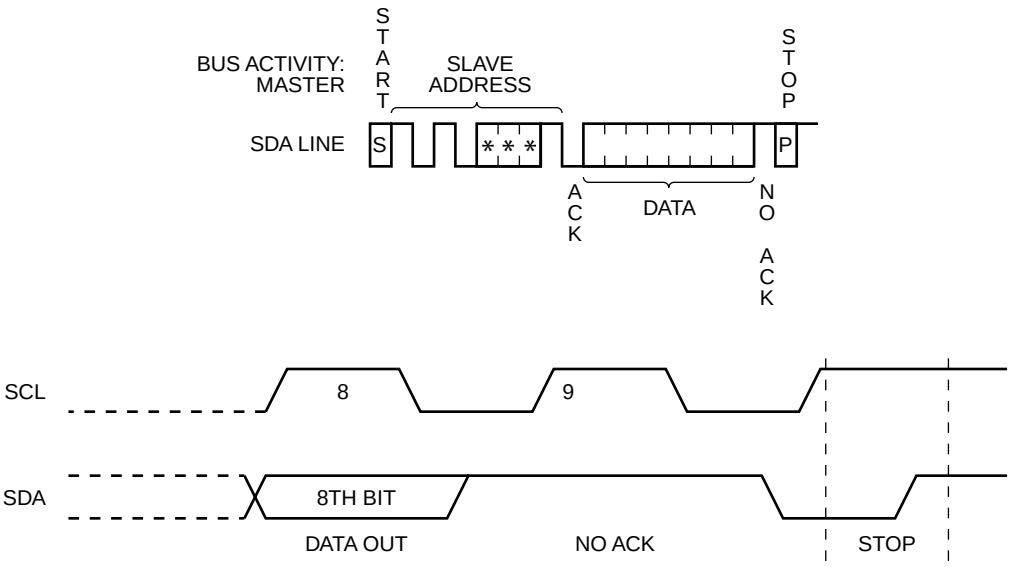


Figure 12. Selective Read Timing

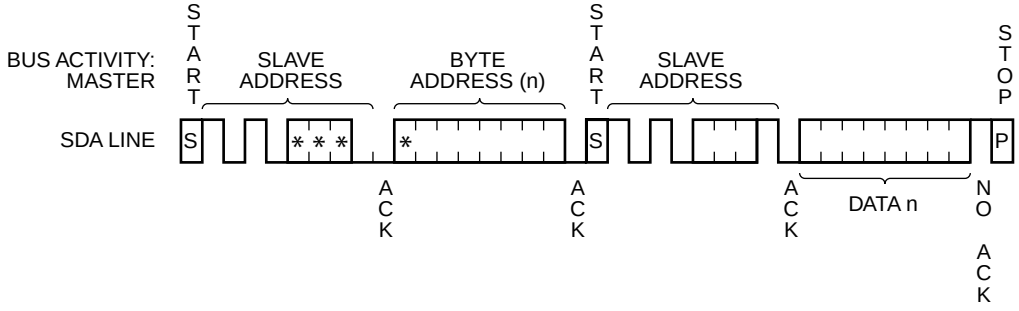
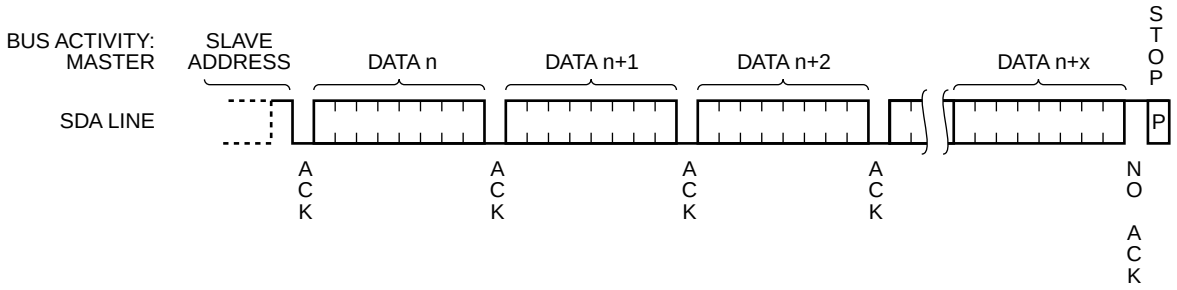
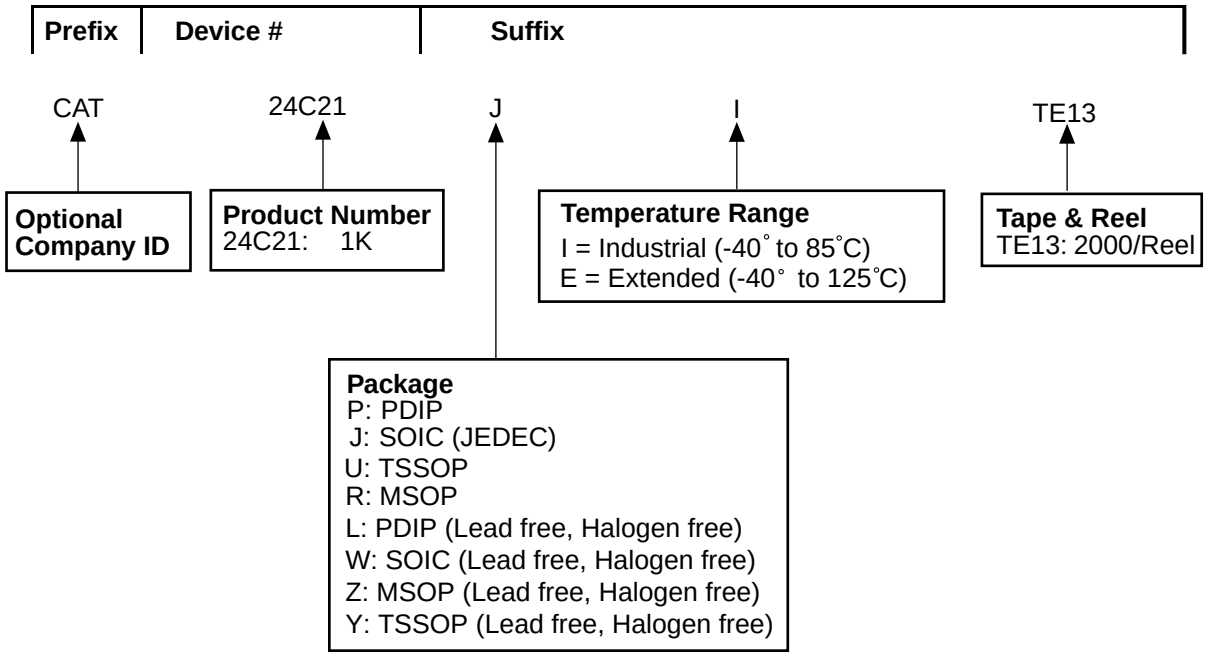


Figure 13. Sequential Read Timing



ORDERING INFORMATION



Notes:
(1) The device used in the above example is a CAT24C21JITE13 (SOIC, Industrial Temperature, 2.5 Volt to 5.5 Volt Operating Voltage, Tape & Reel)

Copyrights, Trademarks and Patents
Trademarks and registered trademarks of Catalyst Semiconductor include each of the following:

DPP ™ AE² ™

I²C is a trademark of Philips.

DDC, DDC1, DDC2 and VESA are trademarks of the Video Electronics Standards Association.

Catalyst Semiconductor has been issued U.S. and foreign patents and has patent applications pending that protect its products. For a complete list of patents issued to Catalyst Semiconductor contact the Company's corporate office at 408.542.1000.

CATALYST SEMICONDUCTOR MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE, EXPRESS OR IMPLIED, REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR THAT THE USE OF ITS PRODUCTS WILL NOT INFRINGE ITS INTELLECTUAL PROPERTY RIGHTS OR THE RIGHTS OF THIRD PARTIES WITH RESPECT TO ANY PARTICULAR USE OR APPLICATION AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY ARISING OUT OF ANY SUCH USE OR APPLICATION, INCLUDING BUT NOT LIMITED TO, CONSEQUENTIAL OR INCIDENTAL DAMAGES.

Catalyst Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Catalyst Semiconductor product could create a situation where personal injury or death may occur.

Catalyst Semiconductor reserves the right to make changes to or discontinue any product or service described herein without notice. Products with data sheets labeled "Advance Information" or "Preliminary" and other products described herein may not be in production or offered for sale.

Catalyst Semiconductor advises customers to obtain the current version of the relevant product information before placing orders. Circuit diagrams illustrate typical semiconductor applications and may not be complete.

Catalyst Semiconductor, Inc.
Corporate Headquarters
1250 Borregas Avenue
Sunnyvale, CA 94089
Phone: 408.542.1000
Fax: 408.542.1200
www.catalyst-semiconductor.com

Publication #: 1032
Revison: G
Issue date: 5/9/03
Type: Preliminary