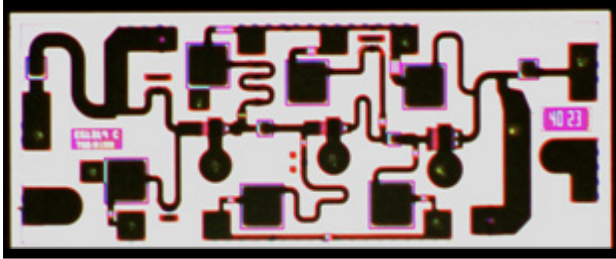


K Band Wideband LNA/Driver

TGA1319C



Chip Dimensions 2.179 mm x .847 mm

Key Features and Performance

- 0.15um pHEMT Technology
- 16-30 GHz Frequency Range
- 2.5 dB Nominal Noise Figure midband
- 21 dB Nominal Gain
- 14 dBm Pout

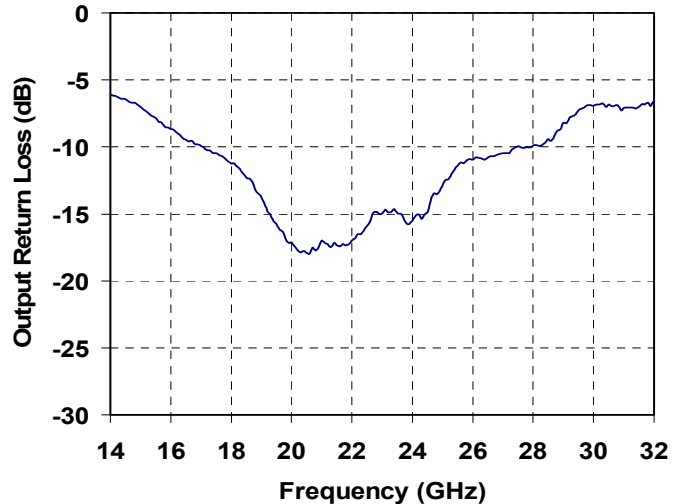
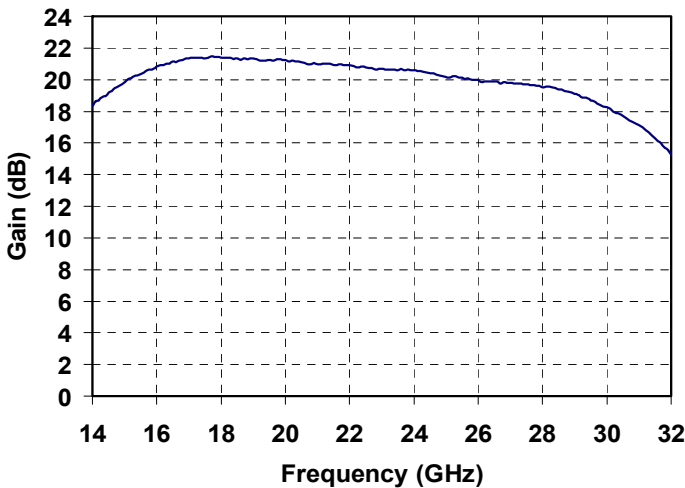
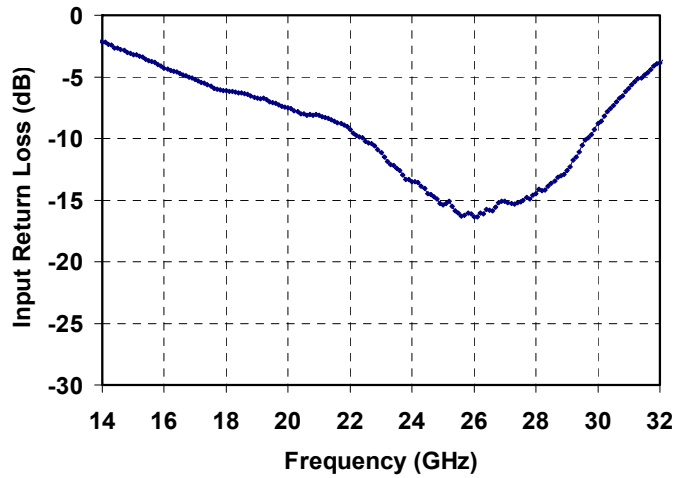
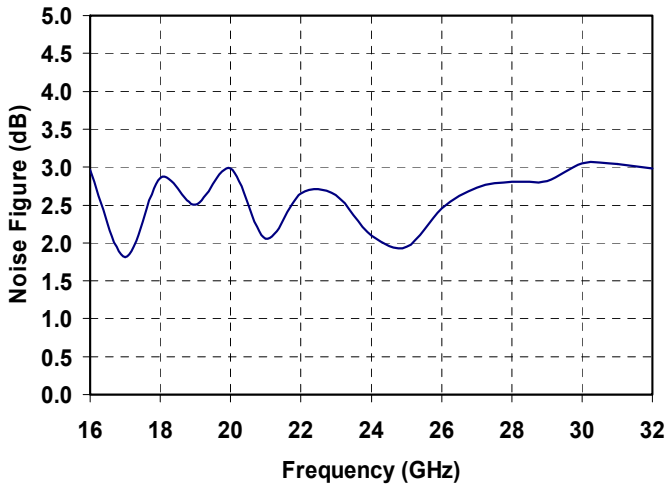
- Bias 5V, 60 mA with $-0.5V < V_g < +0.5V$

Primary Applications

- Point-to-Point Radio
- Point-to-Multipoint Communications

Measured Fixtured Data

Bias: $V_d = 5V, I_d = 60mA$



Note: Datasheet is subject to change without notice.

MAXIMUM RATINGS

SYMBOL	PARAMETER ^{4/}	VALUE	NOTES
V ⁺	POSITIVE SUPPLY VOLTAGE	9 V	
I ⁺	POSITIVE SUPPLY CURRENT	80 mA	<u>1/</u>
I ⁻	NEGATIVE GATE CURRENT	5.28 mA	
P _{IN}	INPUT CONTINUOUS WAVE POWER	15 dBm	
P _D	POWER DISSIPATION	.72 W	
T _{CH}	OPERATING CHANNEL TEMPERATURE	150 °C	<u>2/</u> <u>3/</u>
T _M	MOUNTING TEMPERATURE (30 SECONDS)	320 °C	
T _{STG}	STORAGE TEMPERATURE	-65 to 150 °C	

- 1/ Total current for all stages.
- 2/ These ratings apply to each individual FET.
- 3/ Junction operating temperature will directly affect the device median time to failure (T_M). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.
- 4/ These ratings represent the maximum operable values for the device.

DC PROBE TESTS

(T_A = 25 °C ± 5°C)

Symbol	Parameter	Minimum	Maximum	Value
I _{DSS}	Saturated Drain Current	---	---	mA
V _P	Pinch-off Voltage	-1.5	-0.5	V
BVGS	Breakdown Voltage gate-source	---	---	V
BVGD	Breakdown Voltage gate-drain	---	---	V

ON-WAFER RF PROBE CHARACTERISTICS

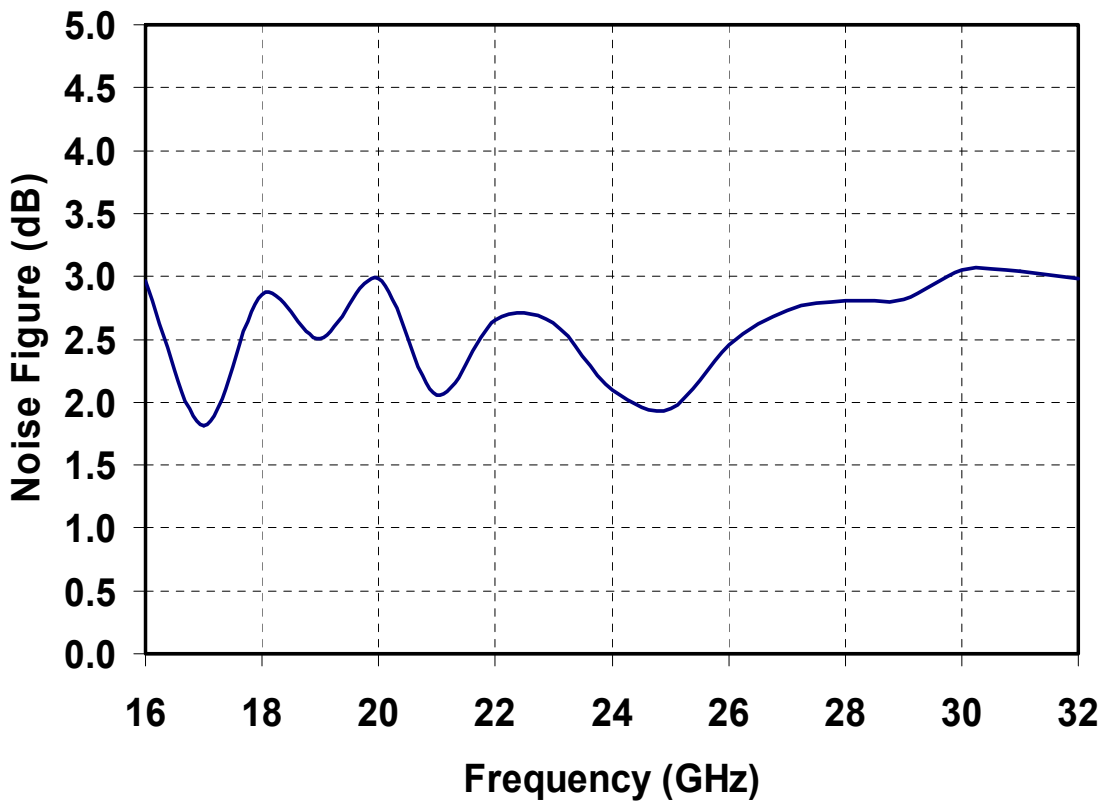
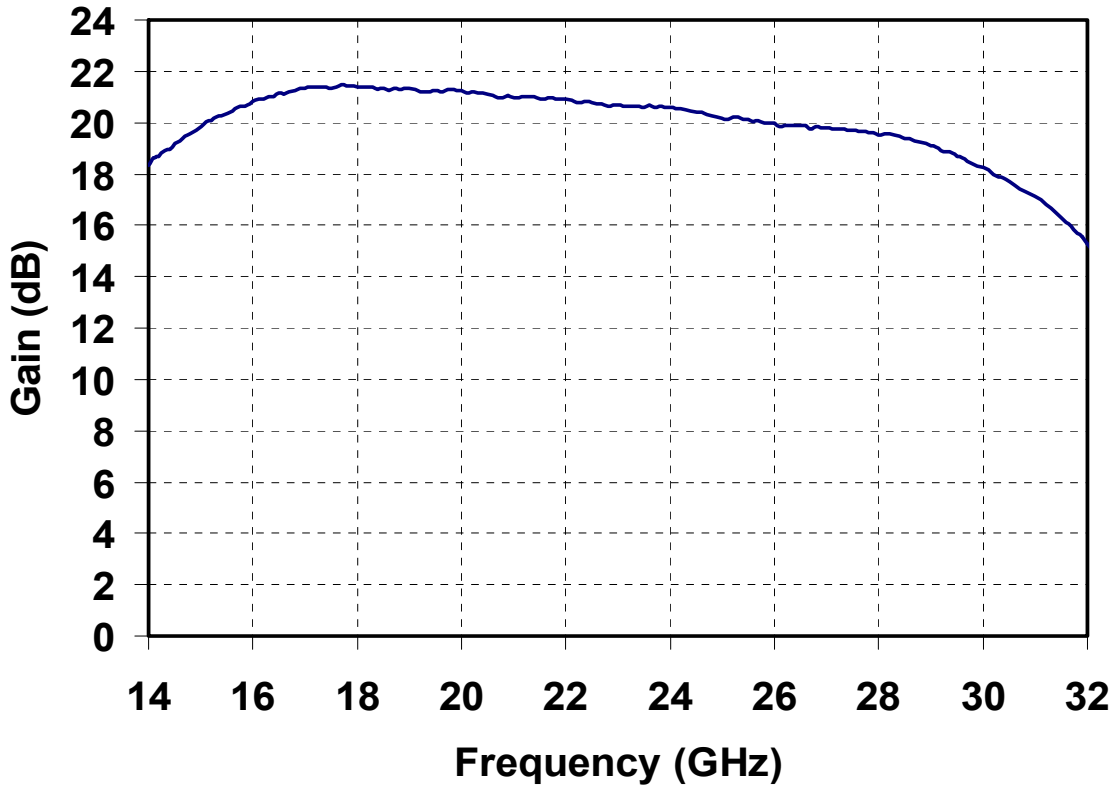
(T_A = 25 °C ± 5°C)

V_d = 5 V, I_{d1} = 60 mA

Symbol	Parameter	Test Condition	Limit			Units
			Min	Typ	Max	
Gain	Small Signal Gain	F = 21 – 27 GHz	19		---	dB
NF	Noise Figure	F = 21 – 25 GHz F = 26 – 26.5 GHz	---		2.5 2	dB
PWR	Output Power @ P1dB	F = 21 – 26 GHz F = 27 GHz	10 9		---	dBm

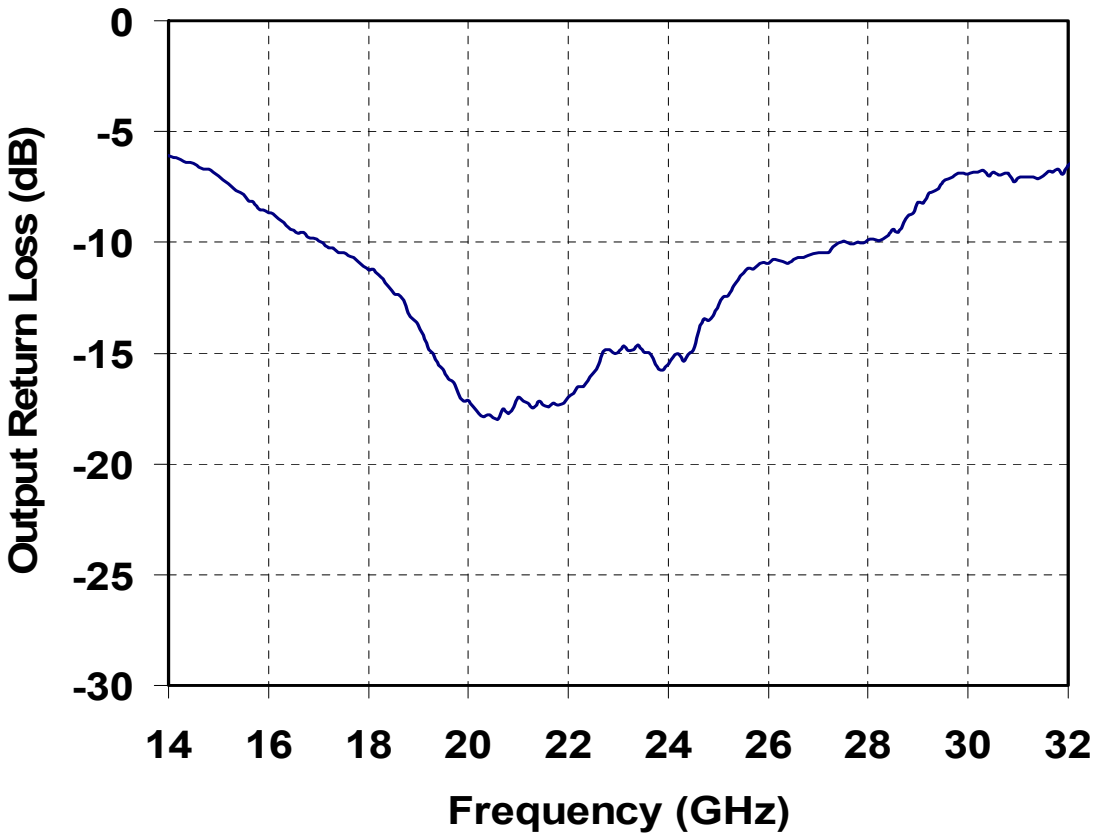
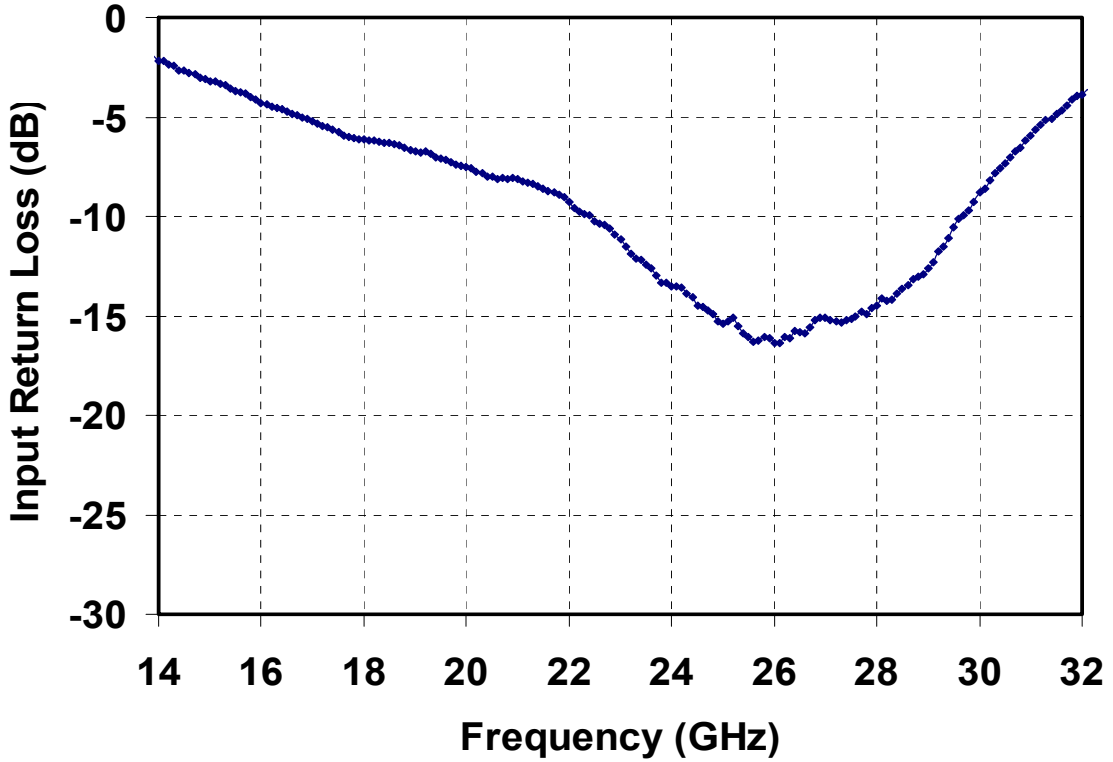
Measured Fixtured Data

Bias: $V_d = 5V$, $I_d = 60mA$

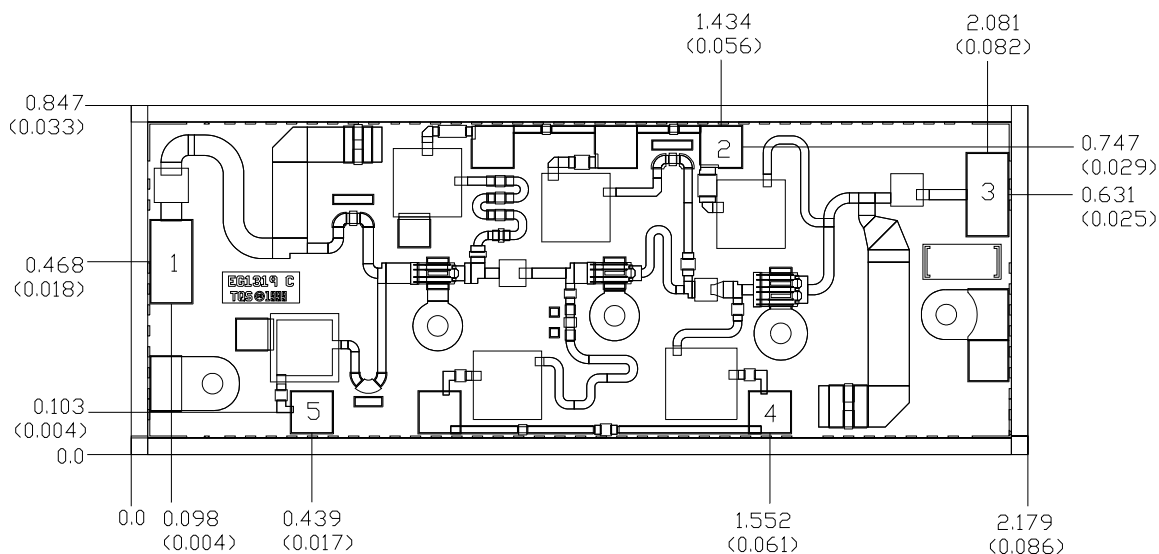


Measured Fixtured Data

Bias: $V_d = 5V$, $I_d = 60mA$



Mechanical Drawing



Units: millimeters (inches)

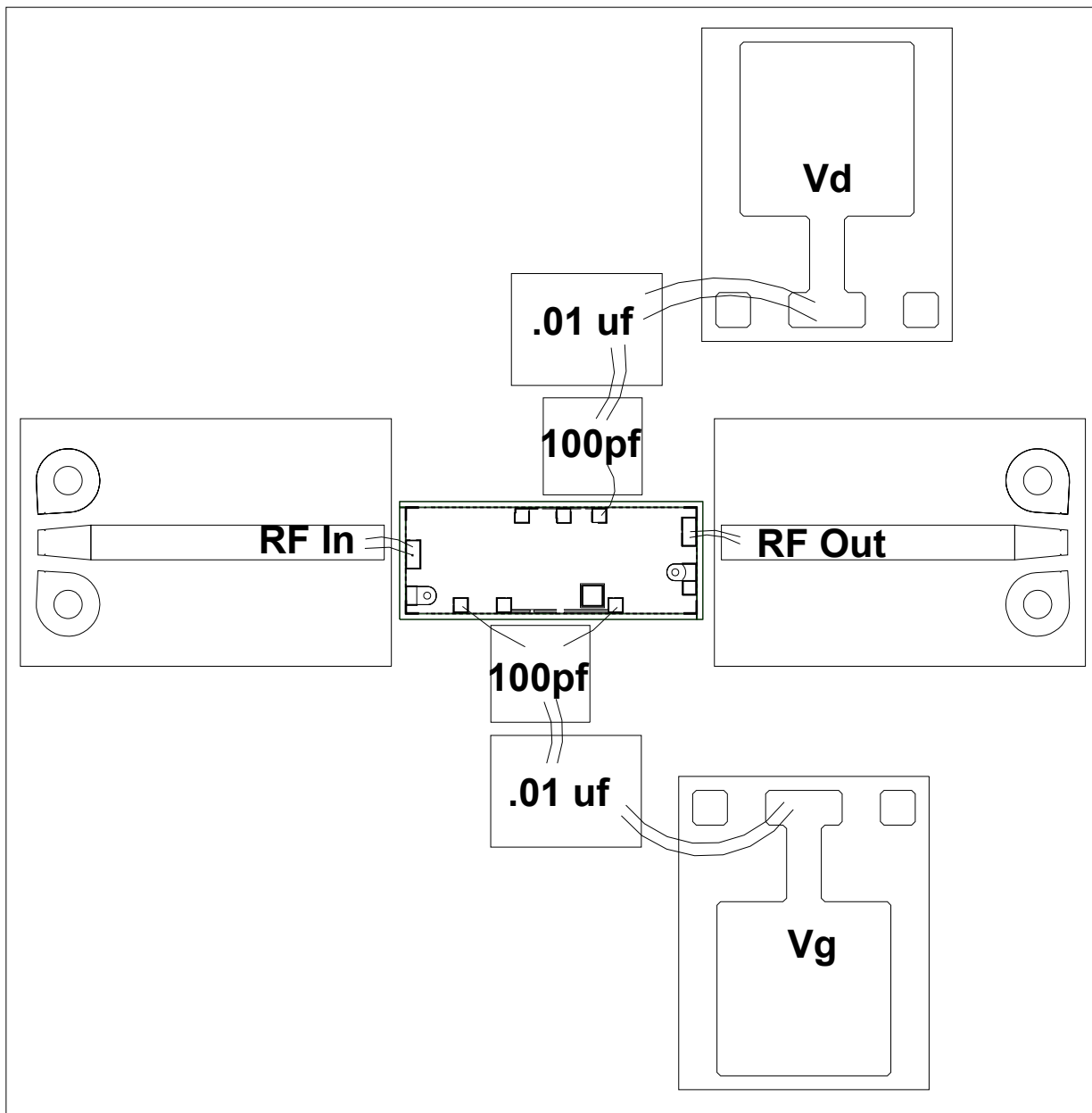
Thickness: 0.1016 (0.004)

Chip edge to bond pad dimensions are shown to center of bond pad

Chip size tolerance: +/- 0.051 (0.002)

Bond Pad #1 (RF Input)	0.100 x 0.200 (0.004 x 0.008)
Bond Pad #2 (Vd)	0.100 x 0.100 (0.004 x 0.004)
Bond Pad #3 (RF Output)	0.100 x 0.200 (0.004 x 0.008)
Bond Pad #4 (Vg2)	0.100 x 0.100 (0.004 x 0.004)
Bond Pad #5 (Vg1)	0.100 x 0.100 (0.004 x 0.004)

Recommended Chip Assembly Diagram



Assembly Process Notes

Reflow process assembly notes:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300⁰C (30 seconds max).
- An alloy station or conveyor furnace with reducing atmosphere should be used.
- No fluxes should be utilized.
- Coefficient of thermal expansion matching is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.

Component placement and adhesive attachment assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- The force impact is critical during auto placement.
- Organic attachment can be used in low-power applications.
- Curing should be done in a convection oven; proper exhaust is a safety concern.
- Microwave or radiant curing should not be used because of differential heating.
- Coefficient of thermal expansion matching is critical.

Interconnect process assembly notes:

- Thermosonic ball bonding is the preferred interconnect technique.
- Force, time, and ultrasonics are critical parameters.
- Aluminum wire should not be used.
- Maximum stage temperature is 200⁰C.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.