SGS-THOMSON MICROELECTRONICS

T74LS160A/161A T74LS162A/163A

LS160A/162A : BCD DECADE COUNTERS
LS161A/163A : 4-BIT BINARY COUNTERS

T-45-23-05

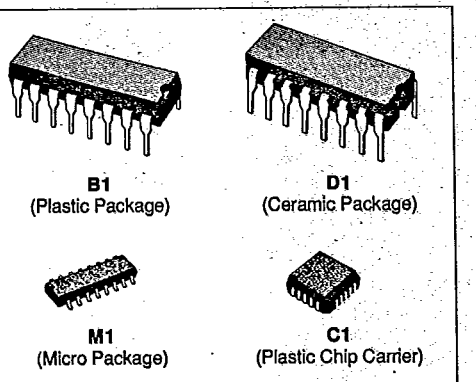
- SYNCHRONOUS COUNTING AND LOADING
- TWO COUNT ENABLE INPUTS FOR HIGH-SPEED SYNCHRONOUSLY EXPANSION
- EDGE-TRIGGERED OPERATION
- TYPICAL COUNT RATE OF 35 MHz
- FULLY TTL AND CMOS COMPATIBLE

DESCRIPTION

The LS160A/161A/162A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building, blocks for counting, memory addressing, frequency division and other applications. The LS160A and LS162A count modulo 10 (BCD). The LS161A and LS163A count modulo 16 (binary).

The LS160A and LS161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162A and LS163A have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD Modulo 10	Binary (modulo 16)
Asynchronous Reset	LS160A	LS161A
Synchronous Reset	LS162A	LS163A



B1 (Plastic Package)

D1 (Ceramic Package)

M1 (Micro Package)

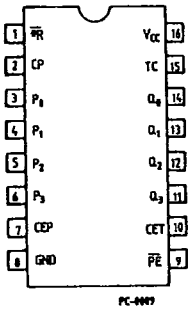
C1 (Plastic Chip Carrier)

ORDER CODES :

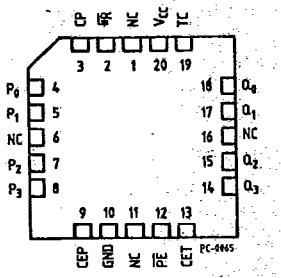
T74LSXXXX D1 T74LSXXXX C1
T74LSXXXX B1 T74LSXXXX M1

PIN CONNECTION (top view)

DUAL IN LINE



CHIP CARRIER



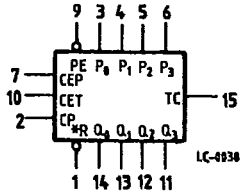
* MR for LS160A/161A
* SR for LS162A/163A
NC = No Internal Connection

PIN NAMES

$\overline{PE}$	PARALLEL ENABLE (active LOW) INPUT
$P_0 - P_3$	PARALLEL INPUTS
CEP	COUNT ENABLE PARALLEL INPUT
CET	COUNT ENABLE TICKLE INPUT
CP	CLOCK (avtive HIGH going edge) INPUT
$\overline{MR}$	MASTER RESET (active LOW) INPUT
$\overline{SR}$	SYNCHRONOUS RESET (active LOW) INPUT
$Q_0 - Q_3$	PARALLEL OUTPUTS
TC	TERMINAL COUNT OUTPUT

LOGIC SYMBOL AND TRUTH TABLE

* $\overline{MR}$ for LS160A/161A
* $\overline{SR}$ for LS162A/163A



V_{CC} = Pin 16
GND = Pin 8

*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge
L	X	X	X	Reset (clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (increment)
H	H	L	X	No Change (hold)
H	H	X	L	No Change (hold)

* For the LS162A and LS163A only

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.5 to 7	V
V_I	Input Voltage, Applied to Input	− 0.5 to 15	V
V_O	Output Voltage, Applied to Output	− 0.5 to 10	V
I_I	Input Current, into Inputs	− 30 to 5	mA
I_O	Output Current, into Outputs	50	mA

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGE

Part Numbers	Supply Voltage			Temperature
	Min.	Typ.	Max.	
T74LS160A/161A/162A/163AXX	4.75 V	5.0 V	5.25 V	0 °C to + 70 °C

XX = package type.

FUNCTIONAL DESCRIPTION

The LS160A/161A/162A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. These counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160A and LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs - Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) - select the mode of operation as shown in the tables. The Count Mode is enabled when the CEP, CET, and $\overline{PE}$ inputs are HIGH.

When the $\overline{PE}$ is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET inputs can be used to inhibit the count sequence. With the PE held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET-CEP) allows synchronous cascading without external gating and without delay accumulation over any pratical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

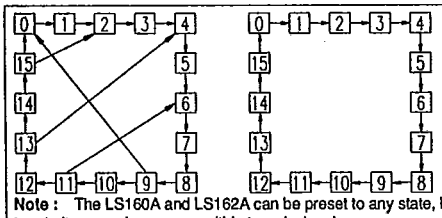
The LS160A and LS162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do not generated a TC output.

The LS161A and LS163A count modulo 16 following a binary sequence. They generated a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the LS160A and LS161A is asynchronous. When the $\overline{MR}$ is LOW, it overrides all other input conditions and sets the outputs LOW. The $\overline{MR}$ pin should never be left open. If not used, the $\overline{MR}$ pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Sinchronous Reset ($\overline{SR}$) input of the LS162A and LS163A acts as an edge-triggered control input, overriding CET, CEP and $\overline{PE}$, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g. to reset the counter synchronously after reaching a predetermined value.

STATE DIAGRAM



LOGIC EQUATIONS

Count Enable = CEP•CET•PE
TC for LS160A & LS162A = CET • Q_0 • $\overline{Q_1}$ • $\overline{Q_2}$ • Q_3
TC for LS161A & LS163A = CET • Q_0 • Q_1 • Q_2 • Q_3
Preset = $\overline{PE}$ • CP + (rising clock edge)
Reset = $\overline{MR}$ (LS160A & LS161A)
Reset = $\overline{SR}$ • CP + (rising clock edge (LS162A & LS163A))

Note : The LS160A and LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14 or 15, it will return to its normal sequence within two clock pulses.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Symbol	Parameter	Limits			Test Condition (note 1)		Unit
		Min.	Typ. (*)	Max.			
V_{IH}	Input HIGH Voltage	2.0			Guaranteed Input HIGH Voltage for All Inputs		V
V_{IL}	Input LOW Voltage			0.8	Guaranteed Input LOW Voltage for All Inputs		V
V_{CD}	Input Clamp Diode Voltage		- 0.65	- 1.5	V_{CC} = MIN, I_{IN} = -18 mA		V
V_{OH}	Output HIGH Voltage	2.7	3.4		V_{CC} = MIN, I_{OH} = - 400 µA V_{IN} = V_{IH} or V_{IL} per Truth Table		V
V_{OL}	Output LOW Voltage		0.25	0.4	I_{OL} = 4.0 mA	V_{CC} = MIN, V_{IN} = V_{IH} or V_{IL} per Truth Table	V
			0.35	0.5	I_{OL} = 8.0 mA		V
I_{IH}	Input HIGH Current MR, Data CEP Clock PE CET (LS160A/161A)			20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	MR, Data CEP Clock PE CET (LS160A/161A)			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
	Data, CEP, Clock PE, CET, SR (LS162A/163A)			20 40	V_{CC} = MAX, V_{IN} = 2.7 V		µA
	Data, CEP, Clock PE, CET, SR (LS162A/163A)			0.1 0.2	V_{CC} = MAX, V_{IN} = 7.0 V		mA
I_{IL}	Input LOW Current MR, Data CEP Clock PE CET (LS160A/161A)			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
	Data, CEP, Clock PE, CET, SR (LS162A/163A)			- 0.4 - 0.8	V_{CC} = MAX, V_{IN} = 0.4 V		mA
I_{OS}	Output Short Circuit Current (note 2)	- 20		- 100	V_{CC} = MAX, V_{OUT} = 0 V		mA
I_{CCH} I_{CCL}	Power Supply Current		18 19	31 32	VCC = MAX		mA

Notes : 1. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
2. Not more than one output should be shorted at a time.
(*) Typical values are at V_{CC} = 5.0 V, T_A = 25 °C.

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Tests Conditions	Unit
		Min.	Typ.	Max.		
t_{PLH} t_{PHL}	Propagation Delay, Clock to TC		20 18	35 35	V_{CC} = 5.0 V C_L = 15 pF	ns
t_{PLH} t_{PHL}	Propagation Delay, Clock to Q		13 18	24 27		ns
t_{PLH} t_{PHL}	Propagation Delay, CET to TC		9.0 9.0	14 14		ns
t_{PHL}	MR or SR to Q		20	28		ns
f_{MAX}	Maximum Clock Frequency	25	32			MHz

AC CHARACTERISTICS : T_A = 25 °C

Symbol	Parameter	Limits			Test Conditions	Unit
		Min.	Typ.	Max.		
t_WCP	Clock Pulse Width	25			V_{CC} = 5.0 V	ns
t_W	$\overline{MR}$ or SR Pulse Width	20				ns
t_s	Set-up Time, any Input	20				ns
t_h	Hold Time, any Input	0				ns

DEFINITION OF TERMS

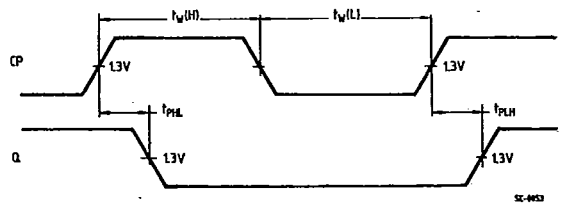
SET-UP-TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) - is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognized and transfer HIGH Data to the Q outputs.

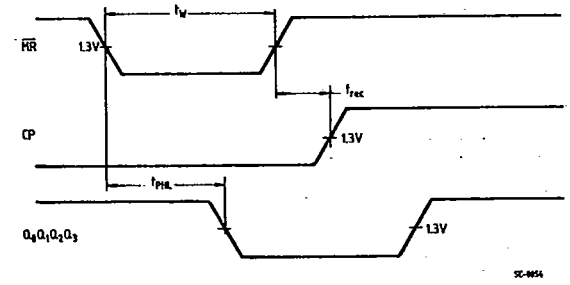
AC WAVEFORMS

Figure 1 :Clock to Output Delays, Count Frequency, and Clock Pulse Width.



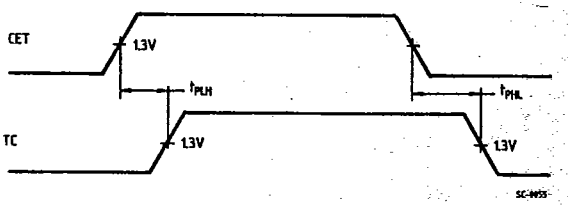
Other Conditions :
$\overline{PE}$ = $\overline{MR}$ ($\overline{SR}$) = H CEP = CET = H

Figure 2 :Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery



Other Conditions : $\overline{PE}$ = L
$P_0 = P_1 = P_2 = P_3$ = H

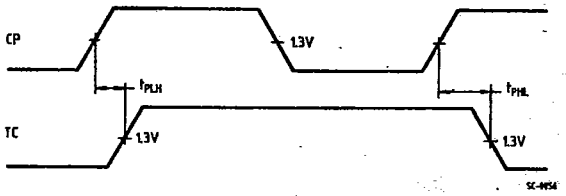
Figure 3 :Count Enable Trickle Input to Terminal Count Output Delays.



The positive TC pulse occurs when the outputs are in the ($Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$) state for the LS160A and LS162A and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the LS161A and LS163A.

Other Conditions :
$\overline{CP} = \overline{PE} = CEP = \overline{MR} = H$

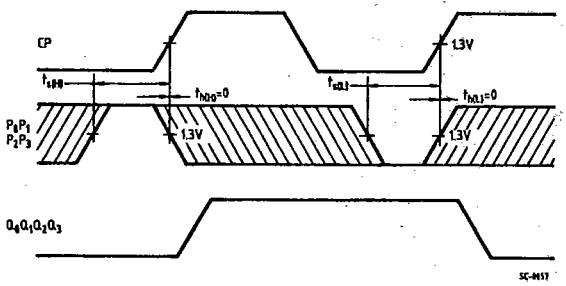
Figure 4 :Clock to Terminal Count Delays.



The positive TC pulse in coincident with the output state ($Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3$) state for the LS160A and LS162A and the ($Q_0 \bullet Q_1 \bullet Q_2 \bullet Q_3$) state for the LS161A and LS163A.

Other Conditions :
$\overline{PE} = CEP = \overline{CET} = \overline{MR} = H$

Figure 5 :Set-up Time (t_s) and Hold Time (t_h) for Parallel Data Inputs.



Other Conditions : $\overline{PE} = L$, $\overline{MR} = H$

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 6 :Set-up Time (t_s) and Hold Time (t_h) for Count Enable (CEP) and (CET) and Parallel Enable ($\overline{PE}$) Inputs.

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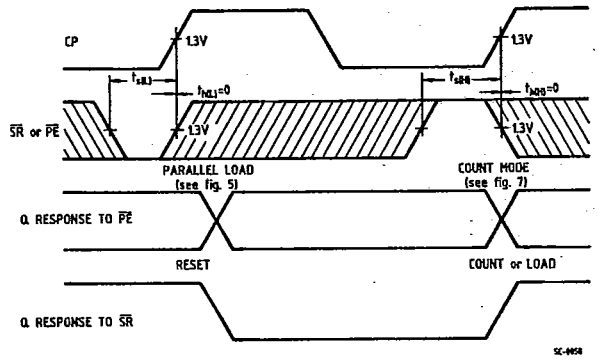
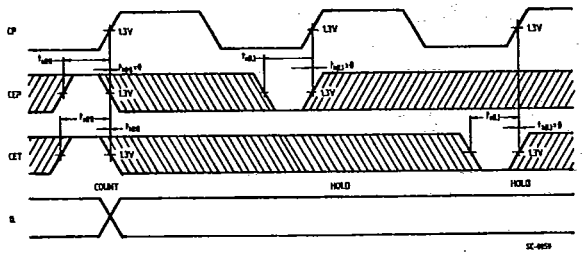


Other Conditions : $\overline{PE}$ = L, $\overline{MR}$ = H

The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 7.



Other Conditions : $\overline{PE}$ = L, $\overline{MR}$ = H