NJMDAC-08

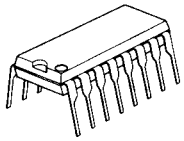
NJMDAC-08 series are 8-bit monolithic multiplying digital to analog converters with very high speed perfomance. Open collector output provides dual complementary current outputs increasing versatility in application. Adjustable threshold logic input voltage through V_{LC} pin, can be connected to various type of digital IC products.

■ Features

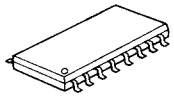
Resolution	8bit
Settling Time	85ns
Linearity Error	±0.1%FS MAX (NJM DAC−08H)
Full Scale Current Temperature Drift	50ppm/℃ MAX (NJM DAC−08H/E)
Wide Power Supply Range	±5V～±18V
Wide Output Voltage Range	−10V～+18V
Wide Range Adjustable Threshold Logic Input	−10V～+13.5 (V^+/V^-=±15V)
Multiplying operations can be performed	

■ Package Outline

16pin Plastic DIP

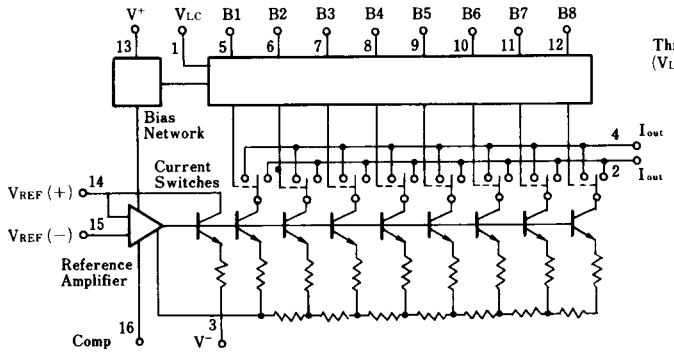


16pin Plastic DMP

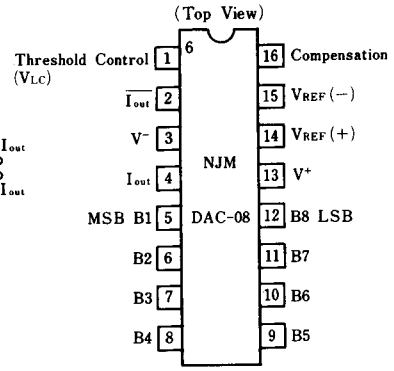


N L	Ceramic DIP	Plastic DIP	Plastic DMP
0.1%	NJM DAC-08JH	NJM DAC-08DH	NJM DAC-08MH
0.19%	NJM DAC-08JE	NJM DAC-08DE	NJM DAC-08ME
0.39%	NJM DAC-08JC	NJM DAC-08DC	NJM DAC-08MC

■ Block Diagram



■ Connection Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Parameters	Symbols	Ratings	Units
Supply Voltage	V^+-V^-	36	V
Logic Input Voltage Range	V_I	V^-～V^-+36	V
Threshold Control Input Voltage	V_{LC}	V^-～V^+	V
Analog Current Outputs	I_O	4.2	mA
Reference Input Voltage Range	V_{REF}	V^-～V^+	V
Reference Input Differential Voltage	$V_{REF(+)}$-$V_{REF(-)}$	±18	V
Reference Input Current	I_{REF}	5.0	mA
Power Dissipation	P_D	500	mW
Operating Temperature Range	T_{opr}	−20～+75	℃
Storage Temperature Range	T_{stg}	−40～+125	℃

■ Electrical Characteristics ($V^+ = \pm 15$ V, $I_{REF} = 2.0$ mA, Ta = 25℃)

Parameter	Symbol	Test Condition	DAC-08H			DAC-08E			DAC-08C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Resolution			8	8	8	8	8	8	8	8	8	Bit
Monotonicity			8	8	8	8	8	8	8	8	8	Bit
Nonlinearity	NL				±0.1			±0.19			±0.39	%FS
*1 Settling Time	ts	To ±1/2LSB,all bits switched ON or OFF		85	135		85	150		85	150	ns
*1 Propagation Delay	tPLH tPHL	All bits switched		35	60		35	60		35	60	ns
*1 Full Scale Tempco	TCIFS			±10	±50		±10	±50		±10	±80	ppm/℃
Output Voltage Compliance	VOC	ΔIFS<1/2 LSB ROUT>20 MΩ typ.	−10		+18	−10		+18	−10		+18	V
Full Scale Current	IFS4	VREF=10.000V R14, R15=5.000kΩ	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Scale Symmetry	IFSS	IFS4−IFS2		±0.5	±4.0		±1.0	±8.0		±2.0	±16.0	μA
Zero Scale Current	IZS			0.1	1.0		0.2	2.0		0.2	4.0	μA
Output Current Range	IOR1	VREF=15 V, V⁻=10 V, R14, 15 ‖ 15.000 kΩ	2.1			2.1			2.1			mA
	IOR2	VREF=25 V, V⁻=12 V, R14, 15 ‖ 15.000 kΩ	4.2			4.2			4.2			mA
Logic Input Level "0"	VIL	VLC=0 V			0.8			0.8			0.8	V
〃 "1"	VIH	VLC=0 V	2.0			2.0			2.0			V
Logic Input Current "0"	IIL	VLC=0 V, VIN=−10 V~+0.8 V		−2.0	−10		−2.0	−10		−2.0	−10	μA
"1"	IIH	VLC=0 V, VIN=2 V~18 V		0.002	10		0.002	10		0.002	10	μA
Logic Input Swing	VIS		−10		+18	−10		+18	−10		+18	V
Logic Threshold Range	VTH2	———	−10		+13.5	−10		+13.5	−10		+13.5	V
Reference Bias Current	IIS			−1.0	−3.0		−1.0	−3.0		−1.0	−3.0	μA
*1 Reference Input Slew Rate	dI/dt		4.0	8.0		4.0	8.0		4.0	8.0		mA/μs
*2 Power Supply Sensitivity	PSSIFS	V⁻=4.5V~18V, IREF=1.0mA		±0.0003	±0.01		±0.0003	±0.01		±0.0003	±0.01	%/%
	PSSIFS	V⁻=−4.5V~18V, IREF=1.0mA		±0.002	±0.01		±0.002	±0.01		±0.002	±0.01	
*3 Power Supply Current	I⁺	V⁺=±5 V, IREF=1.0 mA		2.3	3.8		2.3	3.8		2.3	3.8	mA
	I⁻	〃		−4.3	−5.8		−4.3	−5.8		−4.3	−5.8	
	I⁺	V⁺=5 V, V⁻=−15 V		2.4	3.8		2.4	3.8		2.4	3.8	
	I⁻	〃		−6.4	−7.8		−6.4	−7.8		−6.4	−7.8	
	I⁺	———		2.5	3.8		2.5	3.8		2.5	3.8	
	I⁻	———		−6.5	−7.8		−6.5	−7.8		−6.5	−7.8	

*1 Guaranteed by design

*2 Caluculation formula $PSSI_{FS} = \left(\frac{|\Delta I_{FS}|}{I_{FS}} \times 100\right) \div \left(\frac{18-4.5}{15}\right) \times 100$

*3 Caluculation formula $P_D = I^+ \times (V^+ - V^-) + 2I_{REF} \times |V^-|$

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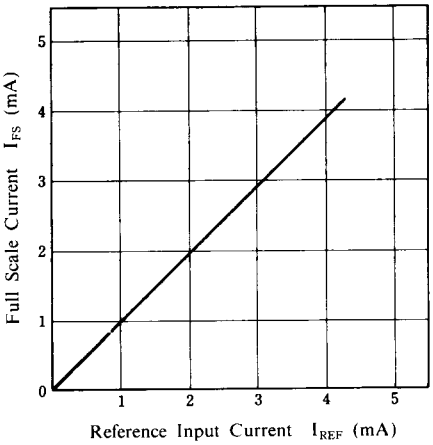
■ Typical Characteristics

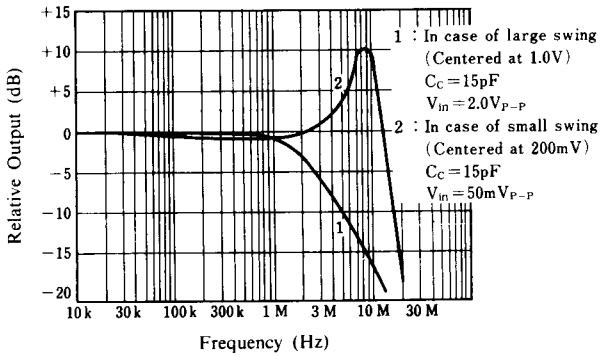
Full Scale Current vs. Reference Input Current

(All bits on, $V^- = -15V$)

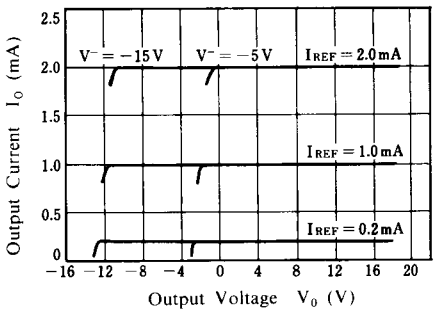


Reference Input Frequency Respons

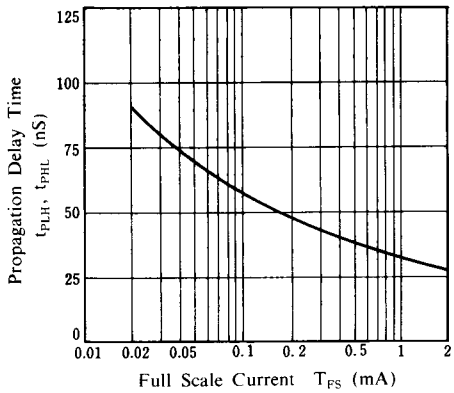
($R_{14}=R_{15}=1k\Omega$, $R_L=100\Omega$, ALL BITS "ON")



Output Current vs. Output Voltage

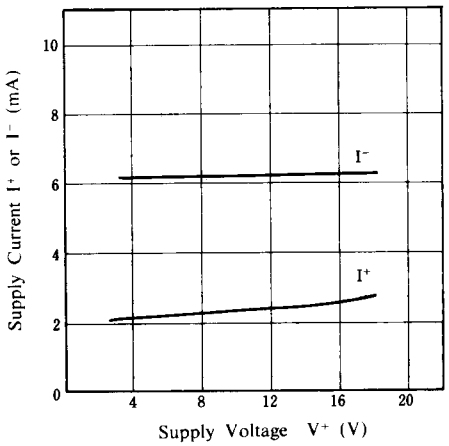


Propagation Delay Time vs. Full Scale Current



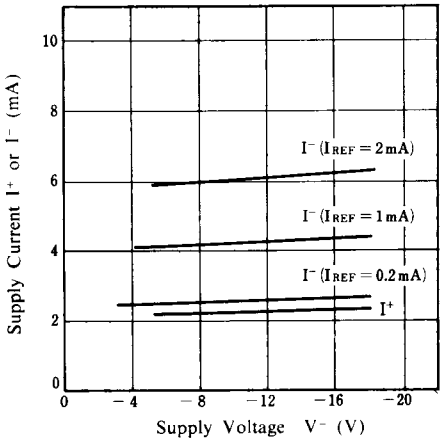
Supply Current vs. Supply Voltage

(ALL BITS "HIGH", OR "LOW")



Supply Current vs. Supply Voltage

(BITS MAY BE "HIGH" OR "LOW")



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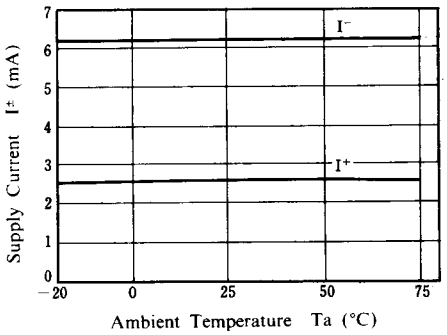
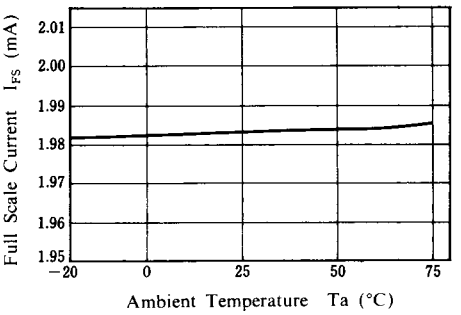
■ Typical Characteristics

Supply Current vs. Ambient Temperature

(I_{REF}=2mA)

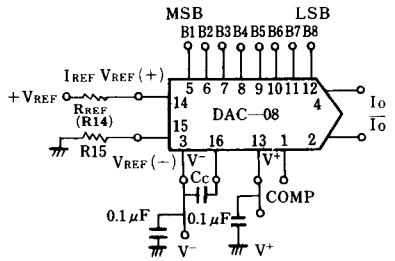


Full Scale Current vs. Ambient Temperature

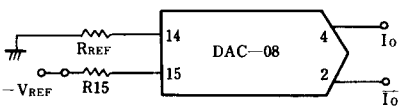


■ Typical Application

① Connecting Reference Voltage

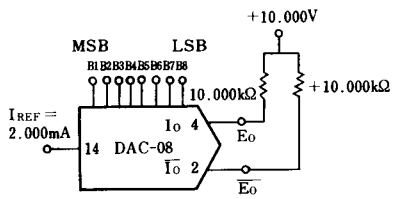


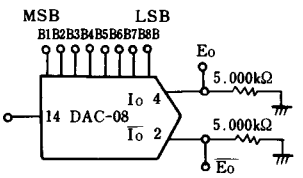
① Positive Reference Voltage
Minimum Compensation Capacitance
$C_C = R_{REF}(k\Omega) \times 15(pF)$



② Negative Reference Voltage
Recommended C_C Value
(When V_{REF} is DC)

② Connecting Output Circuit





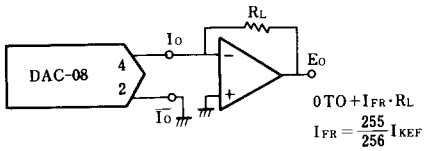
	B1	B2	B3	B4	B5	B6	B7	B8	Eo	Ēo
POS FULL RANGE	1	1	1	1	1	1	1	1	− 9.920	+10.000
POS FULL RANGE−LSB	1	1	1	1	1	1	1	0	− 9.840	+ 9.920
ZERO SCALE+LSB	1	0	0	0	0	0	0	1	− 0.050	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	+ 0.050
ZERO SCALE−LSB	0	1	1	1	1	1	1	1	+ 0.080	0.000
NEG FULL SCALE+LSB	0	0	0	0	0	0	0	1	+ 9.920	− 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	− 9.920

(1) Basic Bipolar Output Operation

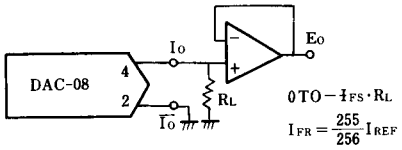
	B1	B2	B3	B4	B5	B6	B7	B8	I_{0mA}	$\bar{I}_{0mA}$	Eo	Ēo
FULL RANGE	1	1	1	1	1	1	1	1	1.992	0.000	−9.960	−0.000
HALF SCALE+LSB	1	0	0	0	0	0	0	1	1.008	0.984	−5.040	−4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	0.992	−5.000	−4.960
HALF SCALE−LSB	0	1	1	1	1	1	1	1	0.992	1.000	−4.960	−5.000
ZERO SCALE+LSB	0	0	0	0	0	0	0	1	0.008	1.984	−0.040	−9.920
ZERO SCALE	0	0	0	0	0	0	0	0	0.000	1.992	−0.000	−9.950

(2) Basic Unipolar Negative Operation

③ Connecting Output Buffer Amp.

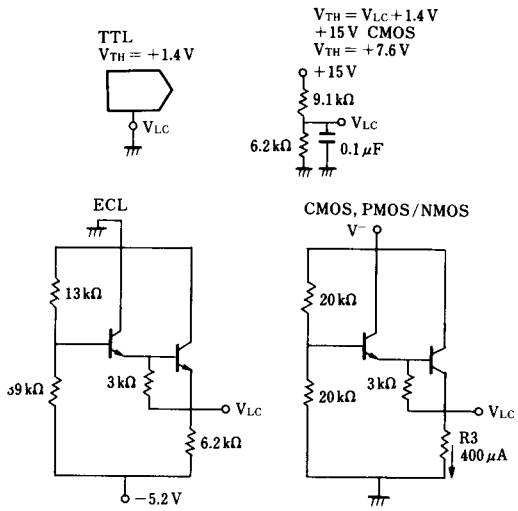


(1) Positive Low Inpedance Output Operation



(2) Negative Low Impedance Output Operation

④ Connecting to various type logic IC products



V_{TH} temperature compensation is considered in the above circuit

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