Signetics

54LS138, 54S138
Decoders/Demultiplexers

1-of-8 Decoder/Demultiplexer

Product Specification

Military Logic Products

FEATURES

- **Demultiplexing capability**
- **Multiple input enable for easy expansion**
- **Ideal for memory chip select decoding**
- **Direct replacement for Intel S205**

DESCRIPTION

The '138 decoder accepts three binary weighted inputs (A_0, A_1, A_2) and when enabled, provides eight mutually exclusive, active Low outputs ($\overline{0}$ - $\overline{7}$). The device features three Enable inputs: two active Low ($\overline{E}_1$, $\overline{E}_2$) and one active High (E_3). Every output will be High unless $\overline{E}_1$ and $\overline{E}_2$ are Low and E_3 is High. This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four '138s and one inverter.

The device can be used as an eight output demultiplexer by using one of the active Low Enable inputs as the Data input and the remaining Enable inputs as strobes. Enable inputs not used must be permanently tied to their appropriate active High or active Low state.

ORDERING INFORMATION

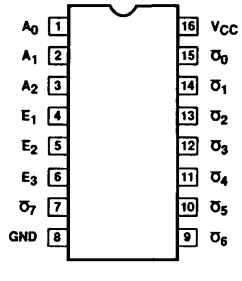
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54LS138/BEA, 54S138/BEA
16-Pin Ceramic FlatPack	54LS138/BFA, 54S138/BFA
16-Pin Ceramic LLCC	54LS138/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S	54LS
All	Inputs	1SUL	1LSUL
All	Outputs	10SUL	10LSUL

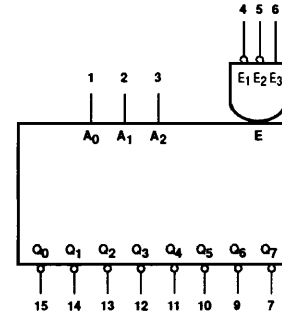
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}, and 54LS Unit Load (LSUL) is 20μA I_{IH} and -0.4mA I_{IL}.

PIN CONFIGURATION



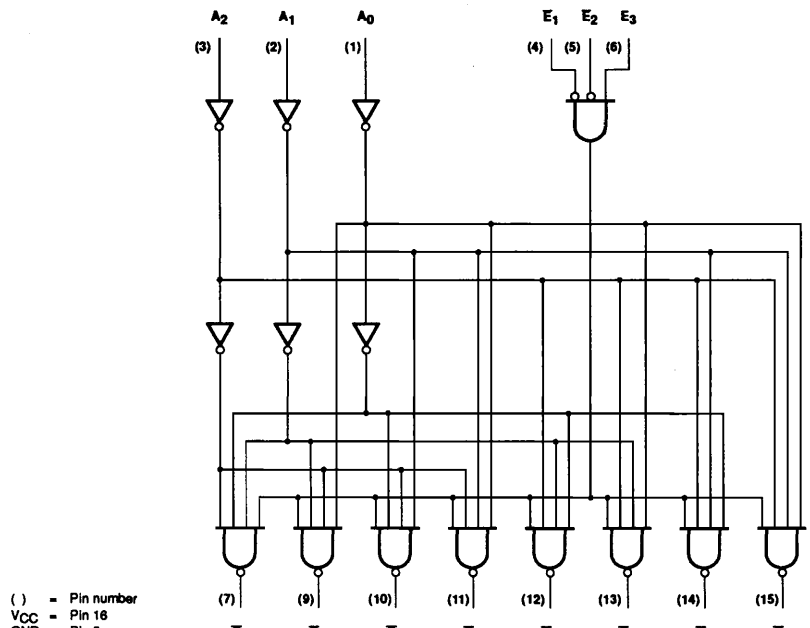
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM



For LLCC pin assignments, see JEDEC Standard No. 2.

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	54LS	54S	UNIT
V_{CC}	Supply voltage	7.0	7.0	V
V_I	Input voltage range	-0.5 to +7.0	-0.5 to +7.0	V
I_I	Input current range	-30 to +1	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150		°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	54LS			54S			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			2.0			V
V_{IL}	Low-level input voltage			+0.7			+0.8	V
I_{IK}	Input clamp current			-18			-18	mA
I_{OH}	High-level output current			-400			-1000	µA
I_{OL}	Low-level output current			4			20	mA
T_A	Operating free-air temperature range	-55		+125	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		54LS138			54S138			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OL} = Max			0.25	0.4			0.5	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.5			-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max	V_I = 5.5V						1.0	mA
			V_I = 7.0V			0.1				mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V				20			50	µA
I_{IL}	Low-level input current	V_{CC} = Max	V_I = 0.4V			-0.4				mA
			V_I = 0.5V						-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-20		-100	-40		-110	mA
I_{CC}	Supply current[4] (total)	V_{CC} = Max			6.3	10		49	74	mA

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

SYMBOL	PARAMETER	TEST CONDITIONS	54LS[5]		54S		UNIT
			C_L = 15pF		C_L = 15pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		20 41		7 10.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		27 39		12 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		18 32		8 11	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1 3 logic levels		26 38		11 11	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

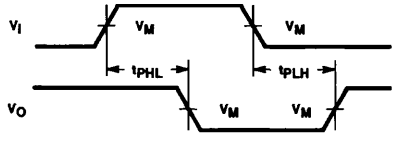
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S[5]		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		25 46		9.5 13.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		32 44		14.5 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		23 37		10.5 13.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1 3 logic levels		31 43		13.5 13.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

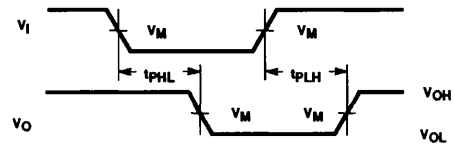
SYMBOL	PARAMETER	TEST CONDITIONS	54LS		54S		UNIT
			C_L = 50pF		C_L = 50pF		
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 2 2 logic levels		32 59		12.5 17	ns ns
t_{PLH} t_{PHL}	Propagation delay Address to output	Waveform 1 3 logic levels		41 57		19 19	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 2 2 logic levels		30 48		13.5 17.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1 3 logic levels		40 56		17.5 17.5	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. To measure I_{CC}, outputs must be enabled and open.
5. These parameters are guaranteed, but not tested.

AC WAVEFORMS



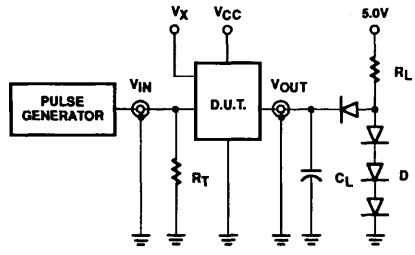
Waveform 1. Waveform for Inverting Outputs



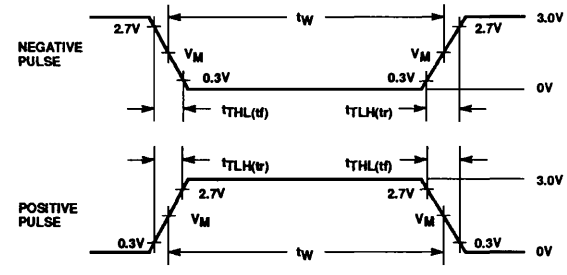
Waveform 2. Waveform for Non-Inverting Outputs

NOTE: V_M = 1.3V for 54LS, V_M = 1.5V for all other TTL families.

TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54LSXXX	2.0kΩ	1.3V	1MHz	500ns	≤15ns	≤6ns
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.