MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Order this document
by MCM218165BV/D

1M x 16

MCM218165BV
EDO
1024 Cycle Refresh

Advance Information

16M CMOS Wide DRAM Family

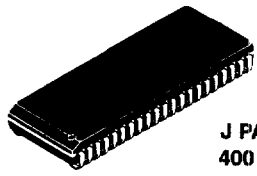
EDO, 1M x 16, and 1K Refresh

The family of 16M Dynamic RAMs is fabricated using 0.4μ CMOS high–speed silicon–gate process technology. It includes devices organized as 1,048,576 sixteen–bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

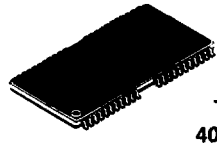
The MCM218165BV is designed to operate from a single 3.3 V only power supply.

These devices are packaged in a standard 400 mil J–lead small outline package (SOJ) and a standard 400 mil thin–small–outline package (TSOP II).

- Single 3.3 V ± 0.3 V Power Supply
- Extended Data Out (EDO) Page Mode Access
- LVTTL–Compatible Inputs and Outputs (V_{CC} = 3.3 V)
- 2 $\overline{CAS}$ Byte Control
- $\overline{RAS}$–Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 1024 Cycle Refresh: 16 ms
- Fast Access Time (t_{RAC}):
  MCM218165BV–60 = 60 ns (Max)
  MCM218165BV–70 = 70 ns (Max)
- Low Active Power Dissipation: 990/935 mW (Max)
- Low Standby Power Dissipation: 1.8 mW (Max)



J PACKAGE
400 MIL SOJ
CASE 986B–01



T PACKAGE
400 MIL TSOP II
CASE 985A–01

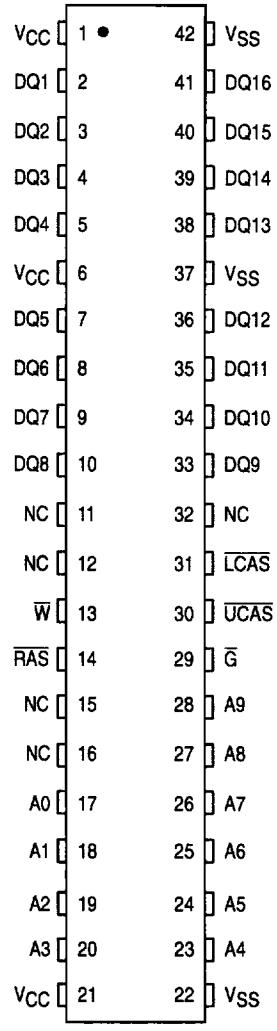
PIN NAMES	
A0 – A9 ..... Address Input	$\overline{UCAS}$, $\overline{LCAS}$ .. Column Address Strobe
DQ1 – DQ16 ..... Data Input/Output	V_{CC} ..... Power Supply (+ 3.3 V)
$\overline{G}$ ..... Output Enable	V_{SS} ..... Ground
$\overline{W}$ ..... Read/Write Enable	NC ..... No Connection
$\overline{RAS}$ ..... Row Address Strobe	

This document contains information on a new product. Specifications and information herein are subject to change without notice.

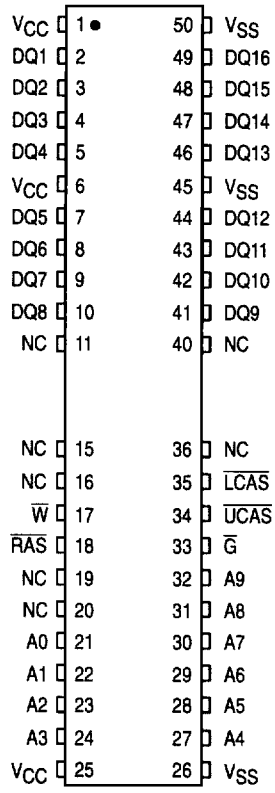
12/19/96

PIN ASSIGNMENTS

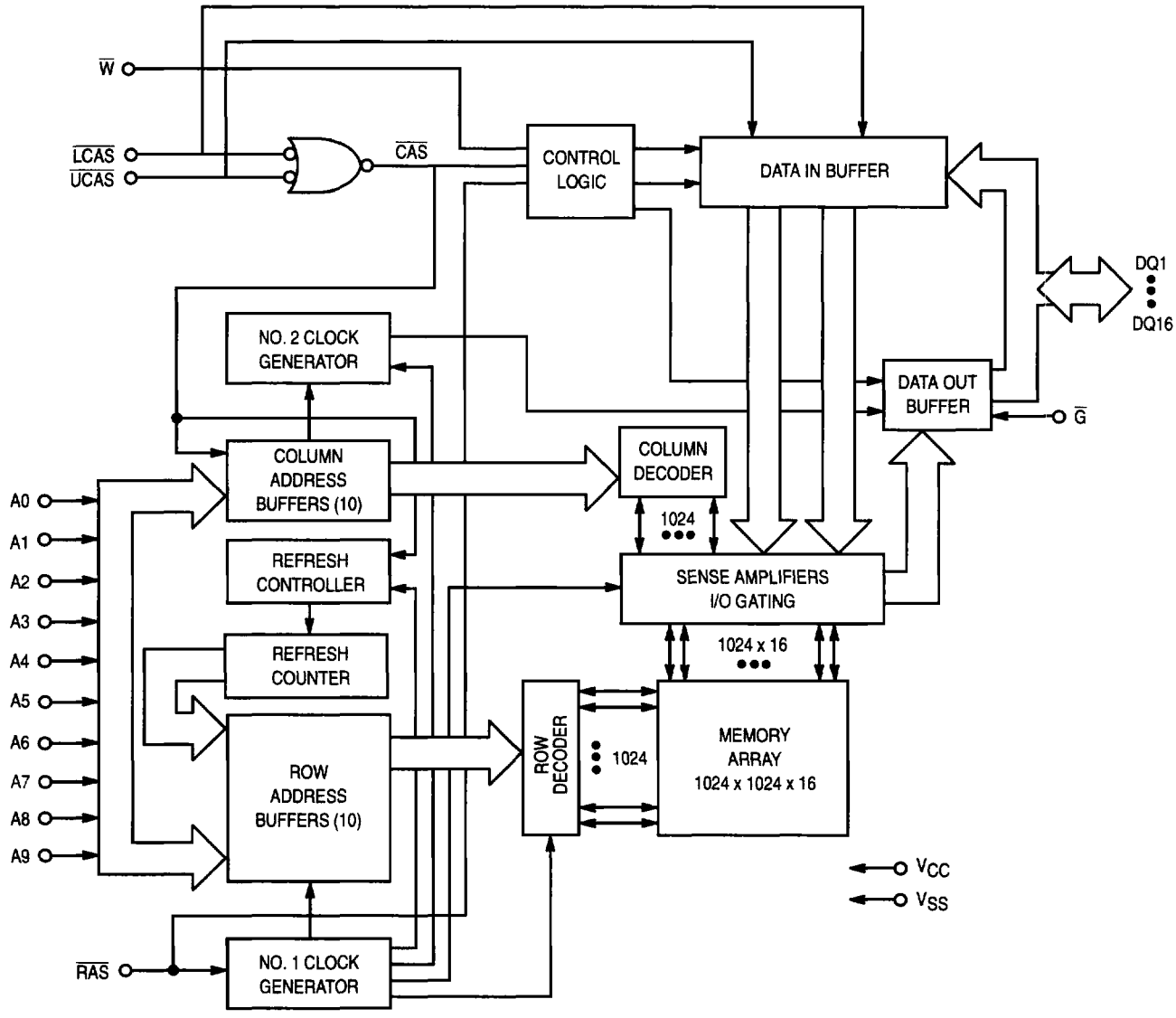
400 MIL SOJ



400 MIL TSOP II



BLOCK DIAGRAM



TRUTH TABLE

Function		$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{W}$	$\overline{G}$	Addresses		DQx	Notes
							Row	Column		
Standby		H	H→X	H→X	X	X	X	X	High–Z	
Read: Word		L	L	L	H	L	Row	Column	Data Out	
Read: Lower Byte		L	L	H	H	L	Row	Column	Lower Byte: Data Out Upper Byte: High–Z	
Read: Upper Byte		L	H	L	H	L	Row	Column	Lower Byte: High–Z Upper Byte: Data Out	
Write: Word (Early Write)		L	L	L	L	X	Row	Column	Data In	
Write: Lower Byte (Early)		L	L	H	L	X	Row	Column	Lower Byte: Data In Upper Byte High–Z	
Write: Upper Byte (Early)		L	H	L	L	X	Row	Column	Lower Byte: High–Z Upper Byte: Data In	
Read–Write		L	L	L	H→L	L→H	Row	Column	Data Out, Data In	1, 2
EDO Page Mode Read	1st Cycle	L	H→L	H→L	H	L	Row	Column	Data Out	2
	2nd Cycle	L	H→L	H→L	H	L	N/A	Column	Data Out	2
EDO Page Mode Write	1st Cycle	L	H→L	H→L	L	X	Row	Column	Data In	1
	2nd Cycle	L	H→L	H→L	L	X	N/A	Column	Data In	1
EDO Page Mode Read Write	1st Cycle	L	H→L	H→L	H→L	L→H	Row	Column	Data Out, Data In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	N/A	Column	Data Out, Data In	1, 2
Hidden Refresh	Read	L→H→L	L	L	H	L	Row	Column	Data Out	2
	Write	L→H→L	L	L	L	X	Row	Column	Data In	1, 3
$\overline{RAS}$–Only Refresh		L	H	H	X	X	Row	N/A	High–Z	
$\overline{CAS}$ Before $\overline{RAS}$ Refesh		H→L	L	L	X	X	X	X	High–Z	4

NOTES:
1. These write cycles may also be byte write cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).
2. These read cycles may also be byte read cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).
3. Early write only.
4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{LCAS}$ or $\overline{UCAS}$).

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Power Supply Voltage	3.3 V	V_{CC}	– 0.5 to 4.6	V
Voltage Relative to V_{SS}	3.3 V	V_{in}, V_{out}	– 0.5 to 4.6	V
Data Out Current		I_{out}	50	mA
Power Dissipation		P_D	1.0	W
Operating Temperature Range		T_A	0 to + 70	°C
Storage Temperature Range		T_{stg}	– 55 to + 125	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high–impedance circuit.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All Voltages Referenced to V_{SS})

Parameter		Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	5 V	V_{CC}	3.0	3.3	3.6	V
Logic High Voltage, All Inputs	5 V	V_{IH}	2.0	—	V_{CC} + 0.3	V
Logic Low Voltage, All Inputs	5 V	V_{IL}	– 0.3	—	0.8	V

DC CHARACTERISTICS AND SUPPLY CURRENTS (All Voltages Referenced to V_{SS})

Characteristic	Symbol	MCM218165BV–60		MCM218165BV–70		Unit	Notes
		Min	Max	Min	Max		
Power Supply Current ($\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ Cycling, t_{RC} = min)	I_{CC1}	—	180	—	170	mA	1, 2
Power Supply Current (Standby) (TTL Interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH}, Data Out = High–Z)n	I_{CC2}	—	2	—	2	mA	
(CMOS Interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} – 0.2 V, Data Out = High–Z)n		—	0.5	—	0.5		
Power Supply Current During $\overline{RAS}$–Only Refresh Cycles ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}, t_{RC} = Min)	I_{CC3}	—	180	—	170	mA	2
Power Supply Current During EDO Page Mode Cycle (t_{PC} = Min)	I_{CC4}	—	100	—	90	mA	1, 3
Power Supply Current During $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle (t_{RC} = Min, $\overline{RAS}$, $\overline{CAS}$ Cycling)	I_{CC5}	—	180	—	170	mA	
Input Leakage Current (0 V ≤ V_{in} ≤ V_{CC})	$I_{lkg(I)}$	– 5	5	– 5	5	µA	
Output Leakage Current (0 V ≤ V_{out} ≤ V_{CC}, Data Out = Disable)	$I_{lkg(O)}$	– 5	5	– 5	5	µA	
Output High Voltage (I_{OH} = – 5 mA)	V_{OH}	2.4	—	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)	V_{OL}	—	0.4	—	0.4	V	

NOTES:
1. I_{CC} depends on the output load condition when the device is selected. I_{CC} max is specified at the ouput open condition.
2. Address may be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address may be changed once or less while $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IL}.
4. All V_{CC} and V_{SS} pins will be supplied with the same voltage.

CAPACITANCE (f = 1.0 MHz, T_A = 25°C, V_{CC} = 3.3 V ± 0.3 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit	Notes
Input Capacitance	A0 – A9	C_{in}	5	pF	1
	$\overline{G}$, $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{W}$		7		
Input/Output Capacitance	DQ1 – DQ16	$C_{I/O}$	7	pF	1, 2

NOTES:
1. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.
2. $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH} to disable data out.

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 3.3 V ± 0.3 V, T_A = 0 to 70°C, Unless Otherwise Noted)

Input Timing Reference Level ..... VIH = 2.0 V, VIL = 0.8 V
Input Pulse Levels ..... 0 to 3.0 V
Input Rise/Fall Time ..... 2 ns

Output Timing Reference Level ..... VOL = 0.8 V, VOH = 2.0 V
Output Load ..... One TTL Load and 100 pF

ALL DEVICES: READ, WRITE, READ–MODIFY–WRITE, AND REFRESH CYCLES (See Notes 1, 2, 3, 4, and 5)

Parameter	Symbol		MCM218165BV–60		MCM218165BV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	110	—	130	—	ns	
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	60	10 k	70	10 k	ns	6
$\overline{LCAS}/\overline{UCAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	10	10 k	12	10 k	ns	7
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	ns	8
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	15	—	ns	
$\overline{RAS}$ to $\overline{LCAS}/\overline{UCAS}$ Delay Time	t_{RELCEL}	t_{RCD}	20	42	20	50	ns	9
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	15	30	15	35	ns	10
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	15	—	18	—	ns	
$\overline{LCAS}/\overline{UCAS}$ Hold Time	t_{RELCEH}	t_{CSH}	60	—	70	—	ns	
$\overline{LCAS}/\overline{UCAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	ns	11
$\overline{G}$ to Data In Delay Time	t_{GLHDX}	t_{GD}	15	—	18	—	ns	
Transition Time (Rise and Fall)	t_T	t_T	1	50	1	50	ns	
Refresh Period	t_{RVRV}	t_{REF}	—	16	—	16	ms	12
$\overline{CAS}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	60	—	70	ns	13
Access Time from $\overline{LCAS}/\overline{UCAS}$	t_{CELQV}	t_{CAC}	—	18	—	20	ns	14, 15
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	ns	15, 16
Access Time from $\overline{G}$	t_{GLQV}	t_{GA}	—	15	—	18	ns	

NOTES: (continued)

1. AC measurements assume t_T = 2.0 ns.
2. An initial pause of 100 µs is required after power–up, followed by a minimum of initialization cycles ($\overline{RAS}$–only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$ before $\overline{RAS}$ refresh cycles are required.
3. In delayed write or read–modify–write cycles, $\overline{G}$ must disable the output buffer prior to applying data to the device.
4. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16 bits of data are written into the device. $\overline{LCAS}$ and $\overline{UCAS}$ can not be staggered within the same write/read cycles.
5. All V_{CC} and V_{SS} pins will be supplied with the same voltages.
6. t_{RAS} (min) = t_{RWD} (min) + t_{RWL} (min) + t_T in read–modify–write cycle.
7. t_{CAS} (min) = t_{CWD} (min) + t_{CWL} (min) + t_T in read–modify–write cycle.
8. t_{ASC} (min), t_{RCS} (min), t_{WCS} (min), and t_{RPC} are determined by the earlier falling edge of $\overline{LCAS}$ or $\overline{UCAS}$.
9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
10. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.
11. t_{CRP}, t_{CHR}, t_{RCH}, t_{CPA}, and t_{CPW} are determined by the latter rising edge of $\overline{LCAS}$ or $\overline{UCAS}$.
12. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing or input signals. Transition times are measured between V_{IH} and V_{IL}.
13. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
14. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max).
15. Access time is determined by the longer of t_{AA}, t_{CAC}, t_{CPA}.
16. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).

ALL DEVICES: READ, WRITE, READ–MODIFY–WRITE, AND REFRESH CYCLES (continued)

Parameter	Symbol		MCM218165BV–60		MCM218165BV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	ns	8
Read Command Hold Time to $\overline{LCAS}/\overline{UCAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	ns	11, 17
Read Command Hold Time to $\overline{RAS}$	t_{REHWX}	t_{RRH}	10	—	10	—	ns	17
Output Buffer Turn–Off Time	t_{CEHQZ}	t_{OFF}	0	15	0	18	ns	18
Output Buffer Turn–Off Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	15	0	18	ns	18
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	ns	8, 19
Write Command Hold Time	t_{CELWH}	t_{WCH}	10	—	10	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	10	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	15	—	18	—	ns	
Write Command to $\overline{LCAS}/\overline{UCAS}$ Lead Time	t_{WLCEH}	t_{CWL}	15	—	18	—	ns	20
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	ns	21
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	15	—	ns	21
$\overline{W}$ to Data In Delay	t_{WLDV}	t_{WD}	10	—	10	—	ns	
Read–Modify–Write Cycle Time	t_{RELREL}	t_{RWC}	133	—	157	—	ns	
$\overline{RAS}$ to $\overline{W}$ Delay Time	t_{RELWL}	t_{RWD}	77	—	89	—	ns	19
$\overline{LCAS}/\overline{UCAS}$ to $\overline{W}$ Delay Time	t_{CELWL}	t_{CWD}	32	—	37	—	ns	19
Column Address to $\overline{W}$ Delay Time	t_{AVWL}	t_{AWD}	47	—	54	—	ns	19
$\overline{G}$ Hold Time from $\overline{W}$	t_{WLGL}	t_{GH}	15	—	18	—	ns	
$\overline{LCAS}/\overline{UCAS}$ Setup Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{CELCEL}	t_{CSR}	10	—	10	—	ns	
$\overline{LCAS}/\overline{UCAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{RELCEH}	t_{CHR}	10	—	10	—	ns	11
$\overline{RAS}$ Precharge to $\overline{LCAS}/\overline{UCAS}$ Hold Time	t_{REHCEL}	t_{RPC}	5	—	5	—	ns	8
$\overline{LCAS}/\overline{UCAS}$ Precharge Time (Normal Mode)	t_{CEHCEL}	t_{CPN}	10	—	10	—	ns	22
EDO Page Mode Cycle Time	t_{RELREL}	t_{PC}	25	—	30	—	ns	
EDO Page Mode $\overline{LCAS}/\overline{UCAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	ns	22
EDO Page Mode $\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RASP}	60	100 k	70	100 k	ns	23

NOTES: (continued)

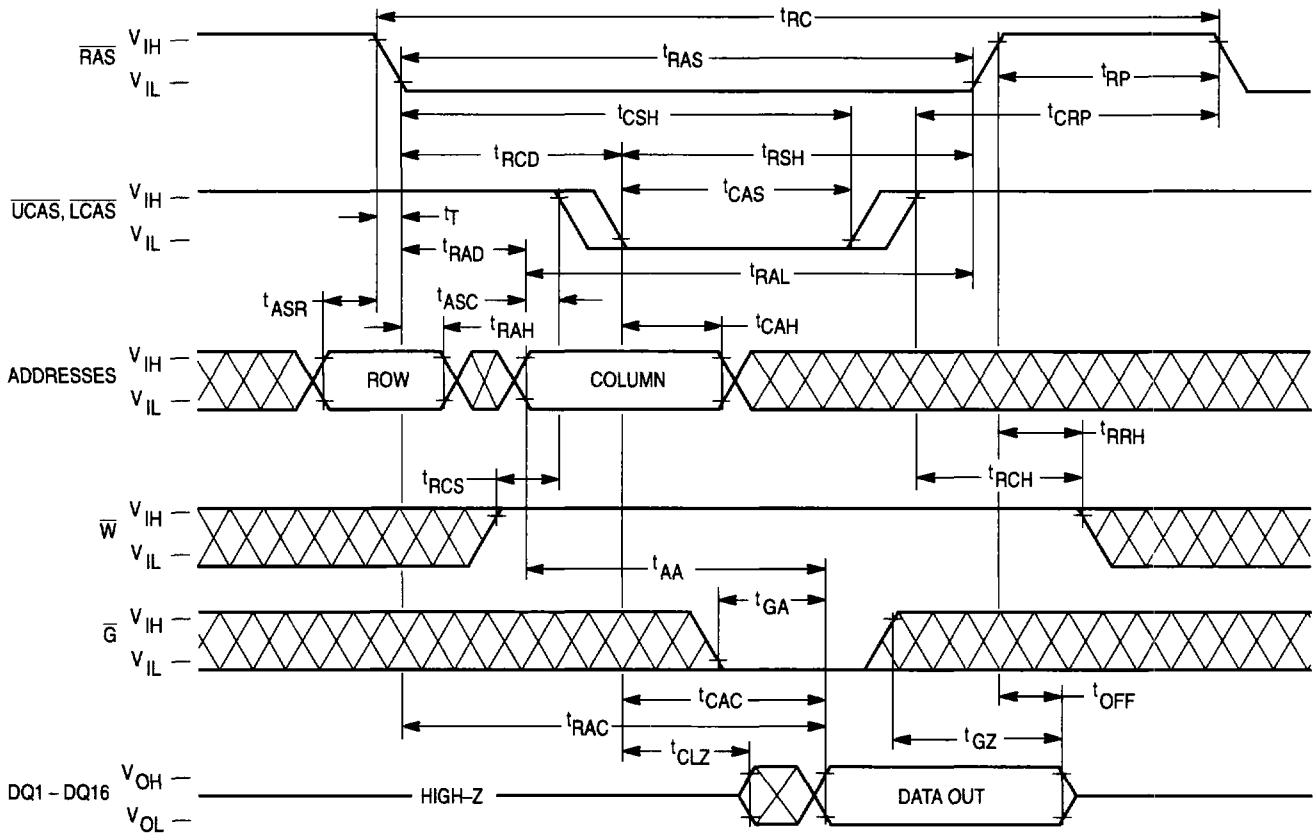
17. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
18. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. t_{OFF} is determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.
19. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read–modify–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
20. t_{CWL} shall be satisfied by both $\overline{LCAS}$ and $\overline{UCAS}$.
21. These parameters are referenced to $\overline{LCAS}$ or $\overline{UCAS}$ separately in an early write cycle and to $\overline{W}$ edge in a delayed write or read–modify–write cycle.
22. t_{CPN} and t_{CP} are determined by the time that both $\overline{LCAS}$ and $\overline{UCAS}$ are high.
23. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.

ALL DEVICES: READ, WRITE, READ–MODIFY–WRITE, AND REFRESH CYCLES (continued)

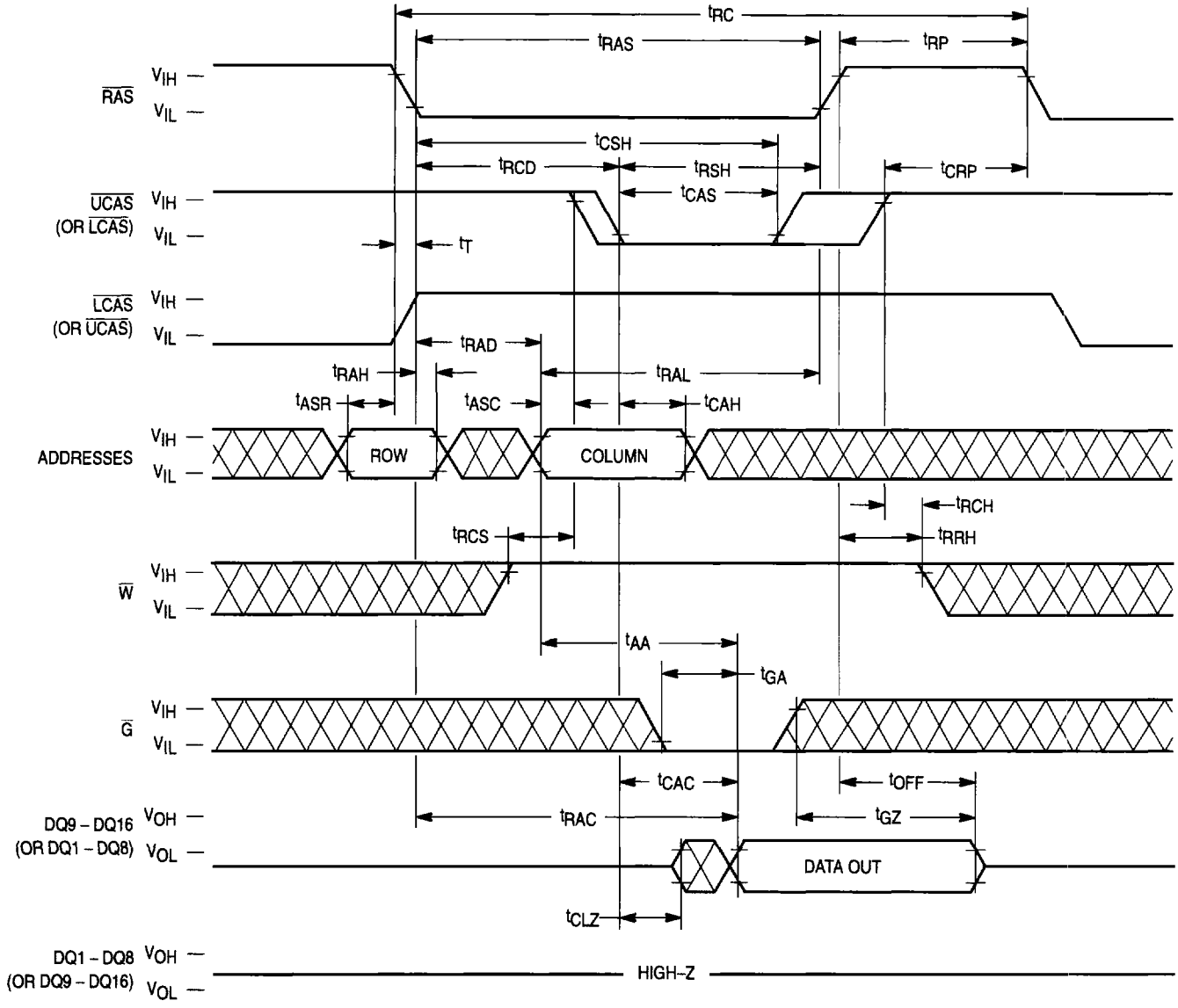
Parameter	Symbol		MCM218165BV–60		MCM218165BV–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max		
Access Time from $\overline{LCAS}$ /$\overline{UCAS}$ Precharge	t_{CEHQV}	t_{CPA}	—	35	—	40	ns	11, 15
$\overline{RAS}$ Hold Time from $\overline{LCAS}$/$\overline{UCAS}$ Precharge	t_{CEHREH}	t_{CPRH}	35	—	40	—	ns	
$\overline{G}$ High Hold Time from $\overline{CAS}$ High	t_{CEHGL}	t_{GHC}	5	—	5	—	ns	
$\overline{G}$ High Pulse Width	t_{GHGL}	t_{GP}	10	—	10	—	ns	
Data Output Hold After $\overline{CAS}$ Low	t_{CELDX}	t_{COH}	5	—	5	—	ns	
Output Disable Delay from $\overline{W}$	t_{WELDX}	t_{WHZ}	3	10	3	10	ns	
$\overline{W}$ Pulse Width for Output Disable When $\overline{CAS}$ High	t_{WLWH}	t_{WPZ}	7	—	7	—	ns	
EDO Page Mode Read–Modify–Write Cycle $\overline{LCAS}$/$\overline{UCAS}$ Precharge to $\overline{W}$ Delay Time	t_{CEHWL}	t_{CPW}	55	—	65	—	ns	11
EDO Page Mode Read–Modify–Write Cycle Time	t_{CELCEL}	t_{PRWC}	68	—	75	—	ns	

TIMING DIAGRAMS

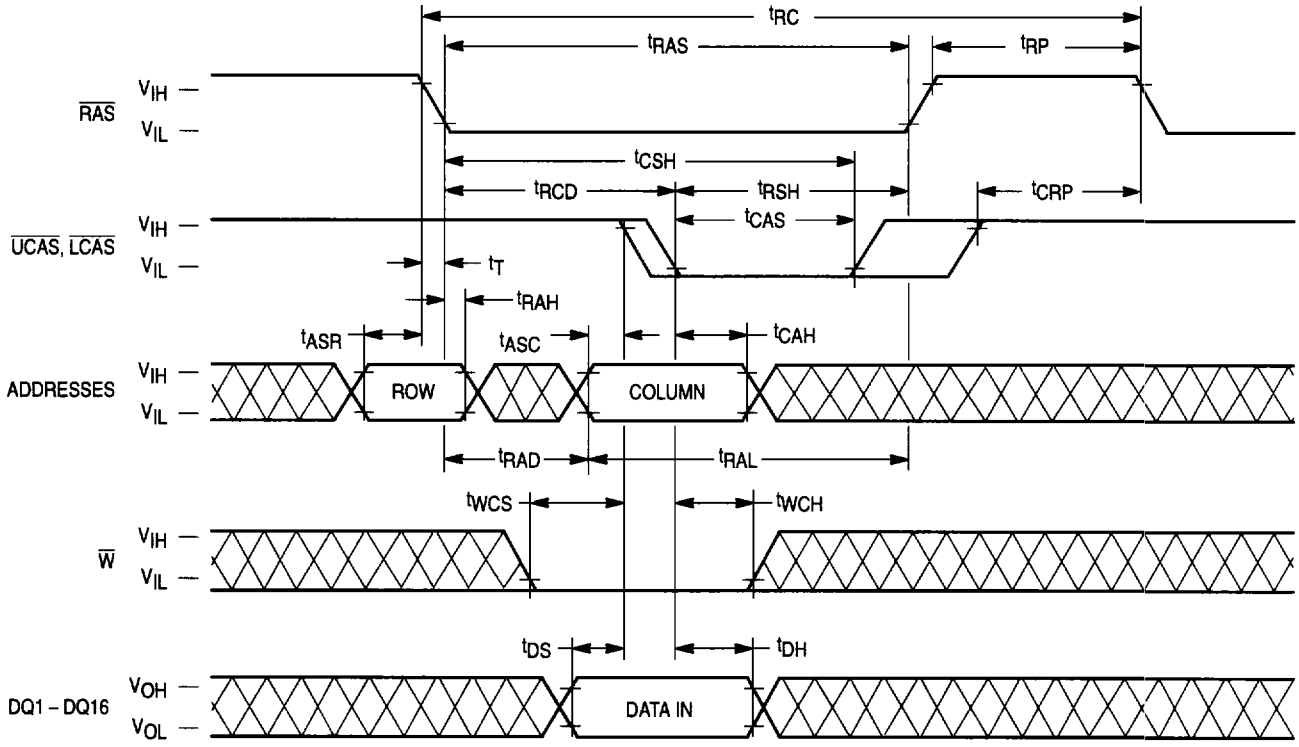
WORD READ CYCLE



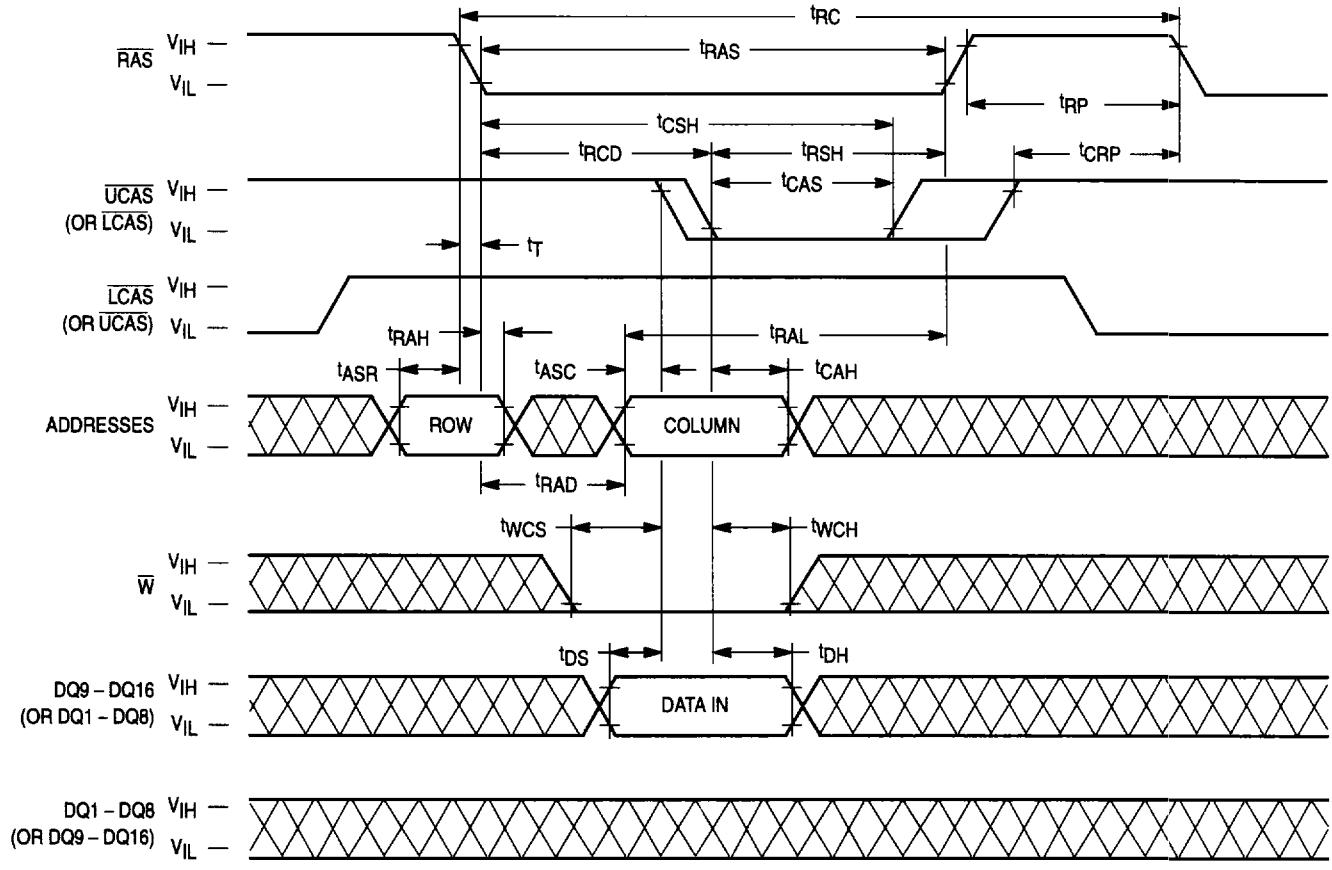
BYTE READ CYCLE



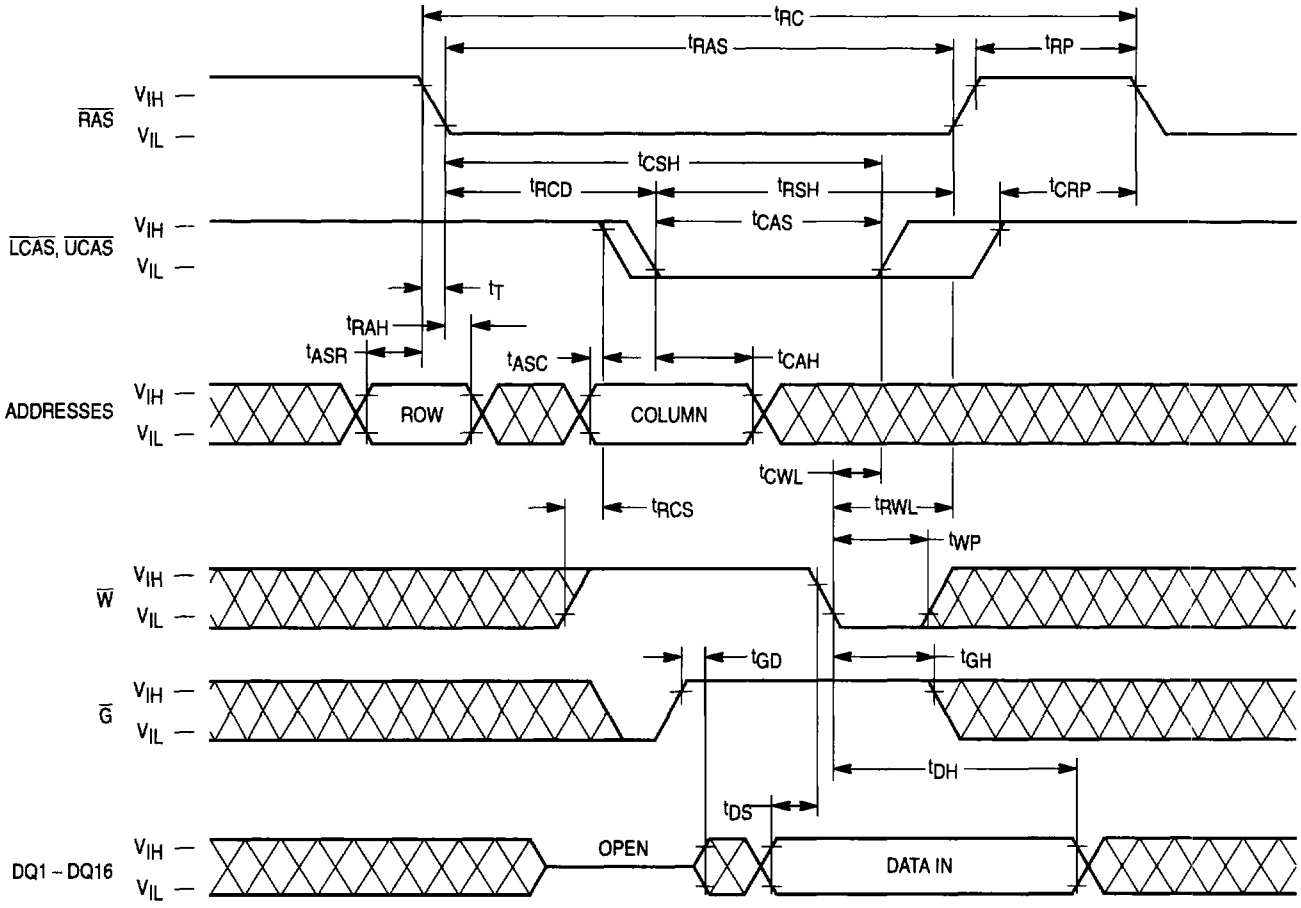
WORD EARLY WRITE CYCLE



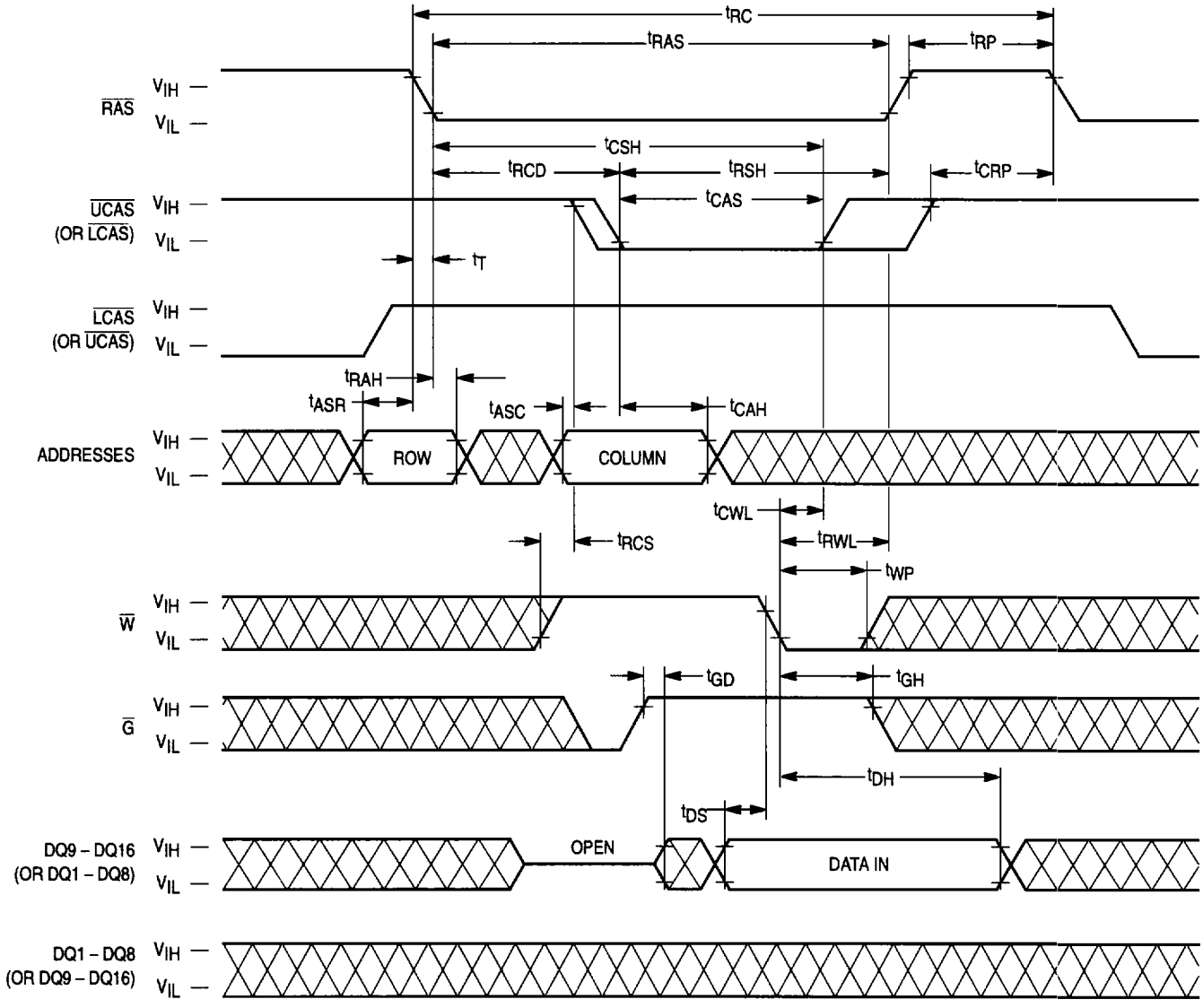
BYTE EARLY WRITE CYCLE



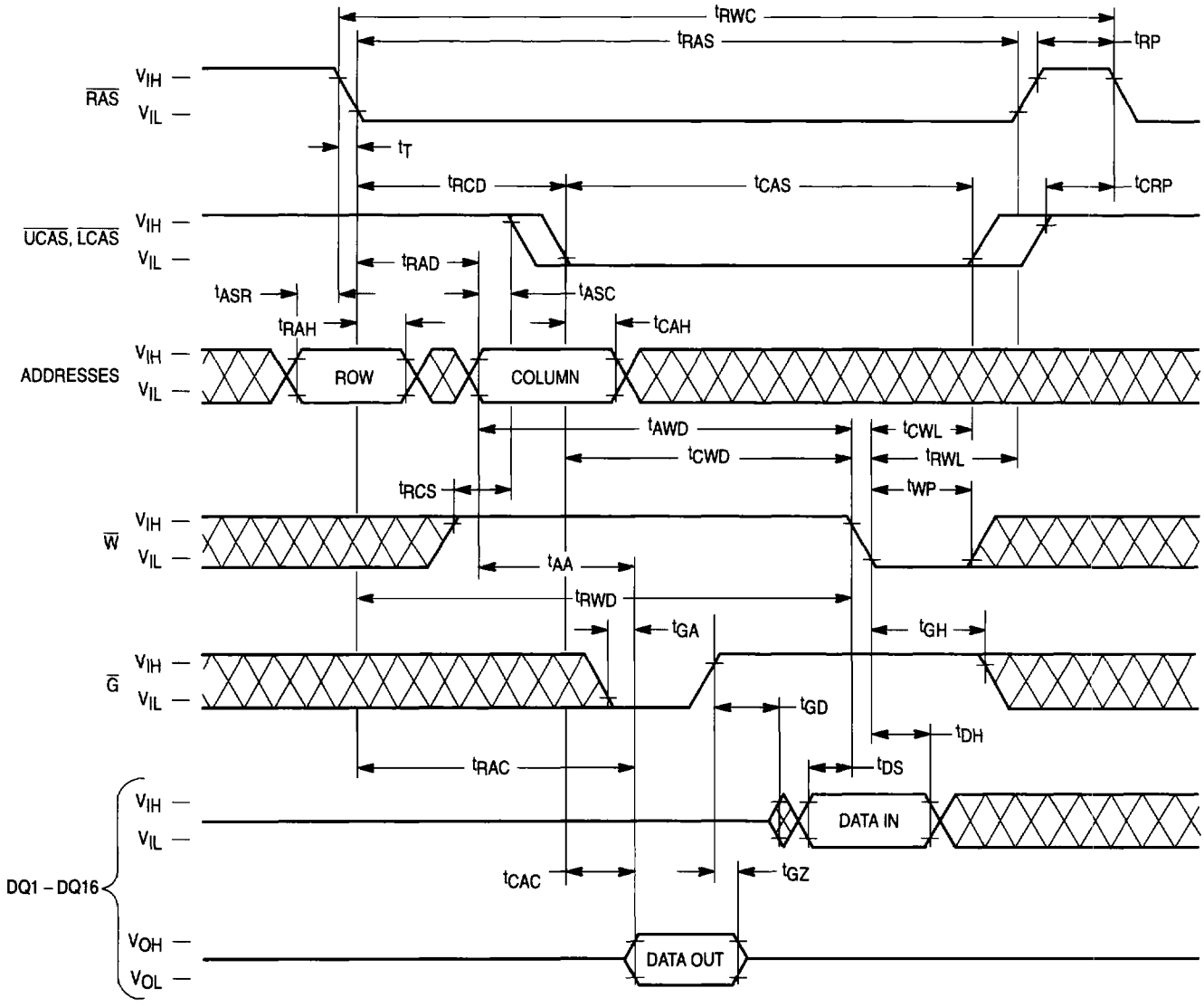
WORD DELAYED WRITE CYCLE



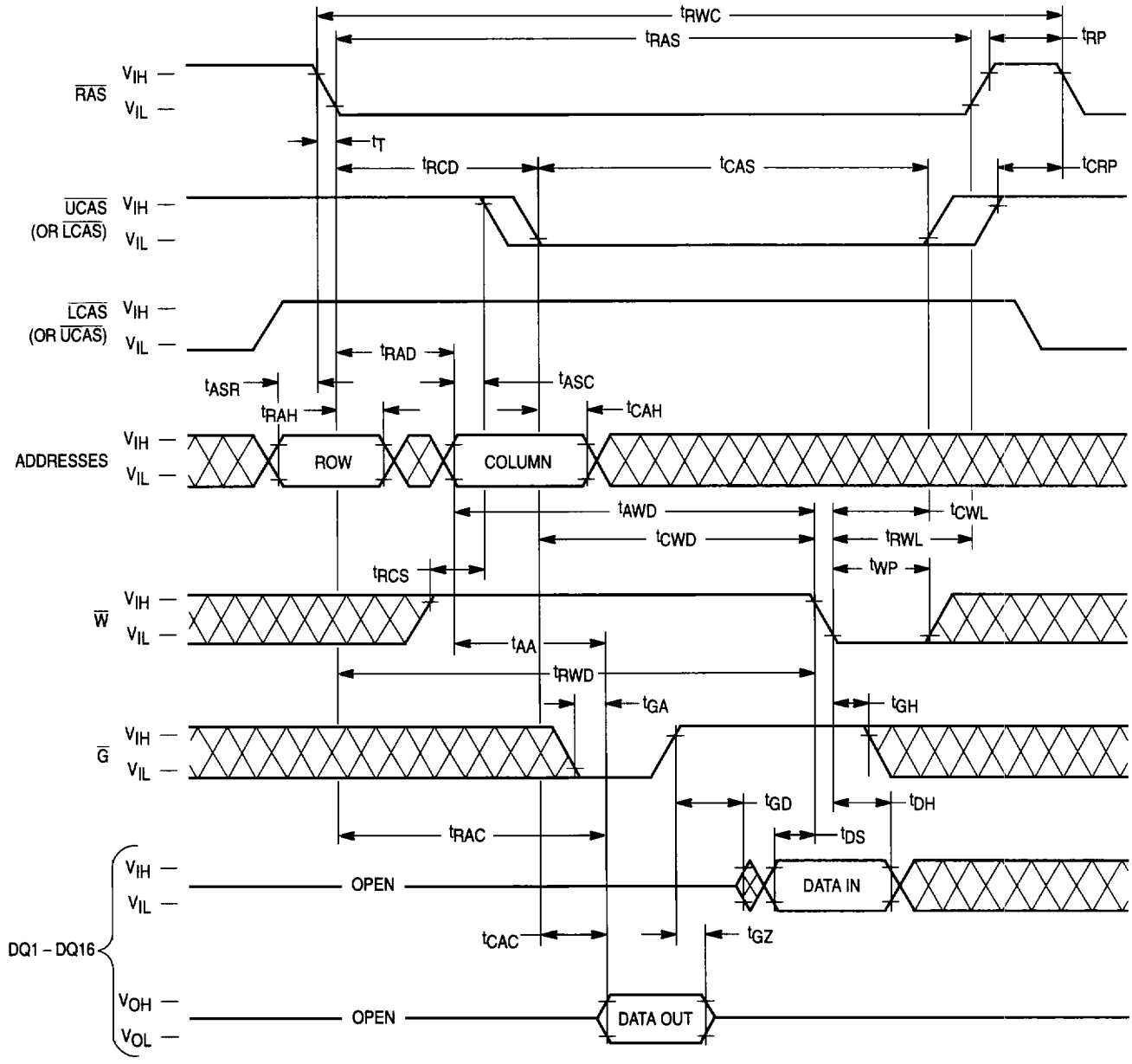
BYTE DELAYED WRITE CYCLE



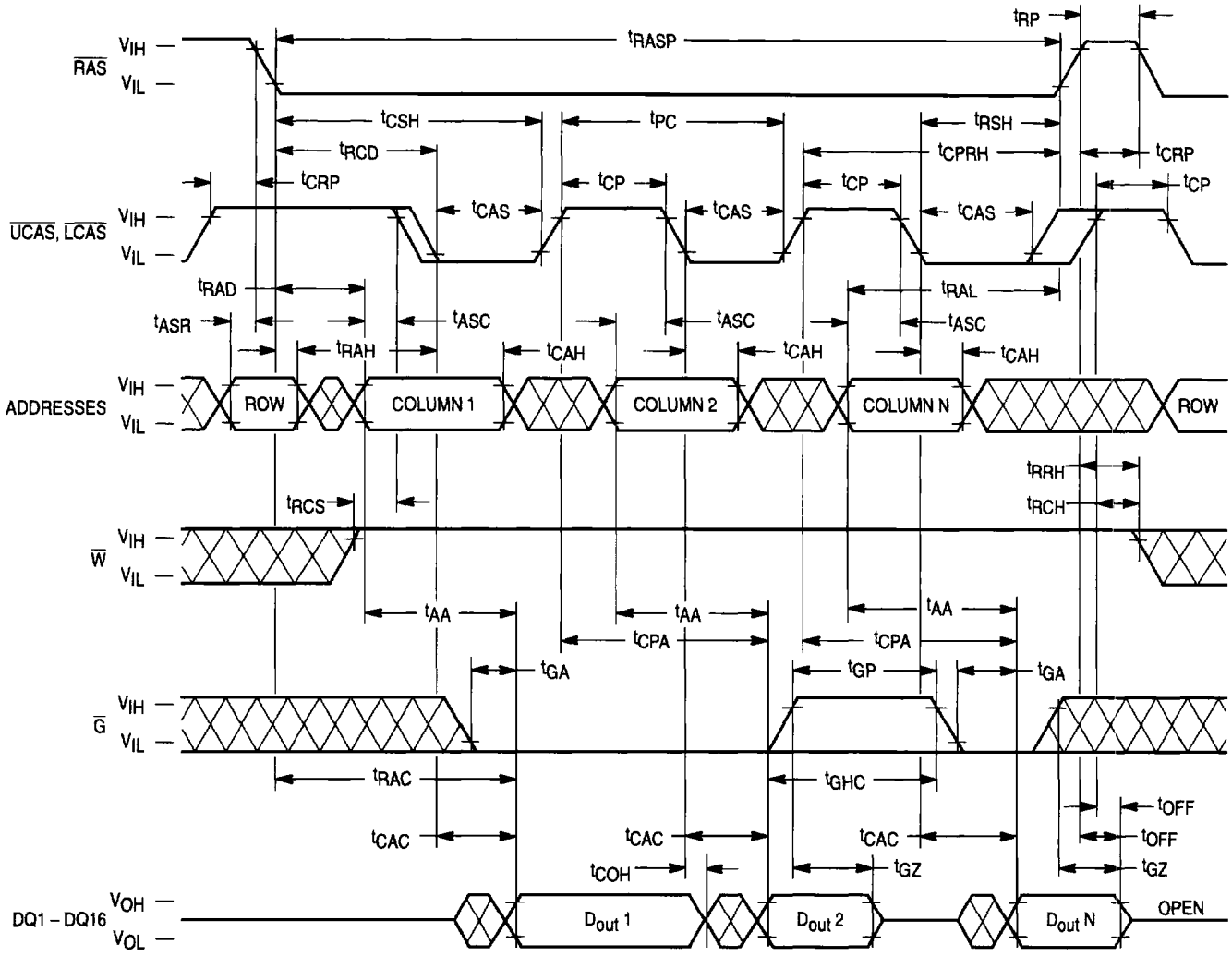
WORD READ–MODIFY–WRITE CYCLE



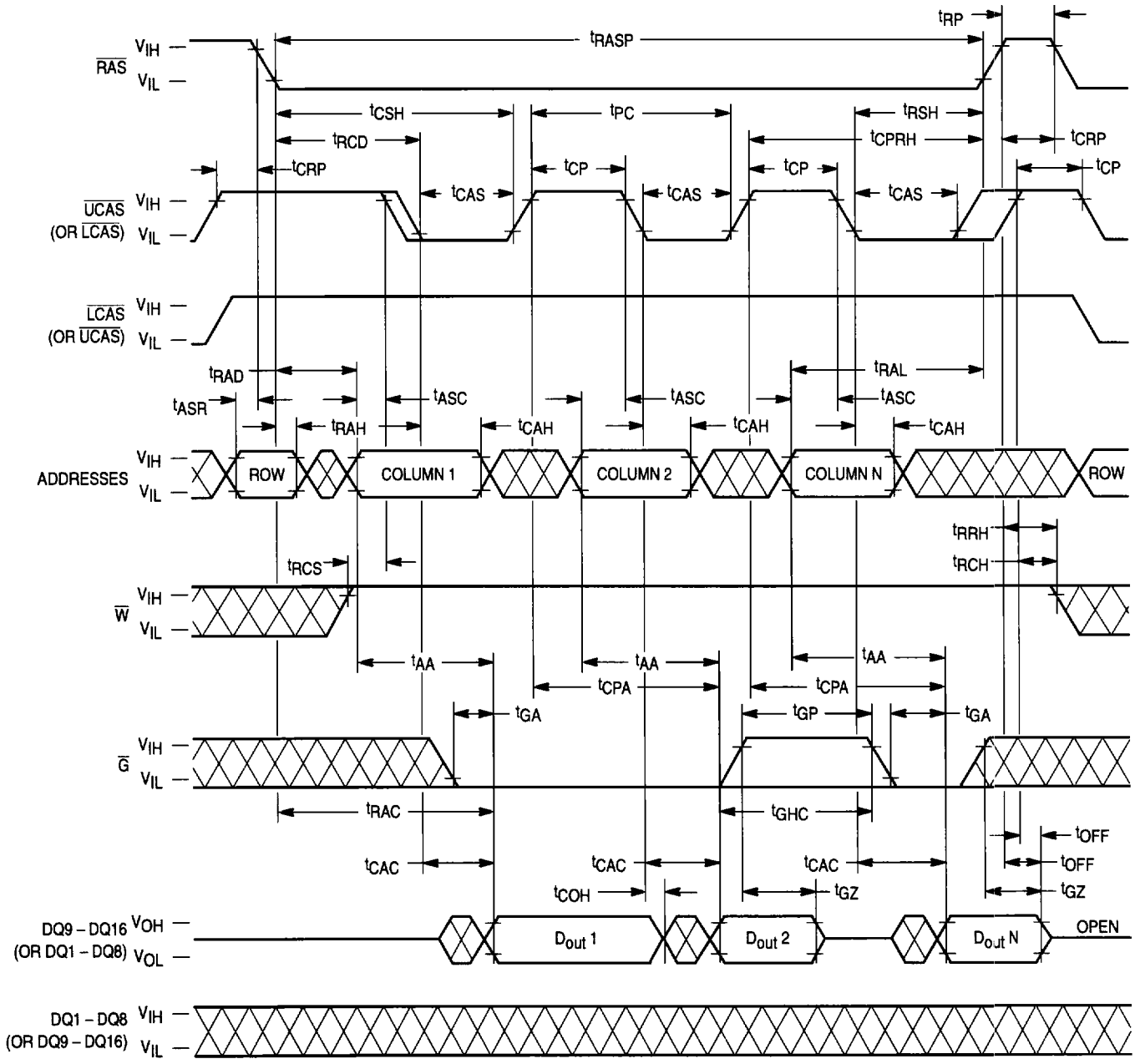
BYTE READ–MODIFY–WRITE CYCLE



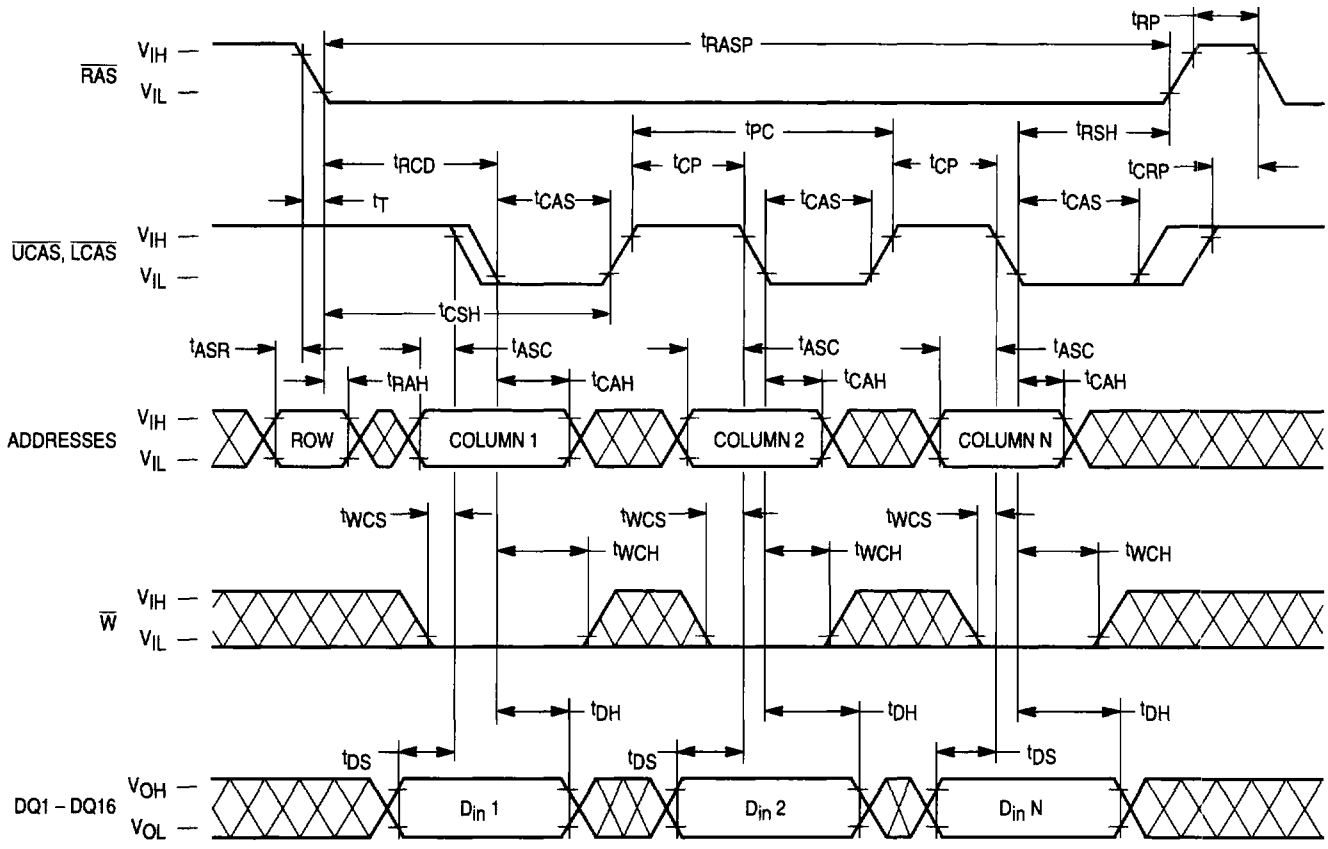
EDO PAGE MODE WORD READ CYCLE



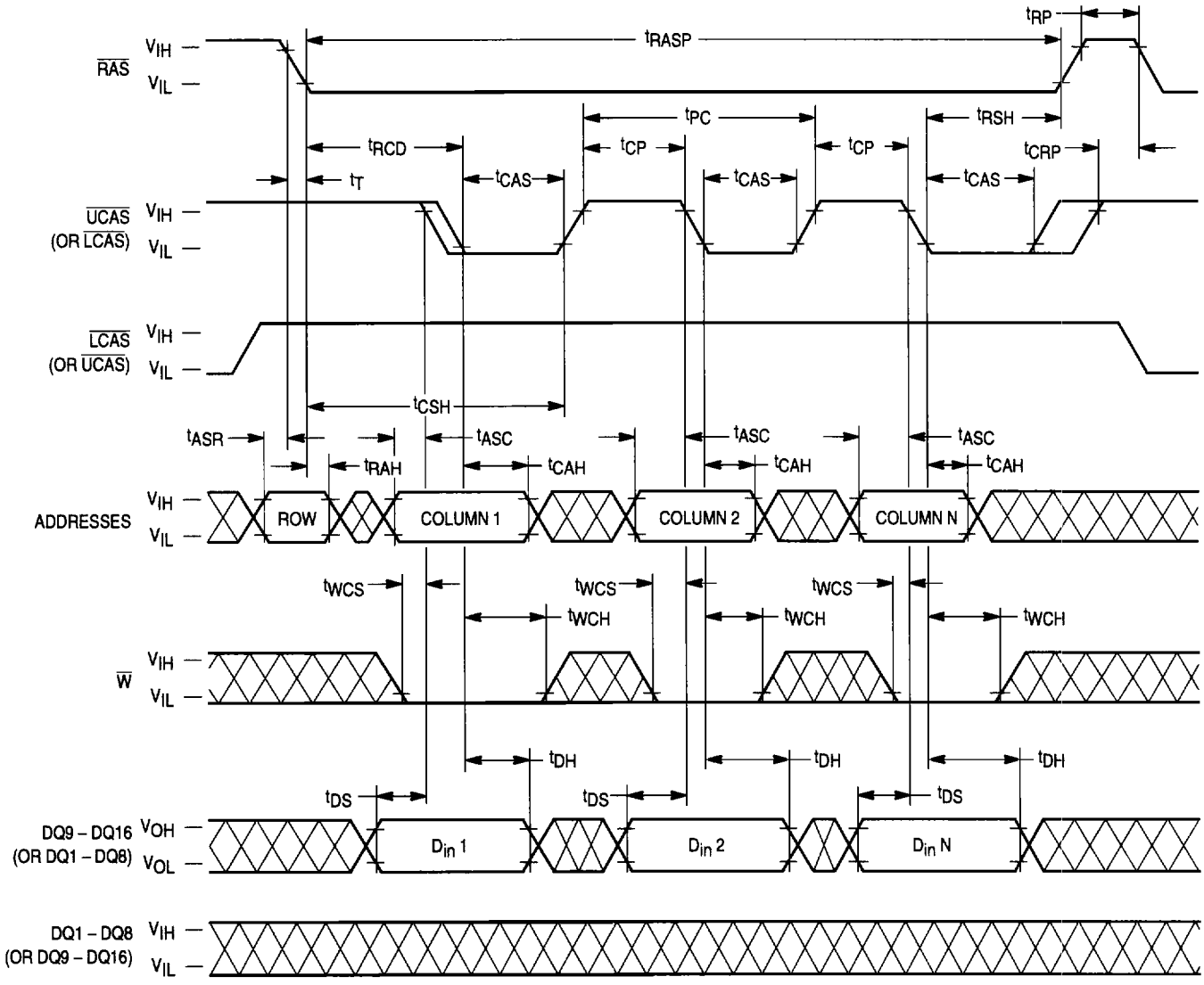
EDO PAGE MODE BYTE READ CYCLE



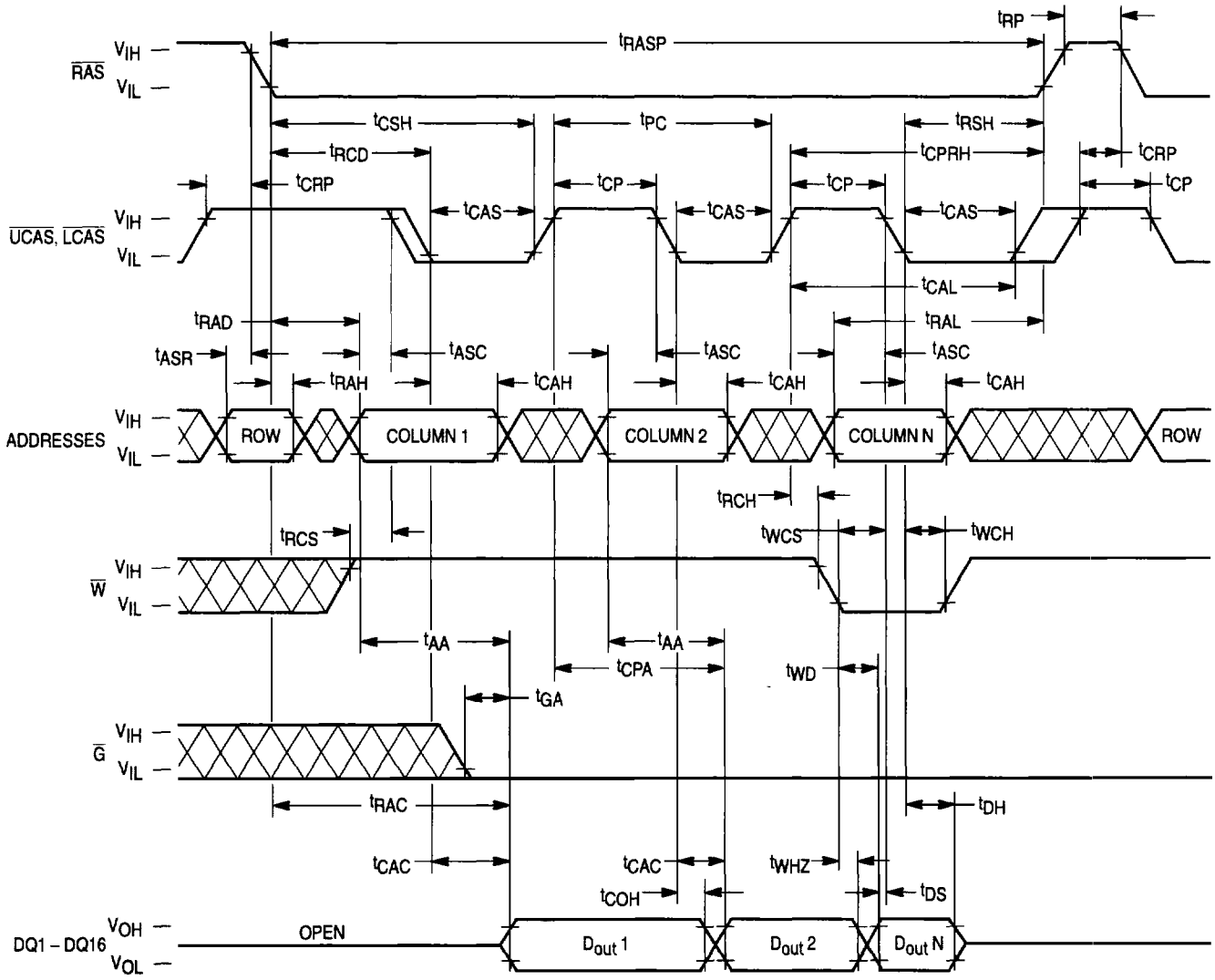
EDO PAGE MODE WORD EARLY WRITE CYCLE



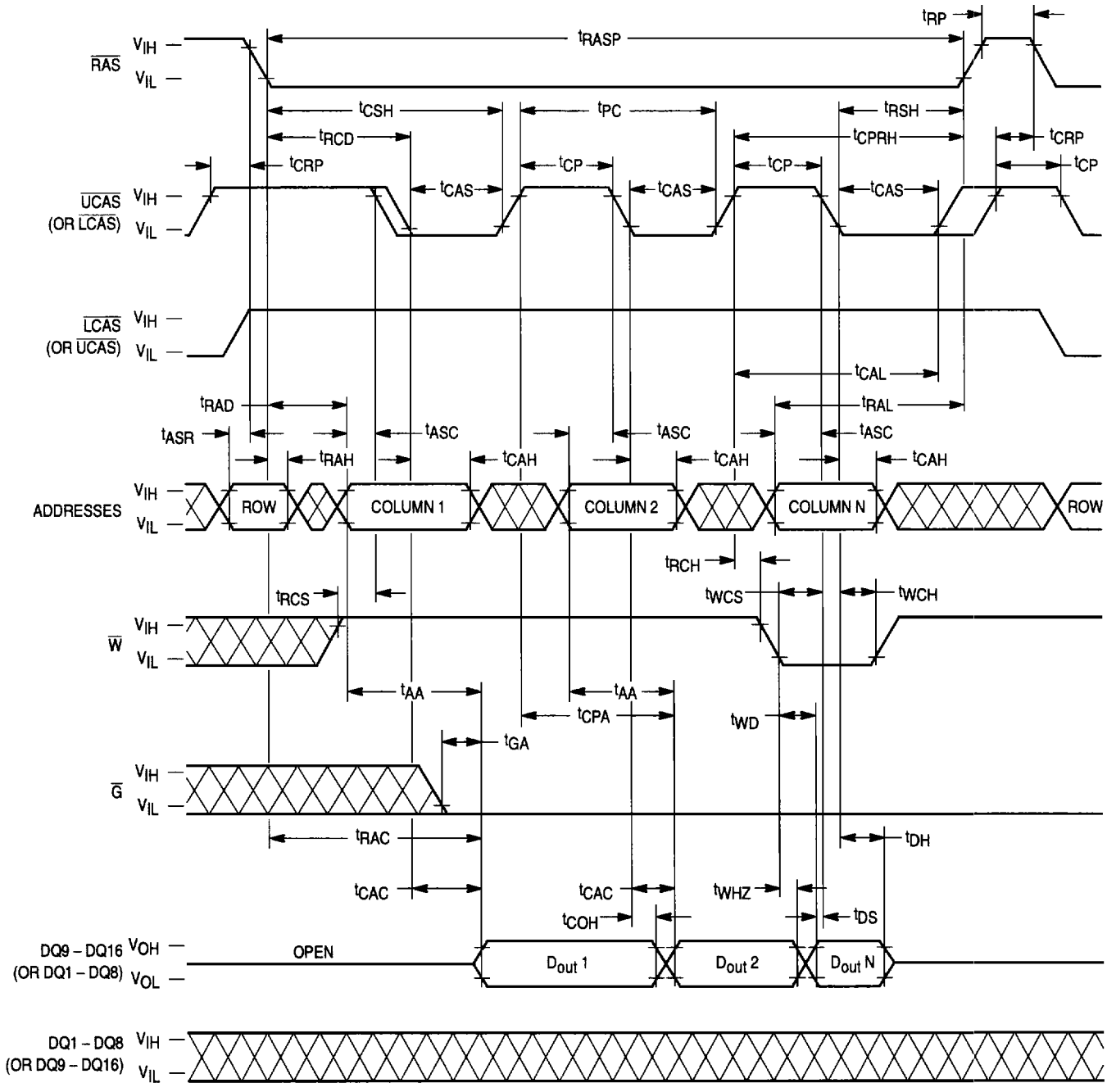
EDO PAGE MODE BYTE EARLY WRITE CYCLE



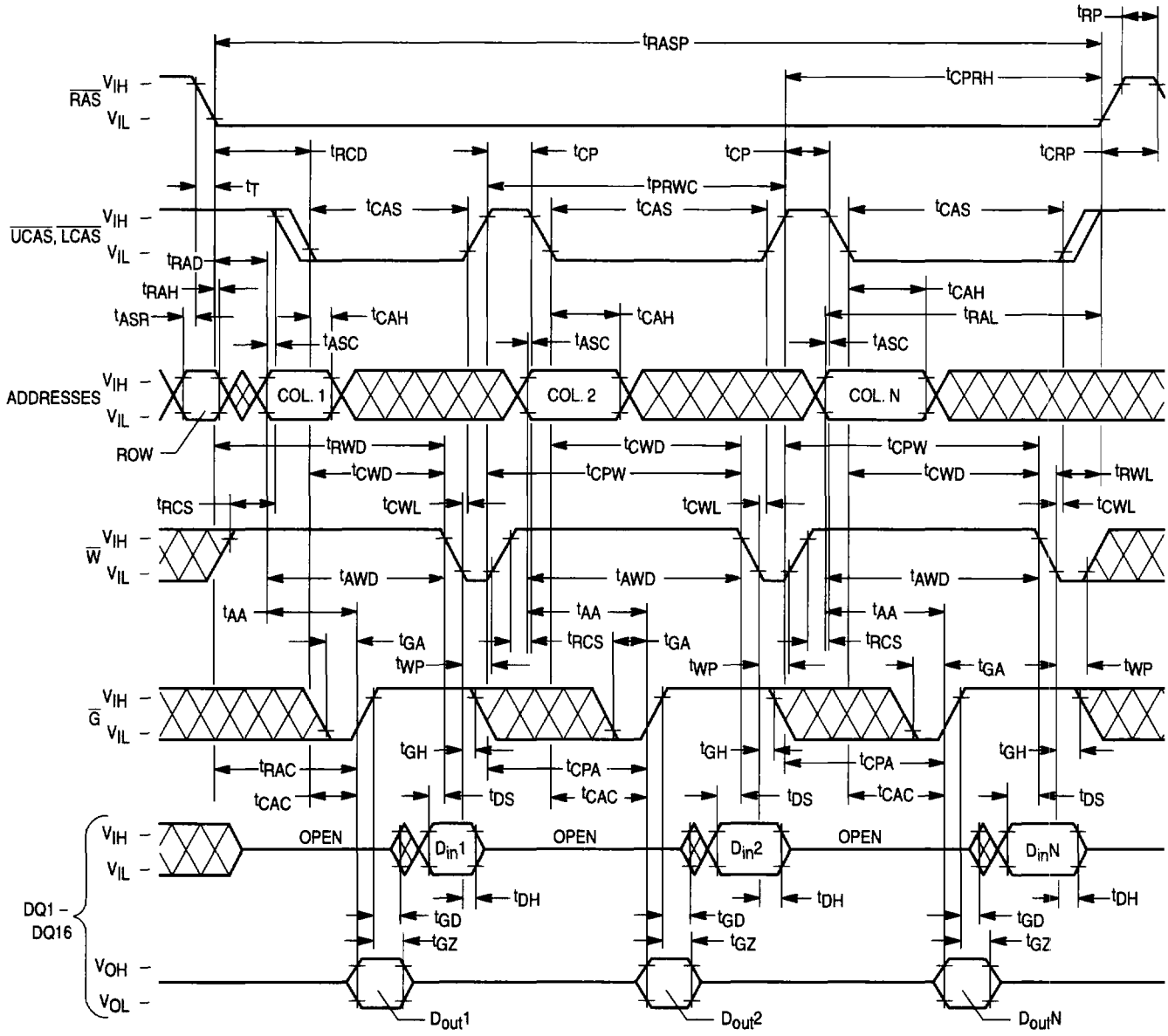
EDO PAGE MODE WORD READ–EARLY–WRITE CYCLE



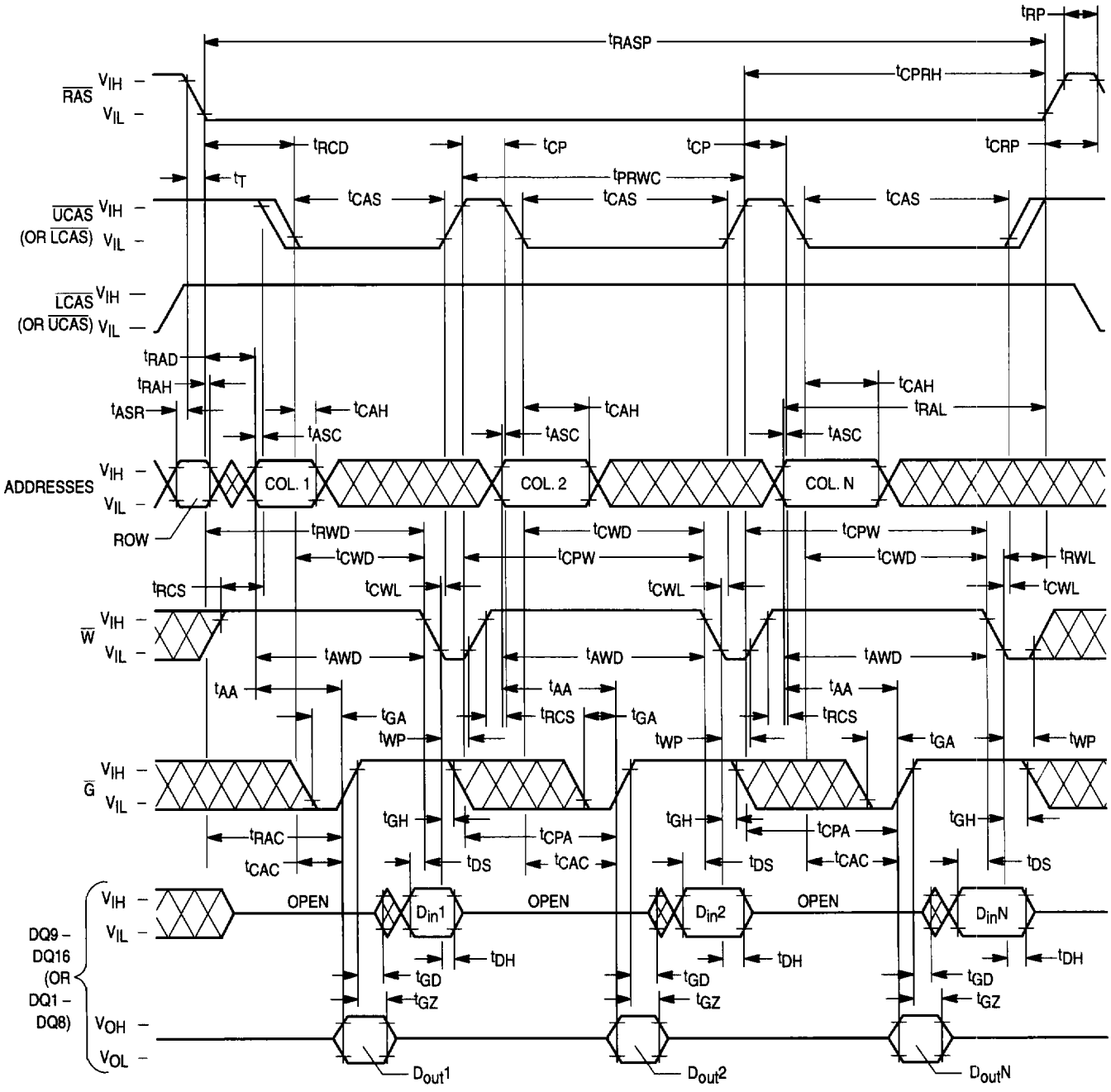
EDO PAGE MODE BYTE READ–EARLY–WRITE CYCLE



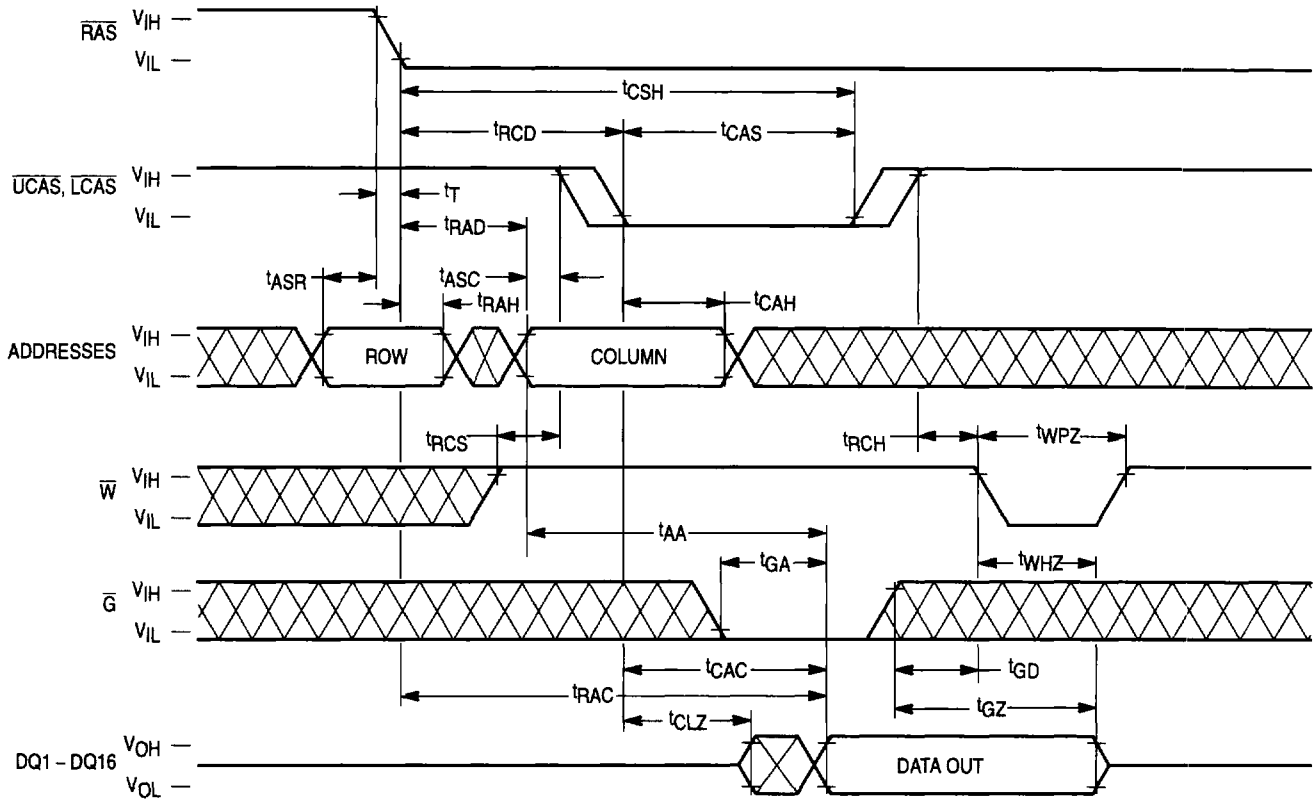
EDO PAGE MODE WORD READ–MODIFY–WRITE CYCLE



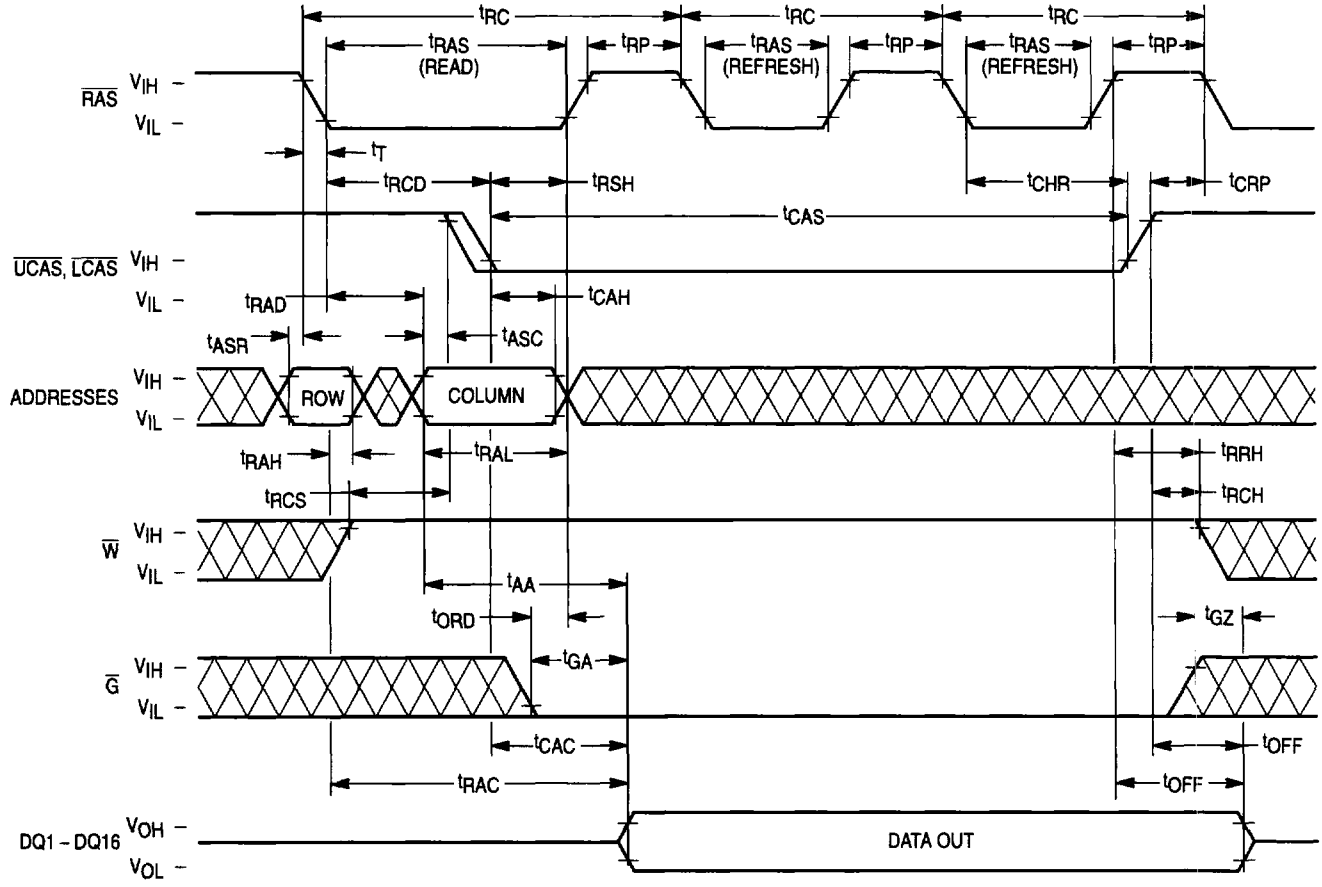
EDO PAGE MODE BYTE READ–MODIFY–WRITE CYCLE



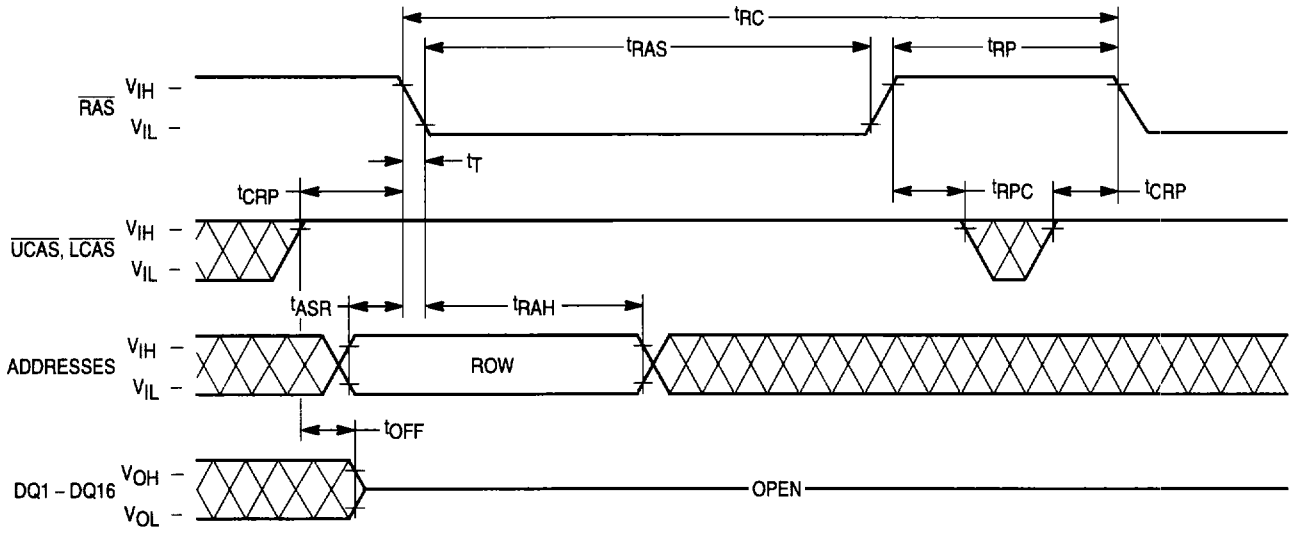
READ CYCLE WITH $\overline{W}$ CONTROLLED DISABLE



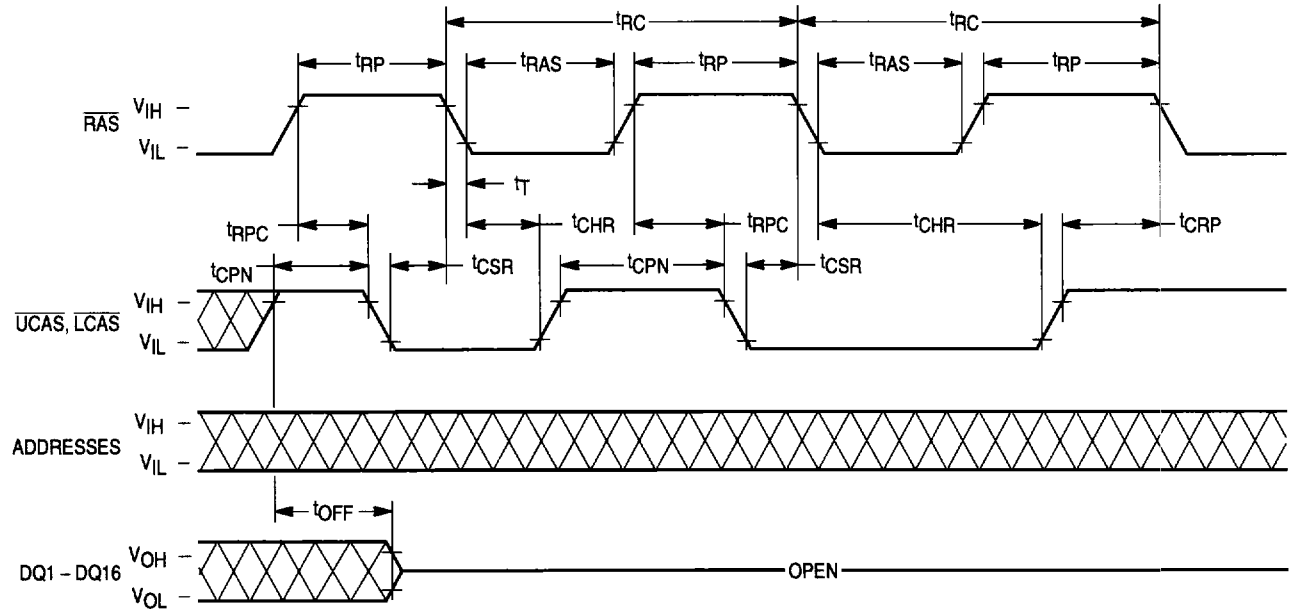
HIDDEN REFRESH CYCLE



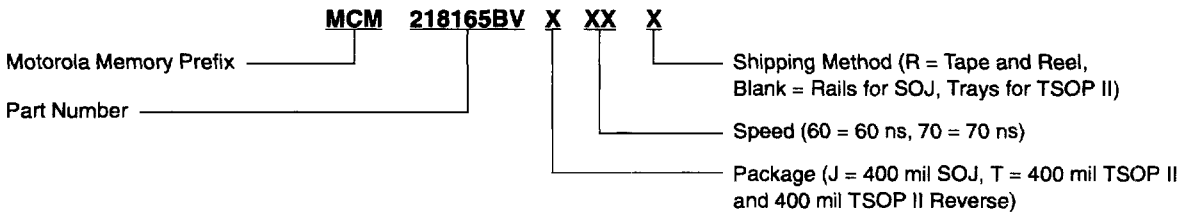
$\overline{\text{RAS}}$–ONLY REFRESH CYCLE



$\overline{\text{CAS}}$ BEFORE $\overline{\text{RAS}}$ REFRESH CYCLE



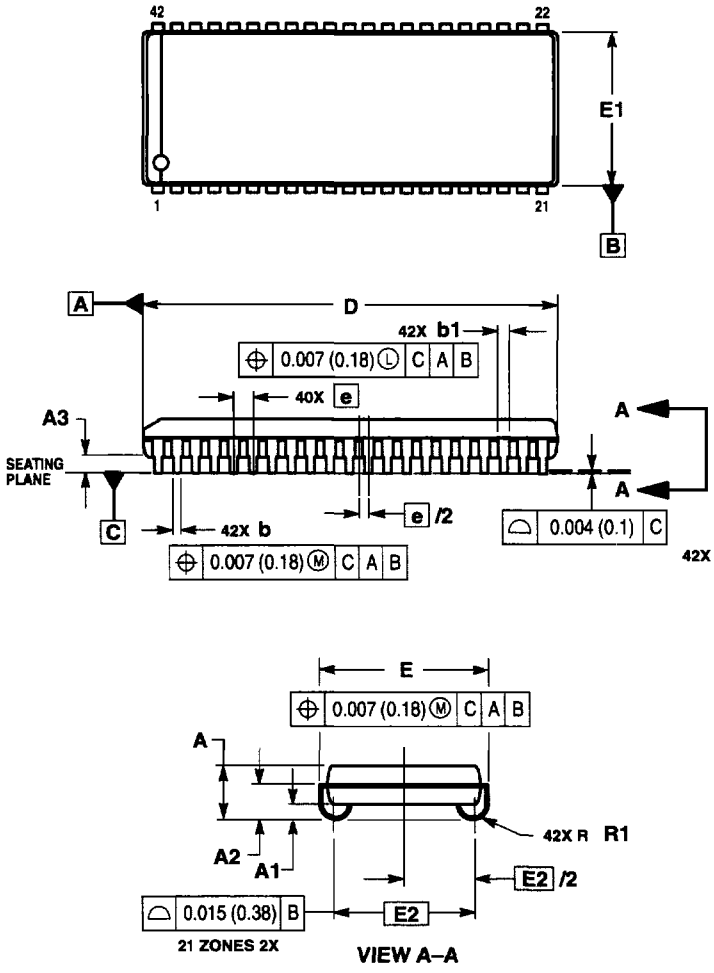
ORDERING INFORMATION
(Order by Full Part Number)



Full Part Numbers — MCM218165BVJ60 MCM218165BVJ60R MCM218165BVT60 MCM218165BVT60R
MCM218165BVJ70 MCM218165BVJ70R MCM218165BVT70 MCM218165BVT70R

PACKAGE DIMENSIONS

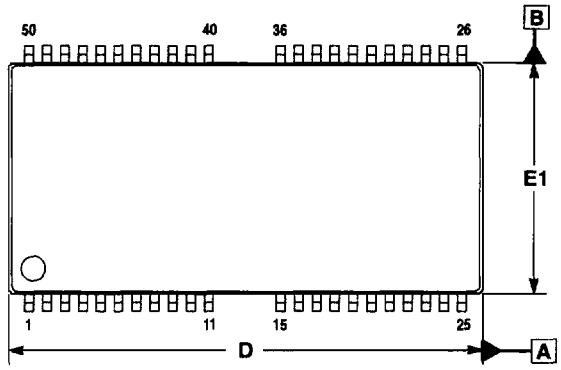
J PACKAGE
400 MIL SOJ
CASE 986B–01

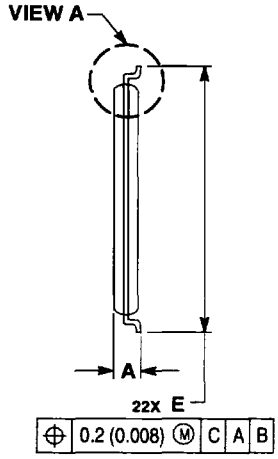


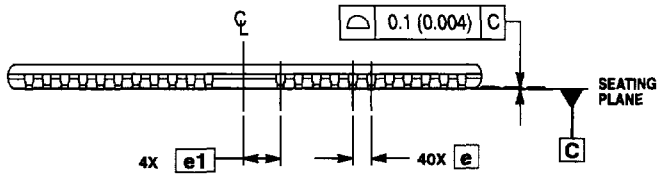
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION D DOES NOT INCLUDE MOLD FLASH, TIE BAR BURRS AND GATE BURRS. MOLD FLASH, TIE BAR BURRS AND GATE BURRS *SHALL NOT EXCEED 0.006 (0.15) PER END.* DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010 (0.25) PER SIDE.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONS D AND E1 AND, HENCE, DATUMS A AND B, ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DIMENSIONS b1 DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE SHOULDER WIDTH TO EXCEED b1 MAX BY MORE THAN 0.005 (0.13). THE DAMBAR INTRUSION(S) SHALL NOT REDUCE THE SHOULDER WIDTH TO LESS THAN 0.001 (0.03 BELOW b2 MIN.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.128	0.148	3.25	3.75
A1	0.025	—	0.635	—
A2	0.082	—	2.08	—
A3	0.035	0.045	0.89	1.14
b	0.015	0.020	0.38	0.50
b1	0.026	0.032	0.66	0.81
D	1.070	1.080	27.19	27.43
E	0.435	0.445	11.05	11.30
E1	0.395	0.405	10.03	10.28
E2	0.370 BSC		9.40 BSC	
e	0.050 BSC		1.27 BSC	
R1	0.030	0.040	0.76	1.01

T PACKAGE
400 MIL TSOP II
CASE 985A–01

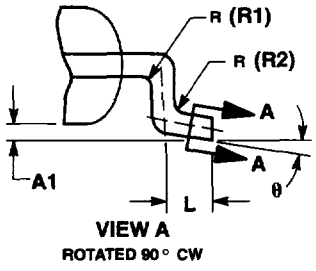




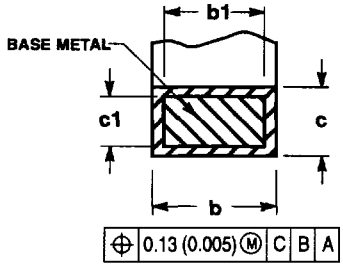


NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MM.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION IS 0.15 (0.006) MAXIMUM PER SIDE.
4. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSIONS. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.58 (0.023).
5. FOR LEAD IDENTIFICATION PURPOSES, PIN POSITIONS 12, 13, 14, 37, 38 AND 39 ARE NOT USED.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	—	1.20	—	0.047
A1	0.05	0.15	0.002	0.006
b	0.25	0.45	0.010	0.018
b1	0.25	0.40	0.010	0.016
c	0.12	0.25	0.005	0.010
c1	0.10	0.20	0.004	0.008
D	20.85	21.06	0.821	0.829
e	0.80 BSC		0.0315 BSC	
e1	1.60 BSC		0.063 BSC	
E	11.56	11.96	0.455	0.471
E1	10.06	10.26	0.396	0.404
L	0.40	0.60	0.016	0.024
R1	0.10 REF		0.004 REF	
R2	0.10 REF		0.004 REF	
θ	0 °	10 °	0 °	10 °



VIEW A
ROTATED 90 ° CW



SECTION A–A
44 PLACES

How to reach us:
USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado, 80217. 303–675–2140 or 1–800–441–2447

Mfax™: RMFAX0@email.sps.mot.com — TOUCHTONE 602–244–6609
INTERNET: http://Design–NET.com

JAPAN: Nippon Motorola Ltd.; Tatsumi–SPD–JLDC, 6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 81–3–3521–8315

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298