



Precision Adjustable Shunt Regulator

FEATURES

- Trimmed Bandgap to 1%
- Wide Operating Current 1mA to 150mA
- Extended Temperature Range 105°C
- Low Temperature Coefficient 30 ppm/°C
- Offered in TO-92, SOIC, SOT-89, μ SOIC™, & SOT-23-5
- Improved Replacement in Performance for TL431.
- Low Cost Solution

APPLICATIONS

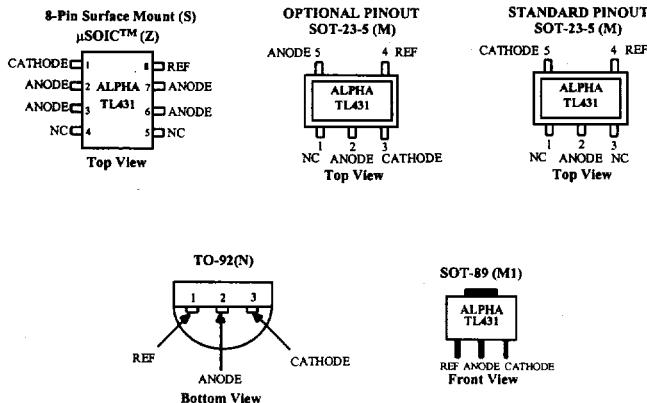
- Battery Operating Equipments
- Adjustable Supplies
- Switching Power Supplies
- Error Amplifiers
- Single Supply Amplifier
- Monitors / VCR / TV
- Personal Computers

PRODUCT DESCRIPTION

The ALPHA Semiconductor TL431 is a 3-terminal Adjustable Shunt Voltage Regulator providing a highly accurate 1% bandgap reference. TL431 acts as an open-loop error amplifier with a 2.5V temperature compensation reference. The TL431 thermal stability, wide operating current (150mA) and temperature range (105°C) makes it suitable for all variety of application are that looking for a low cost solution with high performance.

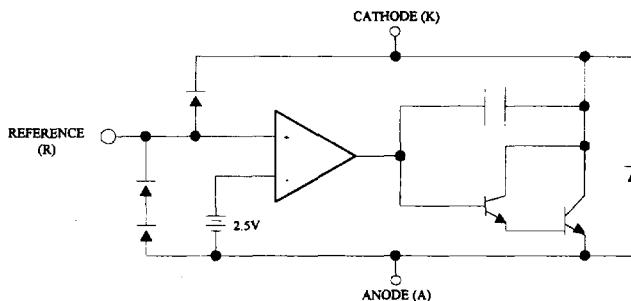
The output voltage may be adjusted to any value between V_{ref} and 36 volts with two external resistors. The TL431 is operating in full industrial temperature range of 0°C to 105°C. The TL431 is available in TO-92, SO-8, μ SOIC™, SOT-89, and SOT-23-5 packages. **ALPHA Semiconductor, is the only manufacture to offer TL431 in μ SOIC™ & SOT-23-5 pin with all above advantages.**

PIN CONFIGURATIONS



ORDERING INFORMATION

Part Number	Temperature Range	Package Type
TL431N	0°C to 105°C	TO-92
TL431M1	0°C to 105°C	SOT-89
TL431S	0°C to 105°C	SO-8
TL431Z	0°C to 105°C	μSOIC™
TL431M	0°C to 105°C	SOT-23-5



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNITS
Cathode-Anode Reverse Breakdown	V_{KA}	37	V
Anode-Cathode Forward Current	I_{AK}	1	A
Operating Cathode Current	I_{KA}	250	mA
Reference Input Current	I_{REF}	10	mA
Continuous Power Dissipation at 25°C	P_D		
TO-92		775	mW
8L SOIC		750	mW
SOT-89		1000	mW
Junction Temperature	T_J	150	°C
Storage Temperature	T_{STG}	- 65 to 150	°C
Lead Temperature (Soldering 10 sec.)	T_L	300	°C

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Cathode Voltage	V_{KA}	V_{REF} to 20	V
Cathode Current	I_k	10	mA

TYPICAL THERMAL RESISTANCES

PACKAGE	θ_{JA}	θ_{JC}	TYPICAL DERATING
TO-92	160° C/W	80° C/W	6.3 mW/°C
SOIC	175° C/W	45° C/W	5.7 mW/°C
SOT-89	110° C/W	8° C/W	9.1 mW/°C

ELECTRICAL CHARACTERISTICS at 25°C I_k @ 10mA $V_k = V_{ref}$ unless otherwise specified.

Parameter	Symbol	Test Conditions	TL431			Unit
			Min	Typ	Max	
Reference Voltage	V_{ref}	$T_A=25^\circ C$ TC=1 Over Temp. TC=1	2.470 2.449	2.495	2.520 2.541	V
ΔV_{ref} with Temp.*	TC	TC=1		0.07	0.20	mV/°C
Ratio of Change in V_{ref} to Cathode Voltage	$\Delta V_{ref} \Delta V_K$	V_{ref} to 10V 10V to 36V TC=2	-2.7 -2	-1.0 -0.4	0.3	mV/V
Reference Input Current	I_{ref}	TC=2		0.7	4	μA
I_{ref} Temp Deviation	ΔI_{ref}	Over Temp. TC=2		0.4	1.2	μA
Min I_k for Regulation	$I_k(\min)$	TC=1		0.4	1	mA
Off State Leakage	$I_k(\text{off})$	$V_{ref} = 0V$, $V_KA = 36V$ TC=3		0.04	250	nA
Dynamic Output Impedance	Z_{KA}	TC=1		0.15	0.5	Ω

TC = Test Circuit

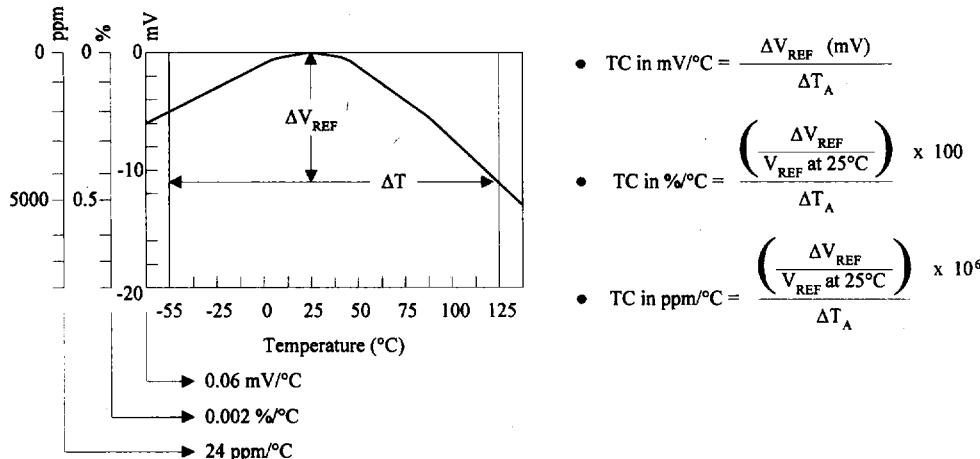
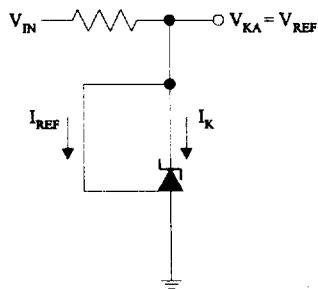
Calculating Average Temperature Coefficient (TC)**TEST CIRCUITS**

Figure 1a. Test Circuit 1

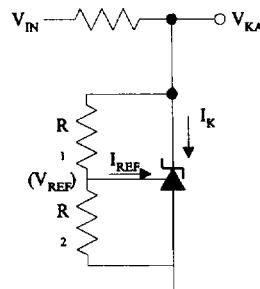


Figure 1b. Test Circuit 2

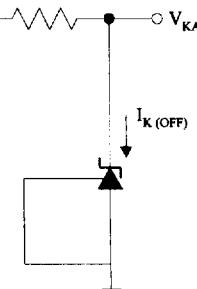


Figure 1c. Test Circuit 3

TYPICAL PERFORMANCE CURVES

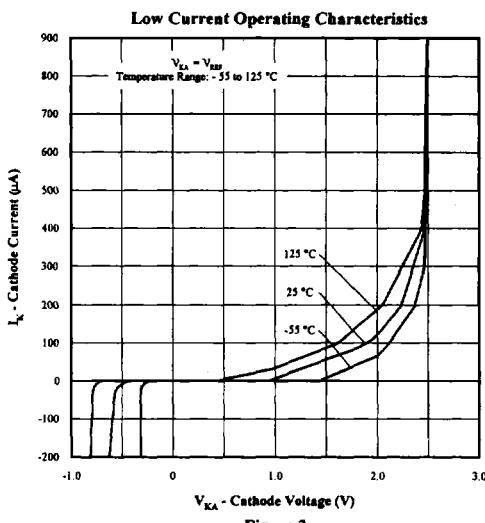


Figure 2

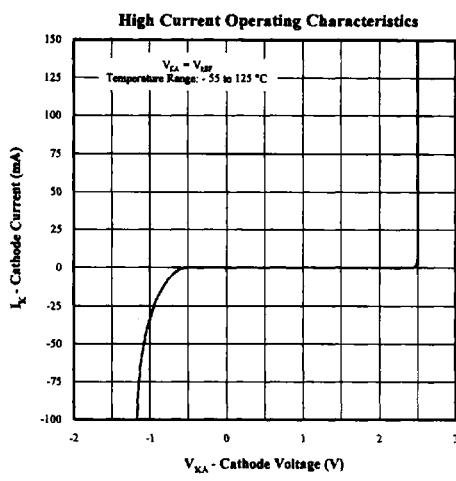


Figure 3

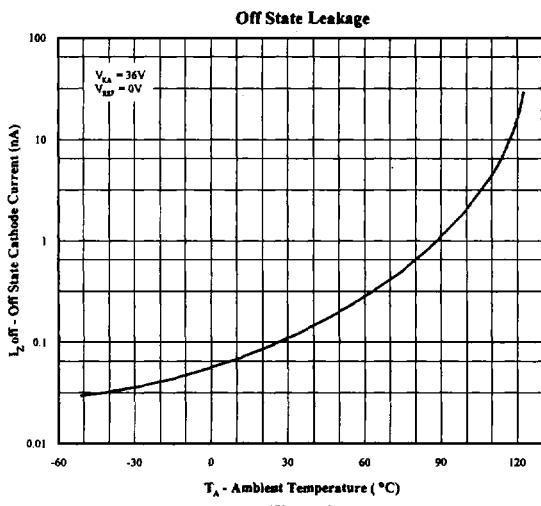


Figure 4

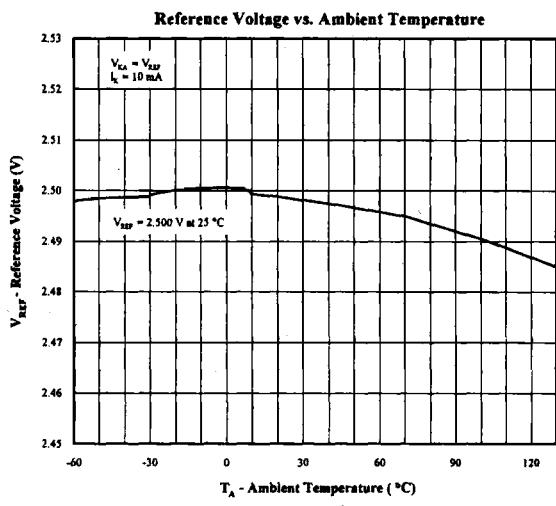


Figure 5

TYPICAL PERFORMANCE CURVES

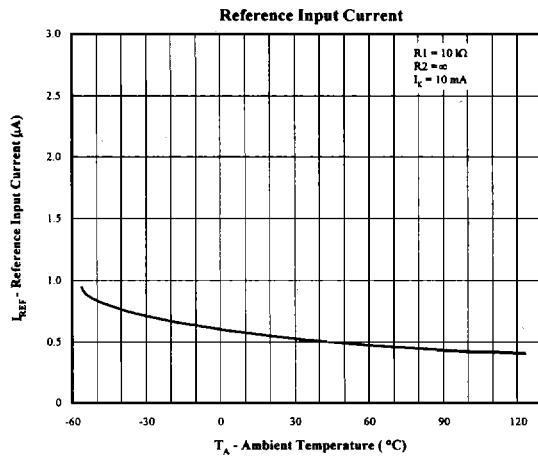


Figure 6

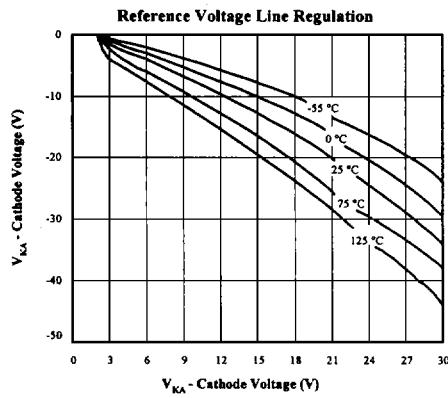


Figure 7

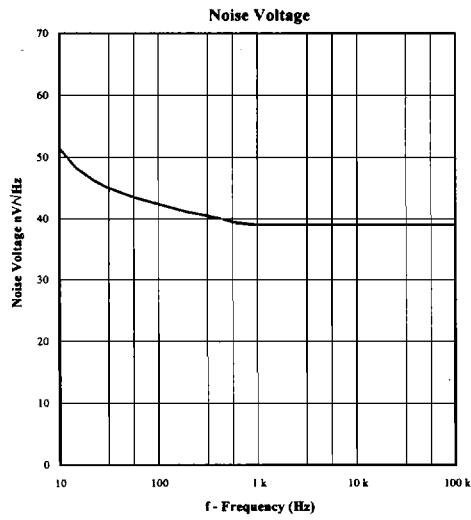


Figure 8

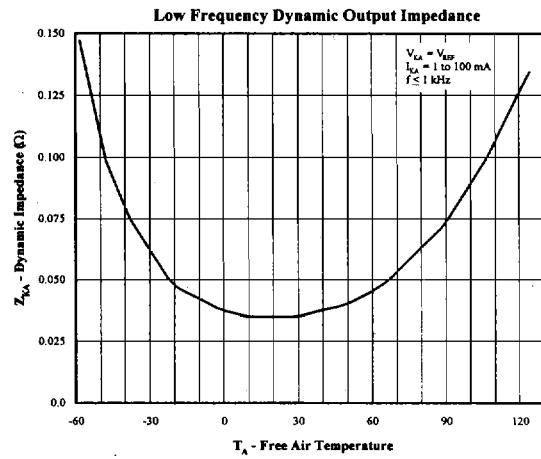


Figure 9

TYPICAL PERFORMANCE CURVES

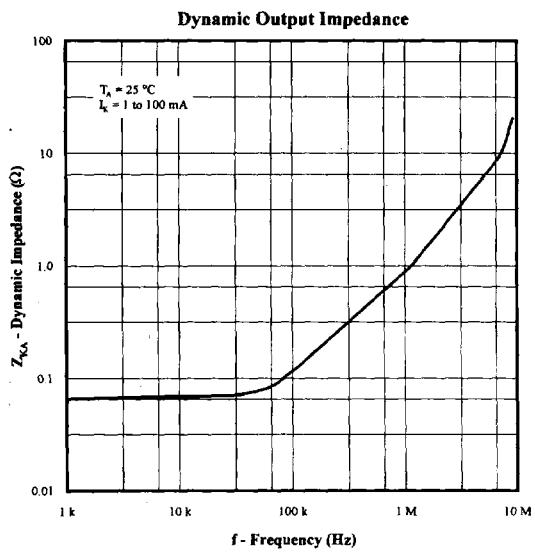


Figure 10

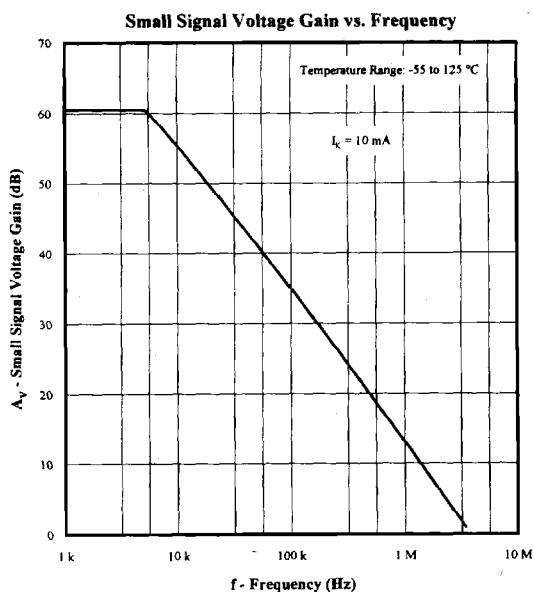
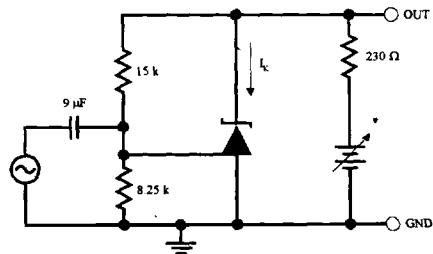


Figure 11



TYPICAL PERFORMANCE CURVES

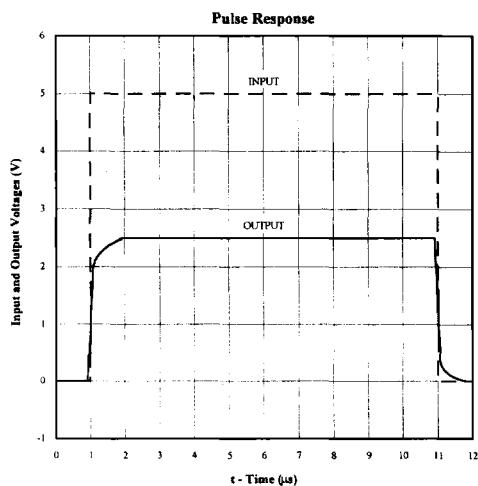


Figure 12

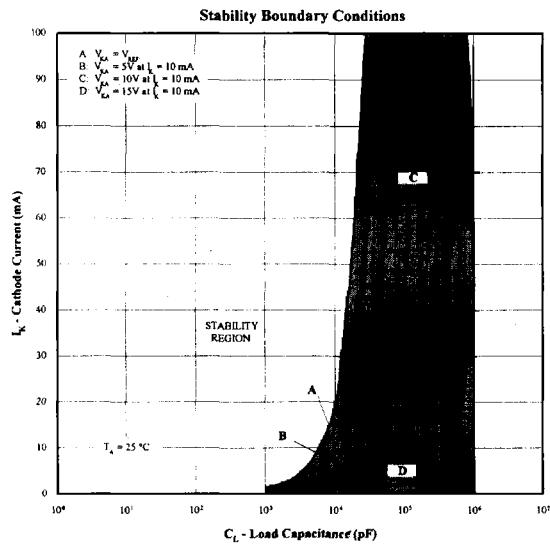
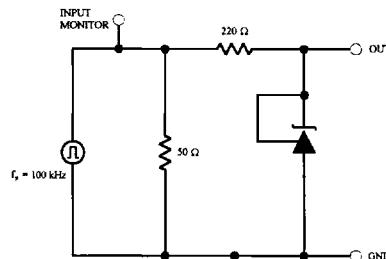


Figure 13

