

Features

- 4.5V–5.5V operation
- Low active power
 - Typical active current: 2.5 mA @ f = 1 MHz
 - Typical active current: 12.5 mA @ f = fmax
- Low standby current
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with \overline{CE} and \overline{OE} features
- CMOS for optimum speed and power
- Available in standard Pb-free and non Pb-free 32-lead (450-mil) SOIC and 32-lead TSOP II packages

Functional Description

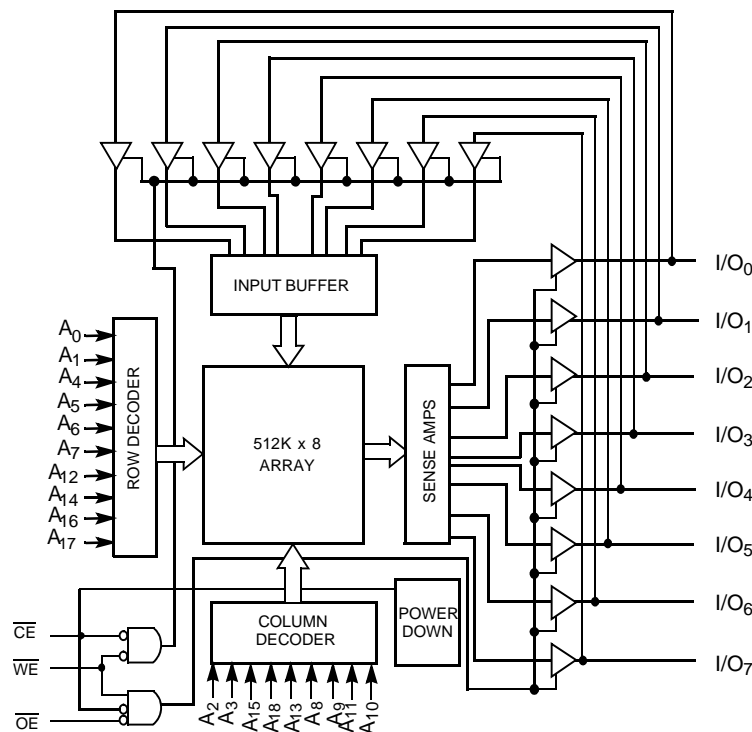
The CY62148BN is a high performance CMOS static RAM organized as 512K words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable (\overline{CE}), an active LOW Output Enable (\overline{OE}), and tri-state drivers. This device has an automatic power down feature that reduces power consumption by more than 99% when deselected.

To write to the device, take Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₁₈).

To read from the device, take Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing Write Enable (\overline{WE}) HIGH for read. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) go into a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), or a write operation is in progress (\overline{CE} LOW and \overline{WE} LOW).

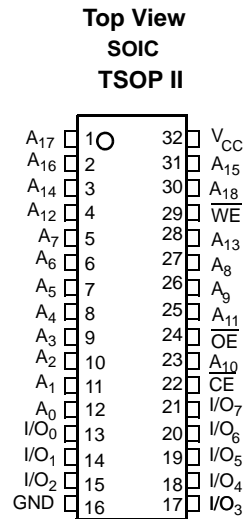
Logic Block Diagram



Contents

Functional Description	1	Write Cycle No. 2 (\overline{WE} Controlled, \overline{OE} HIGH During	
Pin Configuration	3	Write) ^[13, 14]	7
Product Portfolio	3	Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) ^[13, 14]	8
Maximum Ratings	4	Truth Table	8
Operating Range	4	Ordering Information	8
Electrical Characteristics Over the Operating Range	4	Package Diagrams	9
Capacitance ^[4]	4	Document History Page Sales, Solutions, and Legal Infor-	
AC Test Loads and Waveforms	4	mation	10
Switching Characteristics ^[5] Over the Operating Range	5	Worldwide Sales and Design Support	11
Data Retention Characteristics (Over the Operating Range)	6	Products	11
Data Retention Waveform	6	PSoC Solutions	11
Switching Waveforms	6		
Read Cycle No. 1 ^[10, 11]	6		
Read Cycle No. 2 (\overline{OE} Controlled) ^[11, 12]	6		
Write Cycle No. 1 (\overline{CE} Controlled) ^[13]	7		

Pin Configuration



Product Portfolio

Product	V _{CC} Range			Speed	Power Dissipation			
					Operating I _{CC} (mA)		Standby I _{SB2} (μA)	
	Min	Typ	Max		f = f _{max}		Typ ^[1]	Max
					Typ ^[1]	Max		
CY62148BNLL	4.5 V	5.0V	5.5V	70 ns	12.5	20	4	20

Note

1. Typical values are measured at V_{CC} = 5V, T_A = 25°C, and are included for reference only and are not tested or guaranteed.

Maximum Ratings

Exceeding the maximum rating may impair the device's useful life. User guidelines only and are not tested.

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage on V _{CC} to Relative GND	-0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ^[2]	-0.5V to V _{CC} +0.5V

DC Input Voltage ^[2]	-0.5V to V _{CC} +0.5V
Current into Outputs (LOW)	20 mA
Static Discharge Voltage	2001V (per MIL-STD-883, Method 3015)
Latch Up Current	>200 mA

Operating Range

Range	Ambient Temperature ^[3]	V _{CC}
Industrial	-40°C to +85°C	4.5V–5.5V

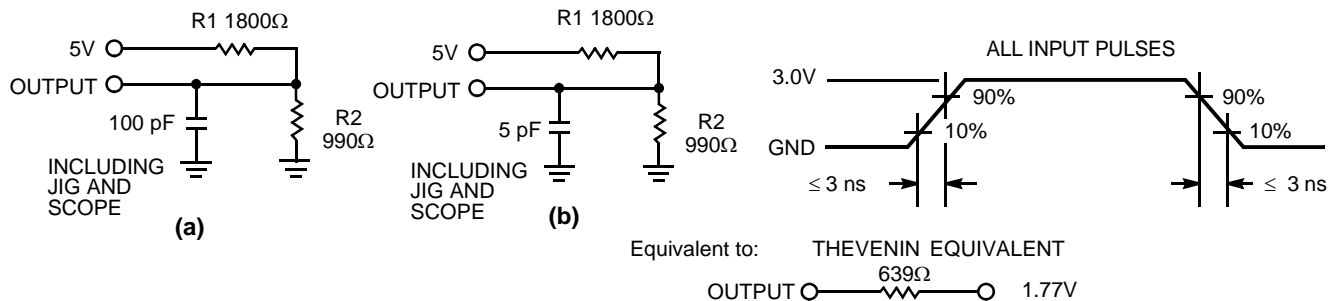
Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	CY62148BN			Unit
			Min	Typ ^[1]	Max	
V _{OH}	Output HIGH Voltage	I _{OH} = -1 mA	2.4			V
V _{OL}	Output LOW Voltage	I _{OL} = 2.1 mA			0.4	V
V _{IH}	Input HIGH Voltage		2.2		V _{CC} +0.3	V
V _{IL}	Input LOW Voltage		-0.3		0.8	V
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	-1		+1	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	-1		+1	μA
I _{CC}	V _{CC} Operating Supply Current	f = f _{MAX} = 1/t _{RC}		12.5	20	mA
		f = 1 MHz	I _{OUT} = 0 mA V _{CC} = Max.,	2.5		mA
I _{SB1}	Automatic CE Power Down Current – TTL Inputs	Max. V _{CC} , $\overline{CE} \geq V_{IH}$ V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}			1.5	mA
I _{SB2}	Automatic CE Power Down Current – CMOS Inputs	Max. V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0		4	20	μA

Capacitance^[4]

Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 5.0V	6	pF
C _{OUT}	Output Capacitance		8	pF

AC Test Loads and Waveforms



Notes

- V_{IL} (min.) = -2.0V for pulse durations of less than 20 ns.
- T_A is the "instant on" case temperature
- Tested initially and after any design or process changes that may affect these parameters.

Switching Characteristics^[5] Over the Operating Range

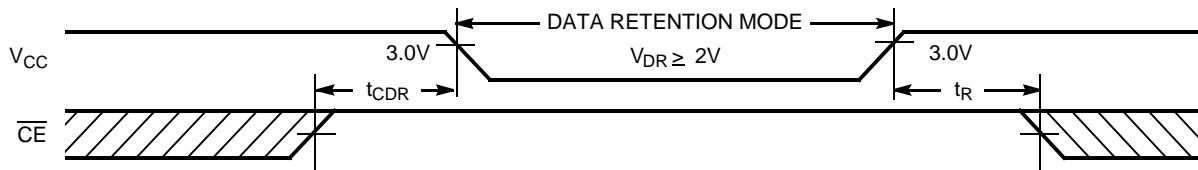
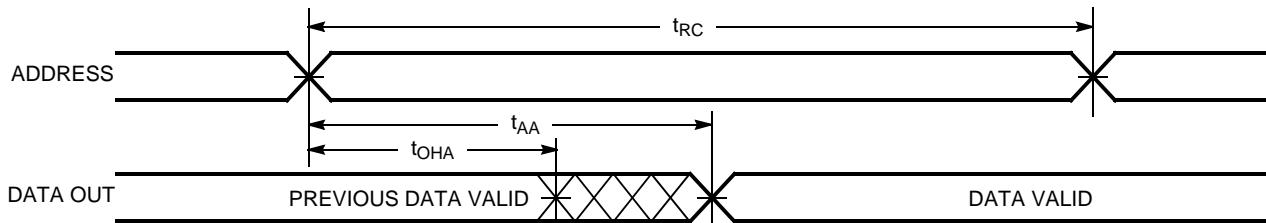
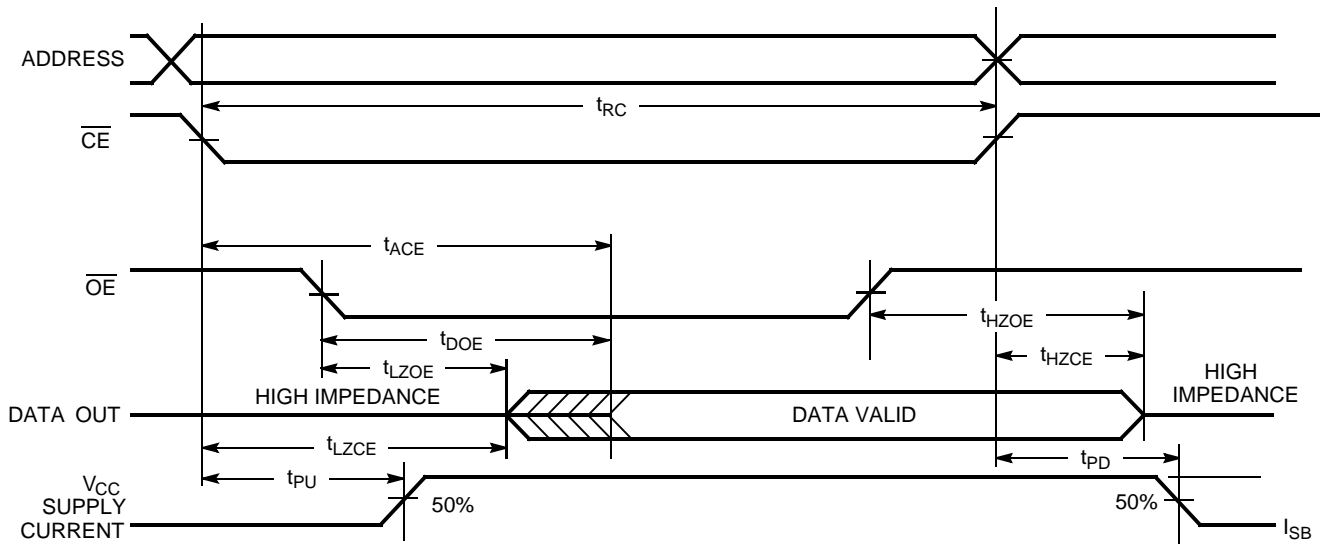
Parameter	Description	CY62148BN		Unit
		Min	Max	
READ CYCLE				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	\overline{CE} LOW to Data Valid		70	ns
t_{DOE}	\overline{OE} LOW to Data Valid		35	ns
t_{LZOE}	\overline{OE} LOW to Low Z ^[6]	5		ns
t_{HZOE}	\overline{OE} HIGH to High Z ^[6, 7]		25	ns
t_{LZCE}	\overline{CE} LOW to Low Z ^[6]	10		ns
t_{HZCE}	\overline{CE} HIGH to High Z ^[6, 7]		25	ns
t_{PU}	\overline{CE} LOW to Power Up	0		ns
t_{PD}	\overline{CE} HIGH to Power Down		70	ns
WRITE CYCLE^[8]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	\overline{CE} LOW to Write End	60		ns
t_{AW}	Address Setup to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	\overline{WE} Pulse Width	55		ns
t_{SD}	Data Setup to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{LZWE}	\overline{WE} HIGH to Low Z ^[6]	5		ns
t_{HZWE}	\overline{WE} LOW to High Z ^[6, 7]		25	ns

Notes

5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of \overline{CE} LOW, and \overline{WE} LOW. \overline{CE} and \overline{WE} must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the write.

Data Retention Characteristics (Over the Operating Range)

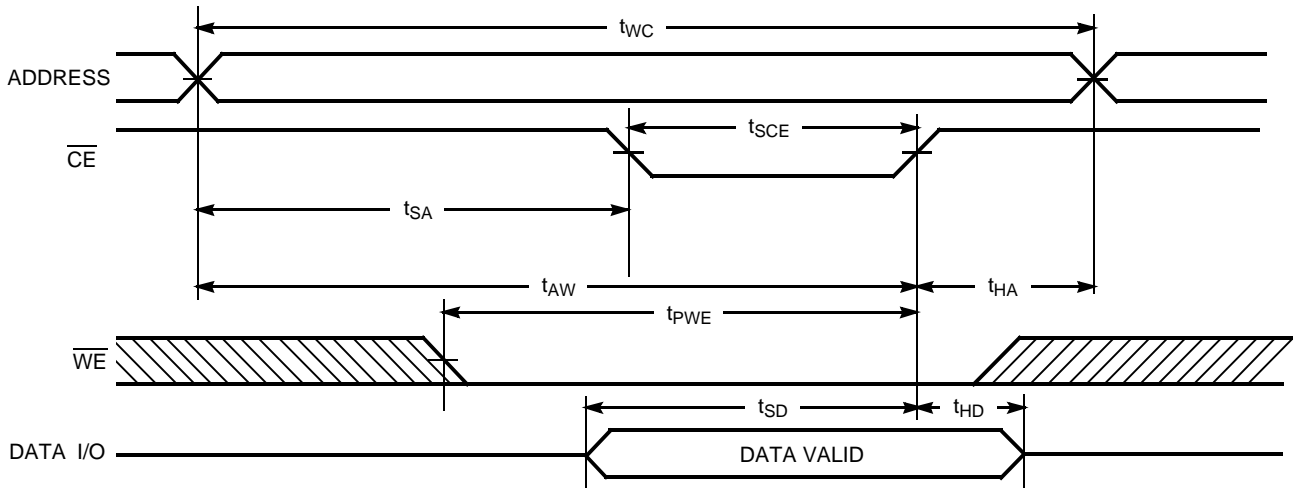
Parameter	Description	Conditions	Min	Typ ^[1]	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0			V
I_{CCDR}	Data Retention Current	No input may exceed $V_{CC} + 0.3V$			20	μA
$t_{CDR}^{[4]}$	Chip Deselect to Data Retention Time	$V_{CC} = V_{DR}$	0			ns
$t_R^{[9]}$	Operation Recovery Time	$CE > V_{CC} - 0.3V$ $V_{IN} > V_{CC} - 0.3V$ or $V_{IN} < 0.3V$	t_{RC}			ns

Data Retention Waveform

Switching Waveforms
Read Cycle No. 1^[10, 11]

Read Cycle No. 2 (\overline{OE} Controlled)^[11, 12]

Notes

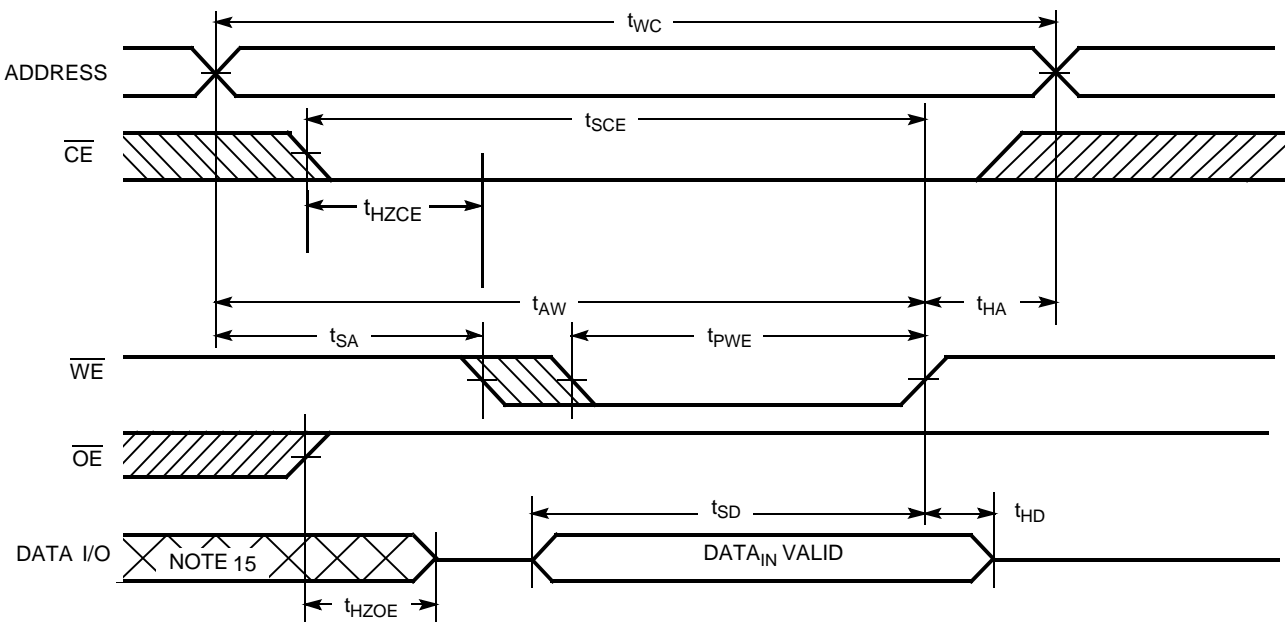
9. Full Device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ ms or stable at $V_{CC(min)} \geq 100$ ms.
10. Device is continuously selected. \overline{OE} , $\overline{CE} = V_{IL}$.
11. \overline{WE} is HIGH for read cycle.
12. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[13]



Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ HIGH During Write)^[13, 14]



Notes

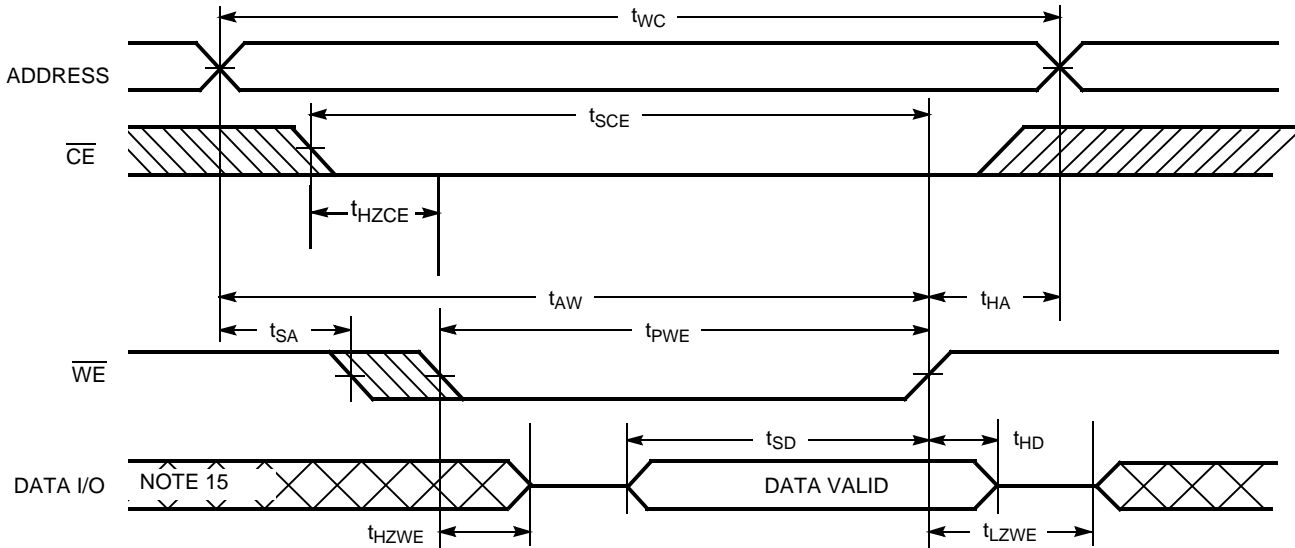
13. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high impedance state.

14. Data I/O is high-impedance if $\overline{\text{OE}} = V_{IH}$.

15. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[13, 14]



Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	I/O ₀ -I/O ₇	Mode	Power
H	X	X	High Z	Power Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62148BNLL-70SXI	51-85081	32-lead (450-Mil) Molded SOIC (Pb-Free)	Industrial
	CY62148BNLL-70ZXI	51-85095	32-lead TSOP II (Pb-Free)	

Note

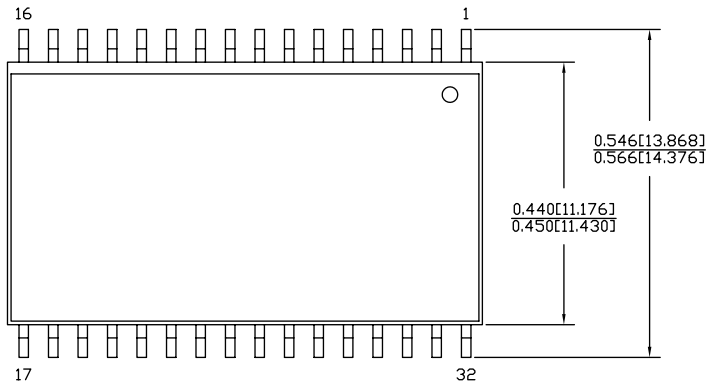
1. CY62148BNSL and CY62148BNLL are identical in specs.

Please contact your local Cypress sales representative for availability of these parts

Package Diagrams

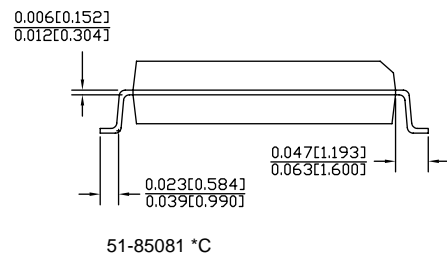
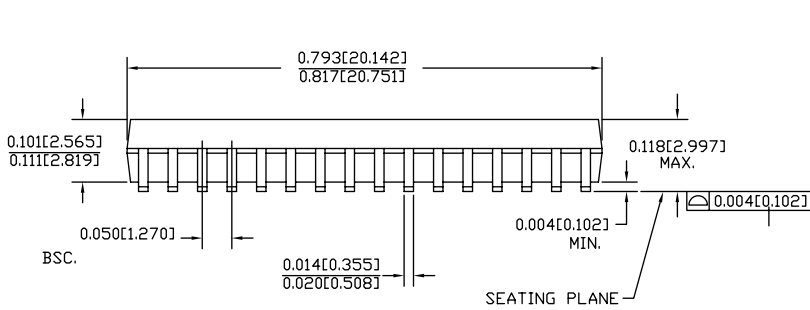
Figure 1. 32-lead (450 Mil) Molded SOIC (51-85081)

32 LD (450 Mil) SOIC



DIMENSIONS IN INCHES[MM] MIN. MAX.
 PACKAGE WEIGHT 1.42gms

PART #	
S32.45	STANDARD PKG.
SZ32.45	LEAD FREE PKG.

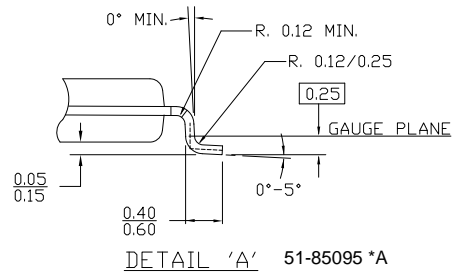
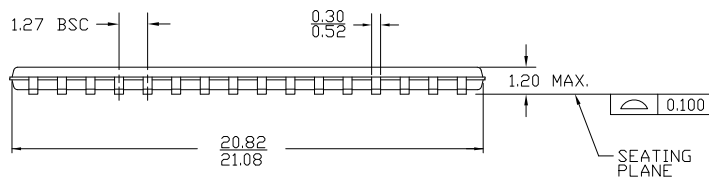
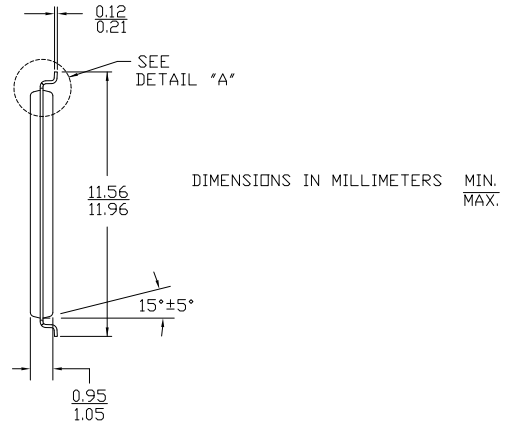
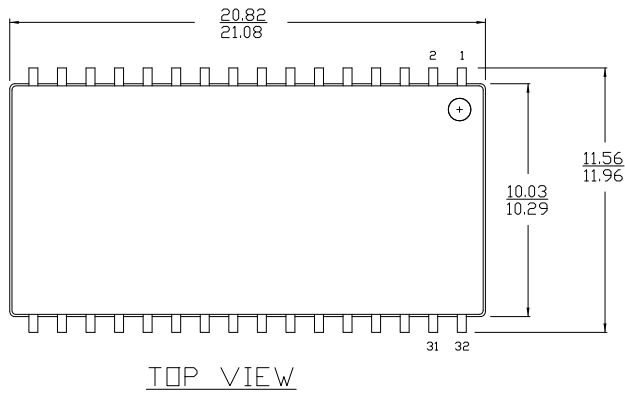


51-85081 *C

Package Diagrams (continued)

Figure 2. 32-Lead Thin Small Outline Package Type II (51-85095)

32 Lead TSOP TYPE II



Document History Page

Document Title: CY62148BN MoBL® 4-Mbit (512K x 8) Static RAM Document Number: 001-06517				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	426504	See ECN	NXR	New Data Sheet
*A	485639	See ECN	VKN	Corrected the typo in the Array size in the Logic Block Diagram
*B	832320	See ECN	NXR	Removed Commercial Operating Range Removed 32-lead Reverse TSOP II package from product offering Corrected the test condition typo error in Electrical Characteristics table Updated Ordering information table
*C	2896152	03/18/2010	AJU	Removed inactive parts from Ordering Information. Added Table of Contents. Updated Packaging Information Updated links in Sales, Solutions, and Legal Information.

© Cypress Semiconductor Corporation, 2006-2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and/or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.