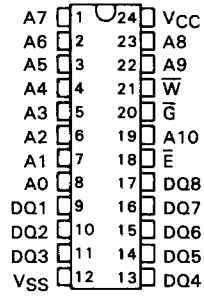
SMJ5517
2048-WORD BY 8-BIT STATIC RAM

DECEMBER 1983

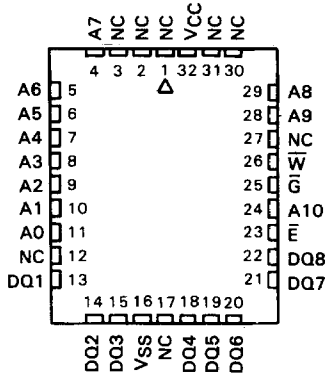
- 2K X 8 Organization, Common I/O
- Single +5-V Supply
- Fully Static Operation (No Clocks, No Refresh)
- JEDEC Standard Pinout
- 24-Pin 600-Mil (15,2 mm) Package Configuration
- Pin Compatible with TMS2516, TMS4016, MB8416, HM6116, and TC5517
- 8-Bit Output for Use in Microprocessor-Based Systems
- 3-State Outputs with $\overline{E}$ for OR-ties
- All Inputs and Outputs Fully TTL Compatible
- Fanout to One Series 54S/74S, Five Series 54LS/74LS or Twenty Series 54ALS/74ALS TTL Loads
- Complementary Silicon Gate MOS Technology with a Six Transistor Memory Cell
- Power Dissipation:
  - Operating — 150 mW Typical
  - Standby — 5 mW Typical
  - Data Retention — 50 μW Typical
- Performance Ranges:

	ACCESS TIME (MAX)
SMJ5517-15	150 ns
SMJ5517-20	200 ns

SMJ5517 . . . JD PACKAGE†
(TOP VIEW)



SMJ5517 . . . FG PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A10	Address
DQ1-DQ8	Data In/Data Out
$\overline{E}$	Chip Enable/Power Down
$\overline{G}$	Output Enable
V_{CC}	+5-V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

The SMJ5517 static random-access memory is organized as 2048 words of 8-bits each. Fabricated using complementary silicon-gate MOS technology, the SMJ5517 operates at high speed and uses less power than conventional NMOS 2K × 8 static RAMs. It is fully compatible with Series 54/74, Series 54S/74S, or 54LS/74LS TTL. Its static design means that no refresh clocking circuitry is needed and timing requirements are simplified. Access time is equal to cycle time. A chip-enable control is provided for controlling the flow of data-in and data-out and another output enable function is included to allow faster access time.

The SMJ5517 static RAM has the same standard pinout as TI's compatible 16K SRAMs, and EPROMs. This makes the SMJ5517 plug-in compatible with the '4016 and the '2516. Few modifications, if any, are needed for other 16K

† Low cost J package available soon.

ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

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5-V SRAM or EPROM. This allows the microprocessor system designer complete flexibility in partitioning his memory board between read/write and nonvolatile storage. Of special importance is the data retention feature of the SMJ5517, as long as $V_{CC} \geq 2$ V, the device retains data indefinitely.

The SMJ5517 is offered in a 24-pin dual-in-line ceramic sidebraze package (JD suffix) and in a 32-pad leadless ceramic chip carrier (FG). The JD package is designed for insertion in mounting-hole rows on 600-mil (15,2 mm) centers, whereas the FG package is intended for surface mounting on solder pads on 0.050-inch (1,27 mm) centers. The FG package offers a three layer rectangular chip carrier with dimensions $0.450 \times 0.550 \times 0.100$ ($11,43 \times 13,97 \times 2,54$).

operation

addresses (A0-A10)

The eleven address inputs select one of the 2048 8-bit words in the RAM. The address-inputs must be stable for the duration of a write cycle.

chip enable/power down ($\overline{E}$)

The chip enable/power down terminal affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip enable/power down is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip enable/power down terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

output enable ($\overline{G}$)

The output-enable terminal affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory location.

data-in/data-out (DQ1-DQ8)

Data can be written into a selected device when the write-enable input is low. The three-state output buffer provides direct TTL compatibility with a fan-out of one Series 54S/74S, five Series 54LS/74LS, or twenty Series 54ALS/74ALS TTL loads. The D/Q terminals are in the high-impedance state when output enable ($\overline{G}$) is high, chip enable ($\overline{E}$) is high, or whenever a write operation is being performed. Data-out is the same polarity as data-in.

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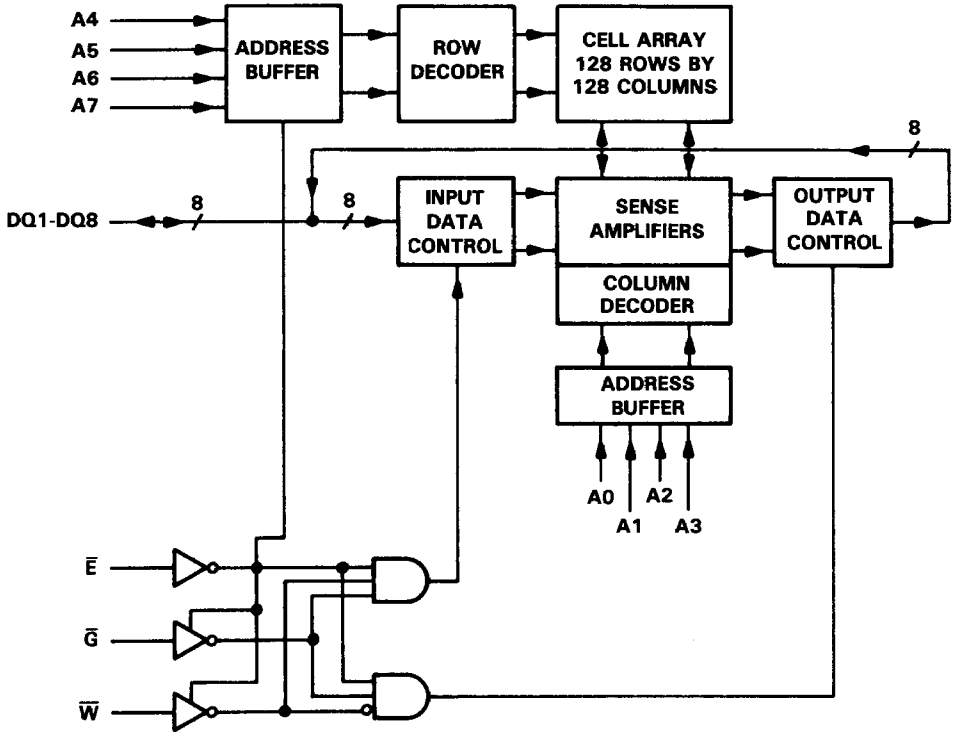
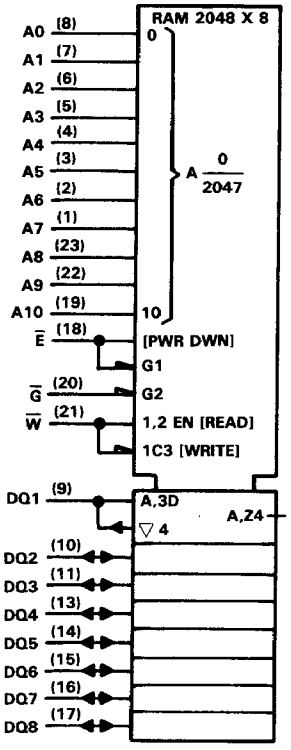
functional block diagram



logic symbol†



FUNCTION TABLE

W̅	Ē	G̅	DQ1-DQ8	MODE
L	L	X	VALID DATA	WRITE
H	L	L	DATA OUTPUT	READ
X	H	X	HI-Z	POWER DOWN
H	L	H	HI-Z	OUTPUT DISABLED

† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 10-1.

absolute maximum ratings over operating case temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1)	−0.5 V to 7 V
Input voltage (any input) (see Note 1)	−1 V to 7 V
Continuous power dissipation	1 W
Operating case temperature range	−55°C to 125°C
Storage temperature range	−55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Voltage values are with respect to the V_{SS} terminal.

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recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.2		$V_{CC}+0.2$	V
Low-level input voltage, V_{IL} (see Note 2)	$V_{SS}-0.2$		0.8	V
Operating case temperature, T_C	−55		125	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = −2 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 2 mA			0.4	V
I_I	Input current	All inputs except DQ1-DQ8	V_I = 0 V to 5.5 V, V_{CC} = 5.5 V	−1		1	μA
		DQ1-DQ8 inputs only		−5		5	μA
I_{CC1}	Operating supply current from V_{CC}		V_{CC} = 5.5 V,		30	90	mA
I_{CC2}	Standby supply current from V_{CC}		I_O = 0, $\overline{E}$ = V_{IH} MIN			5	mA
I_{CC3}	Data retention supply current from V_{CC}		$\overline{E}$ = V_{CC} −0.2 V			100	μA
$V_{CC(DR)}$	V_{CC} required for data retention		$\overline{E}$ = $V_{CC(DR)}$ −0.2 V	2		5.5	V

† All typical values are at V_{CC} = 5 V, T_C = 25°C.

timing requirements over recommended supply voltage range and operating case temperature range†

PARAMETER		SMJ5517-15		SMJ5517-20		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	150		200		ns
$t_{c(W)}$	Write cycle time	150		200		ns
$t_{w(W)}$	Write pulse duration	90		120		ns
$t_{su(A)}$	Address setup time	10		10		ns
$t_{su(E)}$	Chip enable setup time	90		120		ns
$t_{su(D)}$	Data setup time	50		70		ns
$t_{h(A)}$	Address hold time	10		10		ns
$t_{h(D)}$	Data hold time	10		10		ns
t_{AVWH}	Address valid to write enable high	100		130		ns

† AC test conditions:
Input pulse levels: 0.8 V and 2.2 V
Input rise and fall times: t_r = t_f = 5 ns
Input and output timing reference levels: 0.8 v and 2.2 V
Output load: 1 TTL gate, C_L = 100 pF

switching characteristics over recommended supply voltage range and operating case temperature range†

PARAMETER		SMJ5517-15		SMJ5517-20		UNIT
		MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200	ns
$t_{a(E)}$	Access time from chip enable low		150		200	ns
$t_{a(G)}$	Access time from output enable low		60		70	ns
$t_{v(A)}$	Output data valid after address change	10		10		ns
$t_{dis(E)}$	Output disable time after chip enable high		50		60	ns
$t_{dis(G)}$	Output disable time after output enable high		50		60	ns
$t_{dis(W)}$	Output disable time after write enable low		50		50	ns
$t_{en(E)}$	Output enable time after chip enable low	0		0		ns
$t_{en(G)}$	Output enable time after output enable low	0		0		ns
$t_{en(W)}$	Output enable time after write enable high	0		0		ns

† AC test conditions:
Input pulse levels: 0.8 V and 2.2 V
Input rise and fall times: $t_r = t_f = 5$ ns
Input and output timing reference levels: 0.8 V and 2.2 V
Output load: 1 TTL gate, $C_L = 100$ pF

capacitance over recommended supply voltage and operating case temperature ranges, f = 1 MHz†

PARAMETER		TEST CONDITIONS	TYP‡	MAX	UNIT
C_i	Input capacitance	$V_I = 0$ V, f = 1 MHz	5	10	pF
C_o	Output capacitance	$V_O = 0$ V, f = 1 MHz	5	10	pF

† Capacitance measurements are made on a sample basis only.
‡ Typical values are $T_C = 25°C$ and nominal voltages.

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PARAMETER MEASUREMENT INFORMATION

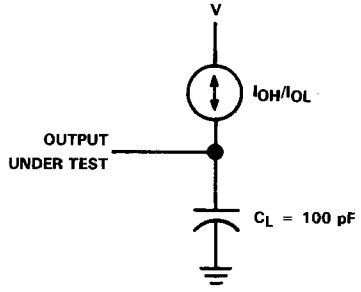
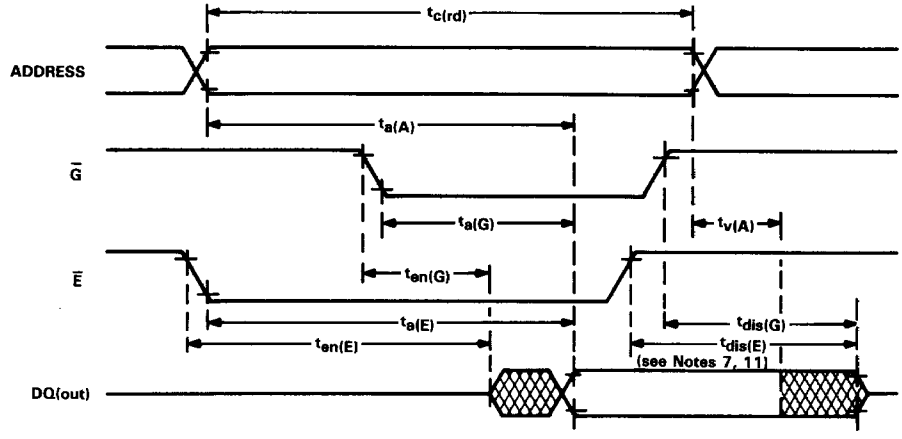


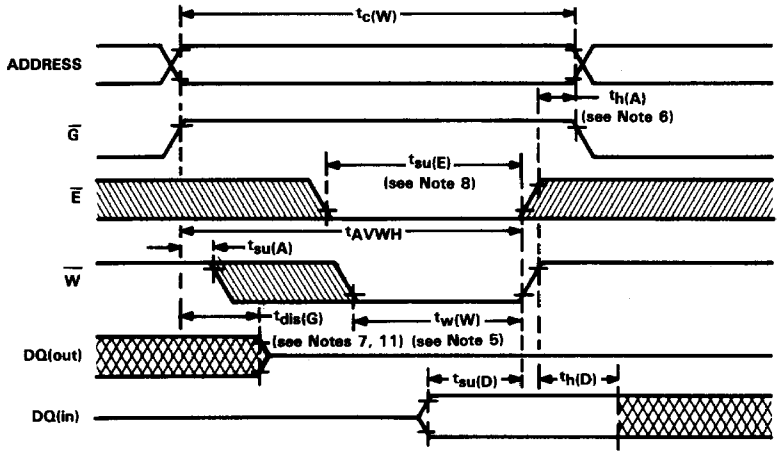
FIGURE 1 – EQUIVALENT LOAD CIRCUIT

timing waveform of read cycle (see note 3)

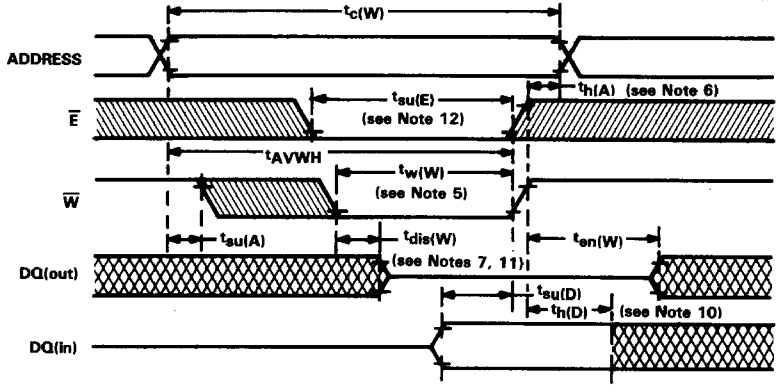


All timing reference points are 0.8 V and 2.2 V.
NOTE 3: $\overline{W}$ is high for Read Cycle.

timing waveform of write cycle no. 1 (see note 4)



timing waveform of write cycle no. 2 (see notes 4 and 9)



All timing reference points are 0.8 V and 2.2 V.

NOTES:
4. $\overline{W}$ must be high during all address transitions.
5. A write occurs during the overlap of a low $\overline{E}$ and a low $\overline{W}$.
6. $t_{h(A)}$ is measured from the earlier of $\overline{E}$ or $\overline{W}$ going high to the end of the write cycle.
7. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
8. If the $\overline{E}$ low transition occurs simultaneously with the $\overline{W}$ low transitions or after the $\overline{W}$ transition, output remains in a high impedance state.
9. $\overline{G}$ is continuously low ($\overline{G}$ = V_{IL}).
10. If $\overline{E}$ is low during this period, I/O pins are in the output state. Data input signals of opposite phase to the outputs must not be applied.
11. Transition is measured ±200 mV from steady-state voltage.
12. If the $\overline{E}$ low transition occurs before the $\overline{W}$ low transition, then the data input signals of opposite phase to the outputs must not be applied for the duration of $t_{dis(W)}$ after the $\overline{W}$ low transition.

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schematics of inputs and outputs