1.1 Scope.

This specification covers the detail requirements for a complete 12-bit, voltage output, D/A converter (DACPORT®) with output amplifier and Zener voltage reference on a monolithic chip.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
−1	AD7245AT(X)/883B
−2	AD7248AT(Y)/883B

1.2.3 Case Outline.

See Appendix 1 of General Specification ADI-M-1000: package outline:

(X)	(Y)	Package	Description
Q		Q-24	24-Pin Cerdip
E		E-28A	28-Pin LCC
	Q	Q-20	20-Pin Cerdip

1.3 Absolute Maximum Ratings.

Positive Supply Voltage (V_{DD}) to AGND . . . . . −0.3 V to +17.0 V
Positive Supply Voltage (V_{DD}) to DGND . . . . . −0.3 V to +17.0 V
V_{DD} to V_{SS} . . . . . +0.3 V to +34 V
AGND to DGND . . . . . 0.3 V to V_{DD}
Digital Input Voltage to DGND . . . . . −0.3 V to V_{DD} + 0.3 V
V_{OUT} to AGND . . . . . V_{SS} to V_{DD}
V_{OUT} to V_{SS} . . . . . 0 V to +24 V
V_{OUT} to V_{DD} . . . . . −32 V to 0 V
Voltage Reference Output (REF OUT) to AGND . . . . . 0 V to V_{DD}
Power Dissipation to +75°C . . . . . 450 mW
Storage Temperature Range . . . . . −65°C to +150°C
Lead Temperature (Soldering 10 sec) . . . . . +300°C

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Table 1. Electrical Performance Characteristics (Dual Supply)

Test	Symbol	Device	Limits Min	Limits Max	Sub Groups	Test Condition[1] ($-55°C \le T_C \le +125°C$ unless otherwise noted)	Unit
Resolution	RES	−1, 2		12	1, 2, 3		Bits
Relative Accuracy	RA	−1, 2	−0.75	+0.75	1, 2, 3	V_{DD} = +11.4 V to +15.75 V V_{SS} = −11.4 V to −15.75 V	LSB
Differential Nonlinearity	DNL	−1, 2	−1	+1	1, 2, 3	Guaranteed Monotonic	LSB
Bipolar Offset Error		−1, 2	2	2	1		LSB
			4	4	2, 3		
DAC Gain Error[2]	GE	−1, 2	−2	+2	1, 2, 3		LSB
Full-Scale Output Voltage Error[3]	$V_{OUT}E$	−1, 2	−0.2	+0.2	1	V_{DD} = +12 V and +15 V V_{SS} = −12 V and −15 V	% FSR
			−0.6	+0.6	2, 3		
ΔFull Scale/ΔV_{DD}		−1, 2	−0.06	+0.06	1	V_{DD} = ±5%	% FSR/V
ΔFull Scale/ΔV_{SS}		−1, 2	−0.01	+0.01	1		% FSR/V
ΔOffset/ΔV_{DD}		−1, 2	−2	+2	1, 2, 3	V_{DD} = ±5%	mW
ΔOffset/ΔV_{SS}		−1, 2	−1	+1	1, 2, 3	V_{SS} = ±5%	mV
Reference Output		−1, 2	4.99	5.01	1	V_{DD} = +12 V and +15 V V_{SS} = −12 V and −15 V	V
ΔReference/ΔV_{DD}		−1, 2		6	1	V_{DD} = ±5%	mV/V
Reference Load Sensitivity		−1, 2	−1.5	+1.5	1, 2, 3	Reference Load Current Change (0 μA–100 μA). Not Including R_{OFS} Current	mV
Digital Input High Voltage	V_{INH}	−1, 2	2.4		1, 2, 3		V
Digital Input Low Voltage	V_{INL}	−1, 2		0.8	1, 2, 3		V
Digital Input Current for Data Inputs	I_{IN}	−1, 2	−10	+10	1, 2, 3	V_{IN} = 0 or V_{DD}	μA
Digital Input High for Control Inputs[4]	I_{INH}	−1, 2	−1	+1	1	V_{IN} = V_{DD}	μA
			−10	+10	2, 3		
Digital Input Low for Control Inputs	I_{INL}	−1, 2		150	1	V_{IN} = 0 V	μA
				200	2, 3		
Digital Input Capacitance	C_{IN}	−1, 2		8	4		pF
Output Range Resistor	R_{OUT}	−1, 2	15	30	1, 2, 3		kΩ
Output Ranges[5]		−1, 2	0	+5	1, 2, 3	Pin Strappable Minimum Load Resistance Is 2 kΩ to GND	V
			0	+10			
			−5	+5			
Power Supply Current	I_{DD}	−1, 2		12	1, 2, 3	Output Unloaded	mA
	I_{SS}			5			
Output Voltage Settling Positive and Negative Full-Scale Change[6]	t_{SL}	−1, 2		10	13[7]	To ±0.5 LSB, R_L = 2 kΩ	μs

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Test	Symbol	Device	Limits Min	Limits Max	Sub Groups	Test Condition[1] ($-55°C \le T_C \le +125°C$ unless otherwise noted)	Unit
Output Voltage Slew Rate	SR	−1, 2	1.5		13, 14, 15[7]		V/μs
Chip Select Pulse Width	t_1	−1, 2	100		9, 10, 11		ns
Write Pulse Width	t_2	−1, 2	80		9, 10, 11		ns
			100				
Chip Select to Write Setup	t_3	−1, 2	0		9, 10, 11		ns
Chip Select to Write Hold	t_4	−1, 2	0		9, 10, 11		ns
Data Valid to Write Setup Time	t_5	−1, 2	80		9, 10, 11		ns
Data Valid to Write Hold Time	t_6	−1, 2	10		9, 10, 11		ns
Load DAC Pulse Width	t_7	−1, 2	100		9, 10, 11		ns
Clear Pulse Width	t_8	−1, 2	100		9, 10, 11		ns

NOTES
[1]Dual Supply: V_{DD} = +11.4 V to +15.75 V; V_{SS} = −11.4 V to −15.75 V; AGND = DGND = 0 V; R_L = 2 kΩ to GND; C_L = 100 pF to GND. REF unloaded unless otherwise noted.
[2]This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.
[3]This error is calculated with respect to an ideal 4.9988 V (on the 5 V range) or 9.9976 V (on the 10 V range). Typical full-scale temperature coefficient is ±30 ppm of FSSR/°C.
[4]Control Inputs are $\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$ and $\overline{CLR}$ for Device 1 and $\overline{CSMB}$, $\overline{CSLOSB}$, $\overline{WR}$ and $\overline{LDAC}$ for Device 2.
[5]0 V to +10 V applies to V_{DD} = +15 V ± 5% only, and V_{SS} = −15 V ± 5%.
[6]For positive full-scale change, DAC register loaded all 0s to all 1s. For negative full-scale change, DAC register loaded all 1s to all 0s.
[7]Special Subgroups 13, 14, 15 (as referenced) shall be measured only for the initial test, or after process or design changes which may affect the parameter in those subgroups. Subgroup 13 is +25°C tests, Subgroup 14 is +125°C tests and Subgroup 15 is −25°C tests.

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Table 2. Electrical Performance Characteristics (Single Supply)

Test	Symbol	Device	Limits Min	Limits Max	Sub Groups	Test Condition[1] ($-55°C \le T_C \le +125°C$ unless otherwise noted)	Unit
Resolution	RES	−1, 2		12	1, 2, 3		Bits
Relative Accuracy	RA	−1, 2	−0.75	+0.75	1, 2, 3	V_{DD} = +11.4 V to +15.75 V	LSB
Differential Nonlinearity	DNL	−1, 2	−1	+1	1, 2, 3	Guaranteed Monotonic	LSB
Unipolar Offset Error		−1, 2	2	2	1		LSB
			4	4	2, 3		
DAC Gain Error[2]	GE	−1, 2	−2	+2	1, 2, 3		LSB
Full-Scale Output Voltage Error[3]	$V_{OUT}E$	−1, 2	−0.2	+0.2	1	V_{DD} = +12 V and +15 V	% FSR
			−0.6	+0.6	2, 3		
ΔFull Scale/ΔV_{DD}		−1, 2	−0.06	+0.06	1	V_{DD} = ±5%	% FSR/V
ΔOffset/ΔV_{DD}		−1, 2	−2	+2	1, 2, 3	V_{DD} = ±5%	mW
Reference Output		−1, 2	4.99	5.01	1	V_{DD} = +12 V and +15 V	V
ΔReference/ΔV_{DD}		−1, 2		6	1	V_{DD} = ±5%	mV/V
Reference Load Sensitivity		−1, 2	−1.5	+1.5	1, 2, 3	Reference Load Current Change (0 μA–100 μA). Not Including R_{OFS} Current	mV
Digital Input High Voltage	V_{INH}	−1, 2	2.4		1, 2, 3		V
Digital Input Low Voltage	V_{INL}	−1, 2		0.8	1, 2, 3		V
Digital Input Current for Data Inputs	I_{IN}	−1, 2	−1	+1	1	V_{IN} = 0 or V_{DD}	μA
			−10	+10	2, 3		
Digital Input High for Control Inputs[4]	I_{INH}	−1, 2	−1	+1	1	V_{IN} = V_{DD}	μA
			−10	+10	2, 3		
Digital Input Low for Control Inputs	I_{INL}	−1, 2		150	1	V_{IN} = 0 V	μA
				200	2, 3		
Digital Input Capacitance	C_{IN}	−1		8	4		pF
		−2		16			
Output Range Resistors	R_{OUT}	−1, 2	15	30	1, 2, 3		kΩ
Output Ranges[5]		−1, 2	0	+5	1, 2, 3	Pin Strappable Minimum Load Resistance Is 2 kΩ to GND	V
			0	+10			
			−5	+5			
Power Supply Current	I_{DD}	−1, 2		12	1, 2, 3	Output Unloaded	mA
Output Voltage Settling Positive and Negative Full-Scale Change[6]	t_{SL}	−1, 2		10	13[7]	To ±0.5 LSB, R_L = 5 kΩ	μs

This information applies to a product under development. Its characteristics and specifications are subject to change without notice. Analog Devices assumes no obligation regarding future manufacture unless otherwise agreed to in writing.

Test	Symbol	Device	Limits Min	Limits Max	Sub Groups	Test Condition[1] ($-55°C \le T_C \le +125°C$ unless otherwise noted)	Unit
Output Voltage Slew Rate	SR	−1, 2	2		13, 14, 15[7]		V/μs
Chip Select Pulse Width	t_1	−1, 2	100		9, 10, 11		ns
Write Pulse Width	t_2	−1, 2	100		9, 10, 11		ns
Chip Select to Write Setup	t_3	−1, 2	0		9, 10, 11		ns
Chip Select to Write Hold	t_4	−1, 2	0		9, 10, 11		ns
Data Valid to Write Setup Time	t_5	−1, 2	80		9, 10, 11		ns
Data Valid to Write Hold Time	t_6	−1, 2	10		9, 10, 11		ns
Load DAC Pulse Width	t_7	−1, 2	100		9, 10, 11		ns
Clear Pulse Width	t_8	−1, 2	100		9, 10, 11		ns

NOTES
[1]Single Supply: V_{DD} = +15 V ±5%; V_{SS} = AGND = DGND = 0 V.
[2]This error is calculated with respect to the reference voltage and is measured after the offset error has been allowed for.
[3]This error is calculated with respect to an ideal 4.9988 V (on the 5 V range) or 9.9976 V (on the 10 V range). Typical full-scale temperature coefficient is ±30 ppm of FSSR/°C.
[4]Control Inputs are $\overline{CS}$, $\overline{WR}$, $\overline{LDAC}$ and $\overline{CLR}$ for Device 1 and $\overline{CSMB}$, $\overline{CSLOSB}$, $\overline{WR}$ and $\overline{LDAC}$ for Device 2.
[5]0 V to +10 V Applies toV_{DD} = +15 V ± 5% only, and V_{SS} = −15 V ± 5%.
[6]For positive full-scale change, DAC register loaded all 0s to all 1s. For negative full-scale change, DAC register loaded all 1s to all 0s.
[7]Special Subgroups 13, 14, 15 (as referenced) shall be measured only for the initial test, or after process or design changes which may affect the parameter in those subgroups. Subgroup 13 is +25°C tests, Subgroup 14 is +125°C tests and Subgroup 15 is −25°C tests.

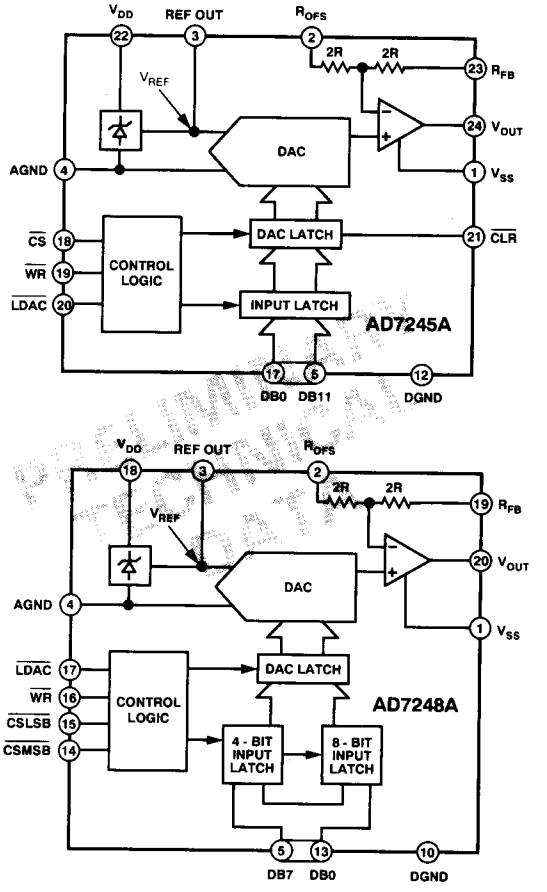
1.4 Recommended Operating Conditions.

Single Supply
- Positive Supply Voltage Range (V_{DD}) . . . . . +15 V ± 5%
- Negative Supply Voltage Range (V_{SS}) . . . . . 0 V
- AGND = DGND . . . . . 0 V

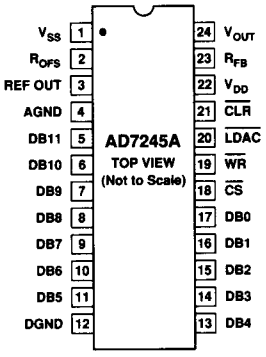
Dual Supply
- Positive Supply Voltage Range (V_{DD}) . . . . . +12 V to +15 V ± 5%
- Negative Supply Voltage Range (V_{SS}) . . . . . −12 V to −15 V +5%
- AGND = DGND . . . . . 0 V

R_L . . . . . 2 kΩ to GND
C_L . . . . . 100 pF to GND
REF OUT . . . . . Unloaded
Ambient Operating Temperature Range . . . . . −55°C to +125°C

3.2.1 Functional Block Diagram and Terminal Assignments.



Q-24



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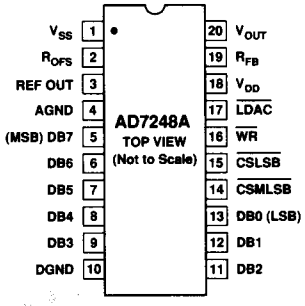
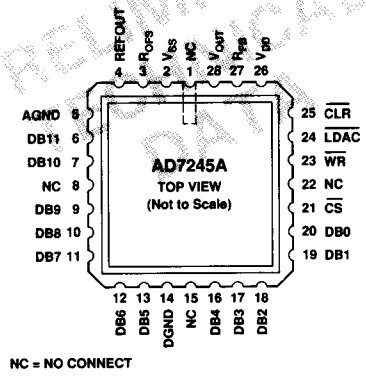


E-28A



3.2.4 Microcircuit Technology Group.

This microcircuit is covered by technology group (80).