ADVANCE

MICRON

MT5LC2568
32K x 8 SRAM

T-46-23-13

NEW 3.3 VOLT SRAM

SRAM

32K x 8 SRAM

LOW VOLTAGE

FEATURES

- High speed: 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +3.3V ±0.3V power supply
- Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ options
- All inputs and outputs are TTL compatible

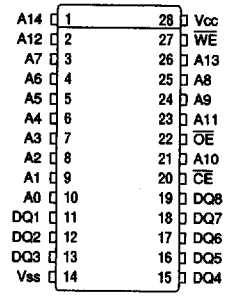
OPTIONS / MARKING

• Timing		
15ns access		-15
20ns access		-20
25ns access		-25
35ns access		-35
• Packages		
Plastic DIP (300 mil)		None
Plastic SOJ (300 mil)		DJ
Plastic ZIP (300 mil)		Z
• 2V data retention		L
• 2V data retention, low power		LP
• Temperature		
Industrial	(-40°C to +85°C)	IT
Automotive	(-40°C to +125°C)	AT
Extended	(-55°C to +125°C)	XT

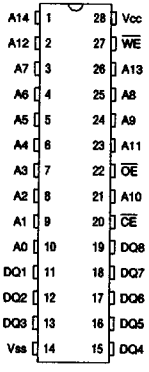
- Part Number Example: MT5LC2568Z-25 LP XT

PIN ASSIGNMENT (Top View)

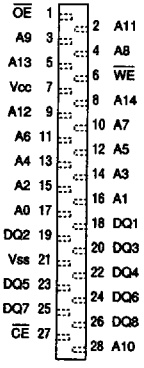
28-Pin SOJ
(SD-2)



28-Pin DIP
(SA-4)



28-Pin ZIP
(SB-1)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high-speed memory applications, Micron offers chip enable ($\overline{CE}$) and output enable ($\overline{OE}$) with this organization. These enhancements can place the outputs in High-Z for additional flexibility in system design.

Writing to these devices is accomplished when write enable ($\overline{WE}$) and $\overline{CE}$ inputs are both LOW. Reading is accomplished when $\overline{WE}$ remains HIGH and $\overline{CE}$ and $\overline{OE}$ go LOW. The device offers a reduced power standby mode when disabled. This allows system designers to meet low standby power requirements.

The "LP" version provides a reduction in both operating current (I_{CC}) and TTL standby current (I_{SB1}). The latter is achieved through the use of gated inputs on the $\overline{WE}$, $\overline{OE}$ and address lines, which also facilitates the design of battery-backed systems. That is, the gated inputs simplify the design effort and circuitry required to protect against inadvertent battery current drain during power-down, when inputs may be at undefined levels.

The MT5C2568 operates from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

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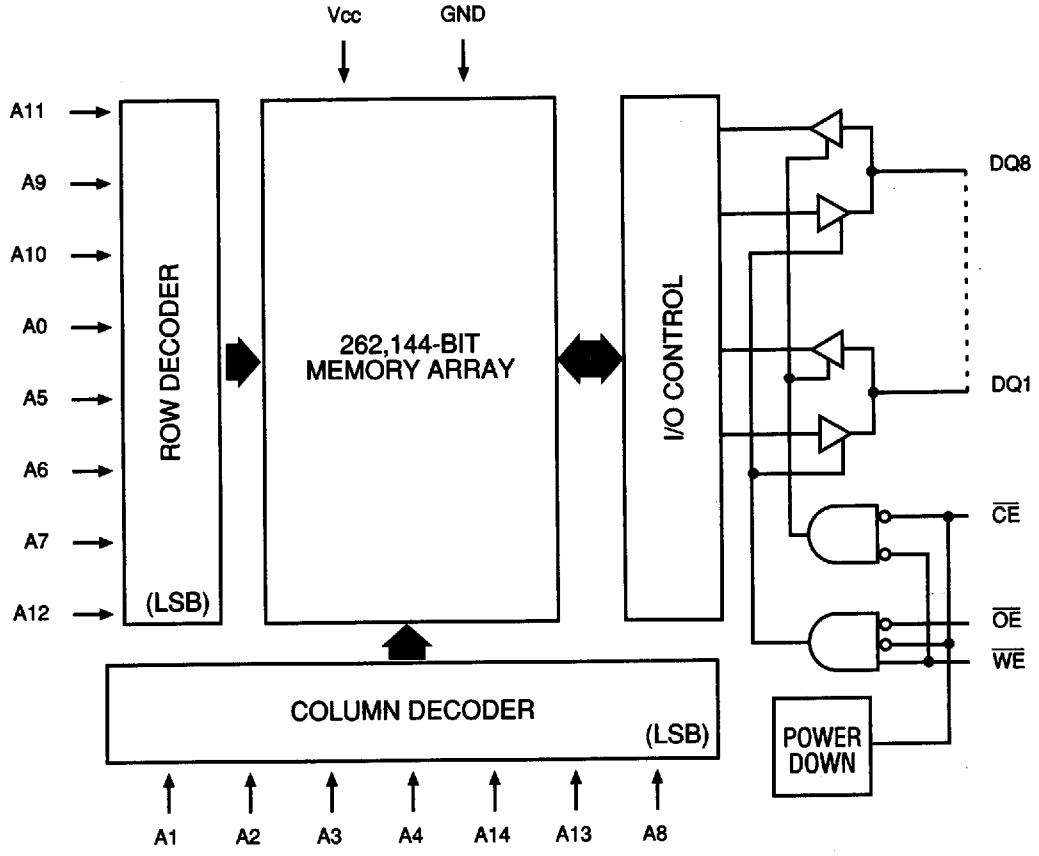
FUNCTIONAL BLOCK DIAGRAM

T-46-23-13



TRUTH TABLE

MODE	$\overline{OE}$	$\overline{CE}$	$\overline{WE}$	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
READ	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

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ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -0.5V to +4.6V
V_{IN} ..... -0.5V to V_{CC}+0.5V (+4.6V MAX)
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.0	V_{CC}+0.3	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.3	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-1	1	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-1	1	µA	
Output High Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V	1
	I_{OH} = -100µA	V_{OH}	V_{CC}-0.2		V	1
Output Low Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V	1
	I_{OL} = 100µA	V_{OL}		0.2	V	1
Supply Voltage		V_{CC}	3.0	3.6	V	1

				MAX					
DESCRIPTION	CONDITIONS	SYMBOL	VER	-15	-20	-25	-35	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}; V_{CC} = MAX Outputs Open f = MAX = 1/t_{RC}	I_{CC}	STD	55	50	45	40	mA	3, 14, 15
			LP	50	45	40	35	mA	
Power Supply Current: Standby	$\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX Outputs Open f = MAX = 1/t_{RC}	I_{SB1}	STD	15	12	8	6	mA	14, 15
			LP	500	500	500	500	µA	14, 15
	$\overline{CE}$ ≥ V_{CC} - 0.2V; V_{CC} = MAX V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ V_{SS} + 0.2V	I_{SB2}	STD	300	300	300	300	µA	14, 15
			LP	300	300	300	300	µA	14, 15

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C; f = 1 MHz	C_I	6	pF	4
Output Capacitance	V_{CC} = 3.3V	C_O	5	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; Vcc = 3.3V ±0.3V)

T-46-23-13

DESCRIPTION	SYM	-15		-20		-25		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle											
READ cycle time	t_{RC}	15		20		25		35		ns	
Address access time	t_{AA}		15		20		25		35	ns	
Chip Enable access time	t_{ACE}		15		20		25		35	ns	
Output hold from address change	t_{OH}	3		3		5		5		ns	
Chip Enable to output in Low-Z	t_{LZCE}	4		6		5		5		ns	7
Chip disable to output in High-Z	t_{HZCE}		9		9		10		15	ns	6, 7
Chip Enable to power-up time	t_{PU}	0		0		0		0		ns	
Chip disable to power-down time	t_{PD}		15		20		25		35	ns	
Output Enable access time	t_{AOE}		8		8		8		12	ns	
Output Enable to output in Low-Z	t_{LZOE}	0		0		0		0		ns	
Output disable to output in High-Z	t_{HZOE}		6		7		7		12	ns	6
WRITE Cycle											
WRITE cycle time	t_{WC}	15		20		25		35		ns	
Chip Enable to end of write	t_{CW}	10		15		15		20		ns	
Address valid to end of write	t_{AW}	10		15		15		20		ns	
Address setup time	t_{AS}	0		0		0		0		ns	
Address hold from end of write	t_{AH}	0		0		0		0		ns	
WRITE pulse width	t_{WP}	10		15		15		20		ns	
Data setup time	t_{DS}	8		10		10		15		ns	
Data hold time	t_{DH}	0		0		0		0		ns	
Write disable to output in Low-Z	t_{LZWE}	4		5		5		5		ns	7
Write Enable to output in High-Z	t_{HZWE}		8		10		10		15	ns	6,7

AC TEST CONDITIONS

Input pulse levels	Vss to 2.8V
Input rise and fall times	3ns
Input timing reference levels	1.4V
Output reference levels	1.4V
Output load	See Figures 1 and 2

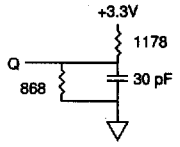

Fig. 1 OUTPUT LOAD EQUIVALENT

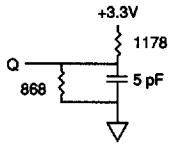

Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

1. All voltages referenced to Vss (GND).
2. -1V for pulse width < ^{t}RC/2.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^{t}HZCE, ^{t}HZOE and ^{t}HZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE and ^{t}HZWE is less than ^{t}LZWE.
8. $\overline{WE}$ is HIGH for READ cycle.
9. Device is continuously selected. All chip enables are held in their active state.
10. Address valid prior to, or coincident with, latest occurring chip enable.
11. ^{t}RC = Read Cycle Time.
12. Chip enable and write enable can initiate and terminate a WRITE cycle.
13. Refer to the IT/XT/AT section of Micron's *SRAM Data Book* for applicable non-commercial temperature range specifications.
14. Typical values are measured at 3.3V, 25°C and 20ns cycle time.
15. Vcc = MAX.

DATA RETENTION ELECTRICAL CHARACTERISTICS (L and LP Versions Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Vcc for Retention Data		V_{DR}	2			V	
Data Retention Current	$\overline{CE}$ ≥ Vcc -0.2V Other Inputs: VIN ≥ Vcc -0.2V or VIN ≤ Vss+0.2V Vcc = 2V	I_{CCDR}		TBD	50	µA	
Chip Deselect to Data Retention Time		^{t}CDR	0			ns	4
Operation Recovery Time		^{t}R	^{t}RC			ns	4, 11

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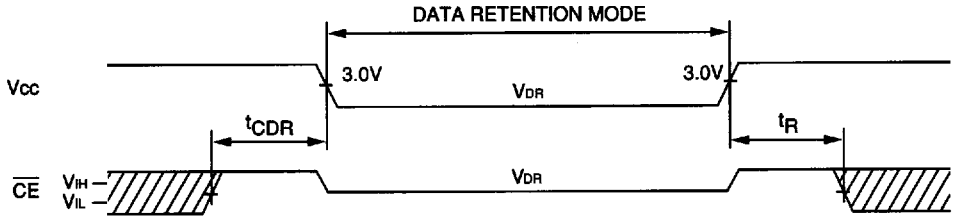
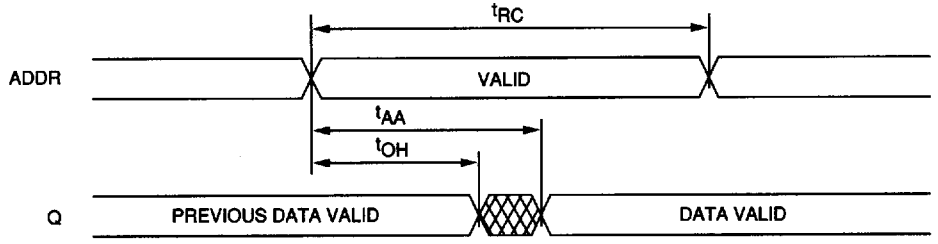
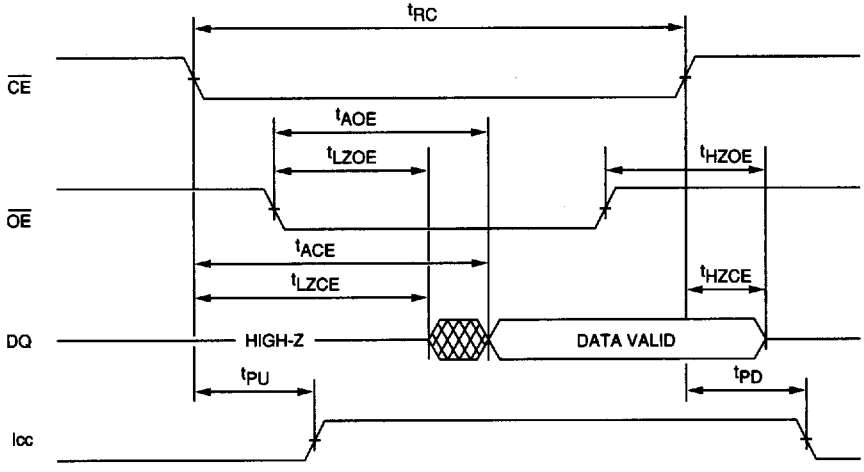
LOW Vcc DATA RETENTION WAVEFORM



READ CYCLE NO. 1 [8, 9]



READ CYCLE NO. 2 [7, 8, 10]

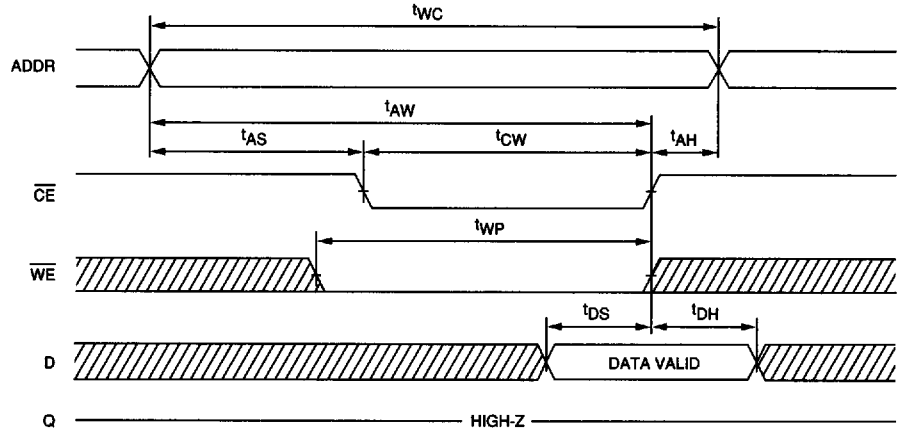


DON'T CARE

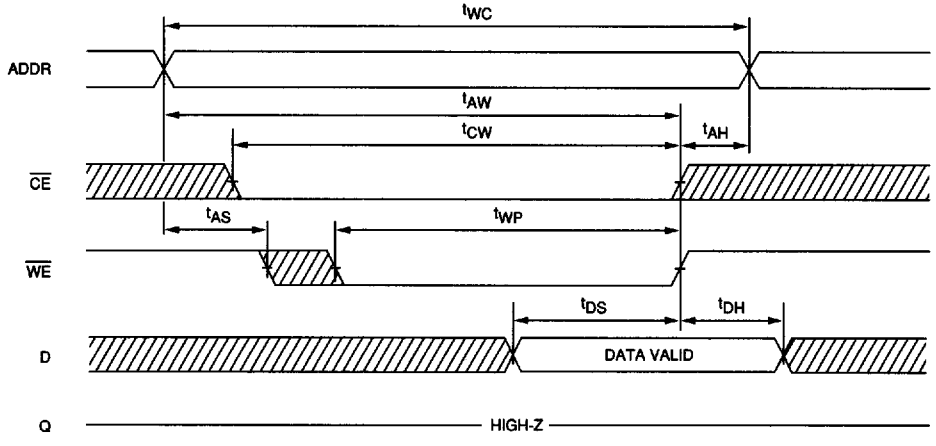
UNDEFINED

T-46-23-13

WRITE CYCLE NO. 1 [12]
(Chip Enable Controlled)



WRITE CYCLE NO. 2 [12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is inactive (HIGH).

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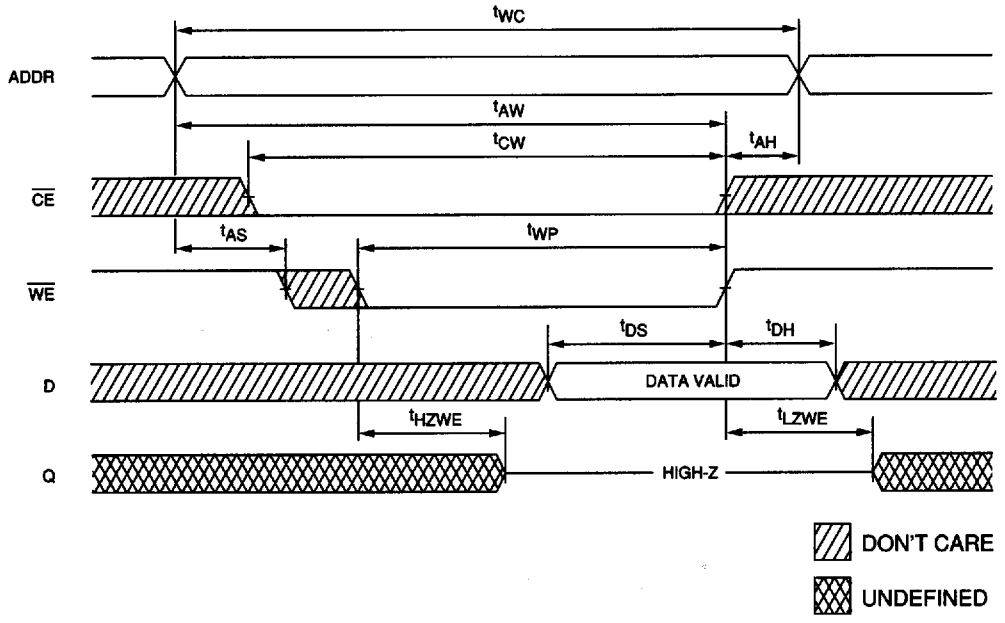
T-46-23-13

WRITE CYCLE NO. 3 [7, 12]
(Write Enable Controlled)



NOTE: Output enable ($\overline{OE}$) is active (LOW).