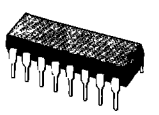
# QUAD PARALLEL REGISTER WITH ENABLE

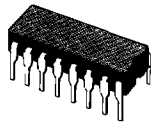
- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- BUFFERED COMMON ENABLE INPUT
- TRUE AND COMPLEMENT OUTPUT
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- FULLY TTL AND CMOS COMPATIBLE

## DESCRIPTION

The T74LS379 is a 4-Bit Register with buffered common Enable. This device is similar to the T74LS175 but feature the common Enble rather than common Master Reset.



**B1**
(Plastic Package)



**D1**
(Ceramic Package)

**M1**
(Micro Package)

**C1**
(Plastic Chip Carrier)

**ORDER CODES :**

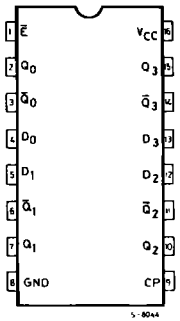
T74LS379 D1 T74LS379 C1
T74LS379 B1 T74LS379 M1

## PIN NAMES

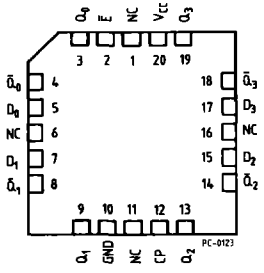
| | |
|---|---|
| $\overline{E}$ | ENABLE (active LOW) INPUT |
| $D_0$-$D_3$ | DATA INPUTS |
| CP | CLOCK (active HIGH going edge) INPUT |
| $Q_0$-$Q_3$ | TRUE OUTPUTS |
| $\overline{Q}_0$–$\overline{Q}_3$ | COMPLEMENTS OUTPUTS |

## PIN CONNECTION (top view)

DUAL IN LINE

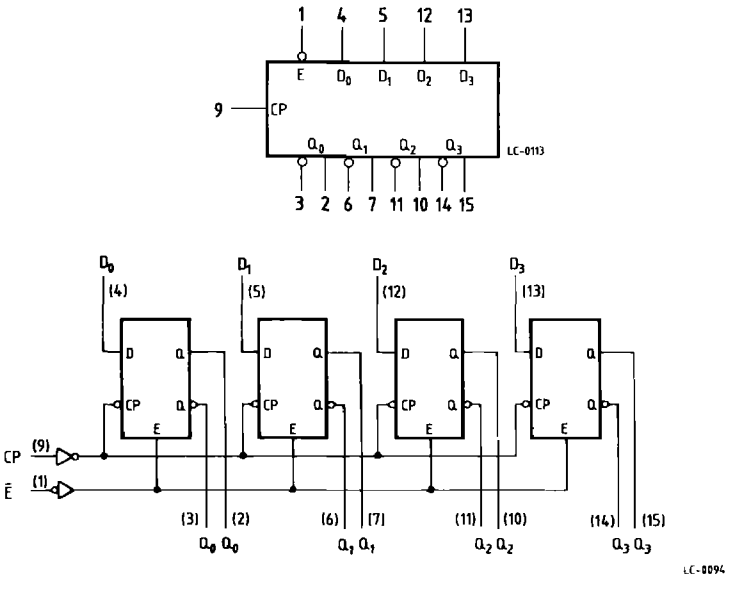



CHIP CARRIER




NC = No Internal Connection

## LOGIC SYMBOL AND LOGIC DIAGRAM




$V_{CC}$ = Pin 16
GND = Pin 8
() = Pin numbers

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Supply Voltage | – 0.5 to 7 | V |
| $V_I$ | Input Voltage, Applied to Input | – 0.5 to 15 | V |
| $V_O$ | Output Voltage, Applied to Output | – 0.5 to 10 | V |
| $I_I$ | Input Current, into Inputs | – 30 to 5 | mA |
| $I_O$ | Output Current, into Outputs | 60 | mA |

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## GUARANTEED OPERATING RANGE

| Part Numbers | Supply Voltage | | | Temperature |
|---|---|---|---|---|
| | Min. | Typ. | Max. | |
| T74LS379XX | 4.75 V | 5.0 V | 5.25 V | 0 °C to + 70 °C |

XX = package type.

## FUNCTIONAL DESCRIPTION

The LS379 consist of four edge-triggered D-type flip-flops with individual D inputs and Q outputs. The Clock (CP) and Enable ($\overline{E}$) inputs are common to all flip-flops.

When the $\overline{E}$ input is HIGH, the register will retain the present data independent of the CP input.

## TRUTH TABLE

| $\overline{E}$ | CP | $D_n$ | $Q_n$ | $\overline{Q}_n$ |
|---|---|---|---|---|
| H | ⊥⌐ | X | No change | No Change |
| L | ⊥⌐ | H | H | L |
| L | ⊥⌐ | L | L | H |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Symbol | Parameter | Limits | | | Test Condition (note 1) | | Unit |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. (*) | Max. | | | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | Guaranteed Input HIGH Voltage for All Inputs | | V |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | Guaranteed Input LOW Voltage for All Inputs | | V |
| $V_{CD}$ | Input Clamp Diode Voltage | | - 0.65 | - 1.5 | $V_{CC}$ = MIN, $I_{IN}$ = -18 mA | | V |
| $V_{OH}$ | Output HIGH Voltage | 2.7 | 3.4 | | $V_{CC}$ = MIN, $I_{OH}$ = - 400 µA<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | | V |
| $V_{OL}$ | Output LOW Voltage | | 0.25 | 0.4 | $I_{OL}$ = 4.0 mA | $V_{CC}$ = MIN, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table | V |
| | | | 0.35 | 0.5 | $I_{OL}$ = 8.0 mA | | V |
| $I_{IH}$ | Input HIGH Current | | | 20 | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V | | µA |
| | Input HIGH Current at MAX Input Voltage E, $D_0$-$D_3$, CP | | | 0.1 | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V | | mA |
| $I_{IL}$ | Input LOW Current E, $D_0$-$D_3$, CP | | | - 0.4 | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V | | mA |
| $I_{OS}$ | Output Short Circuit Current (note 2) | - 20 | | - 100 | $V_{CC}$ = MAX, $V_{OUT}$ = 0 V | | mA |
| $I_{CC}$ | Power Supply Current | | 11 | 16 | $V_{CC}$ = MAX | | mA |

**Notes :** 1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2 Not more than one output should be shorted at a time.
(*) Typical values are at $V_{CC}$ = 5.0 V, $T_A$ = 25 °C.

## AC CHARACTERISTICS : $T_A$ = 25 °C

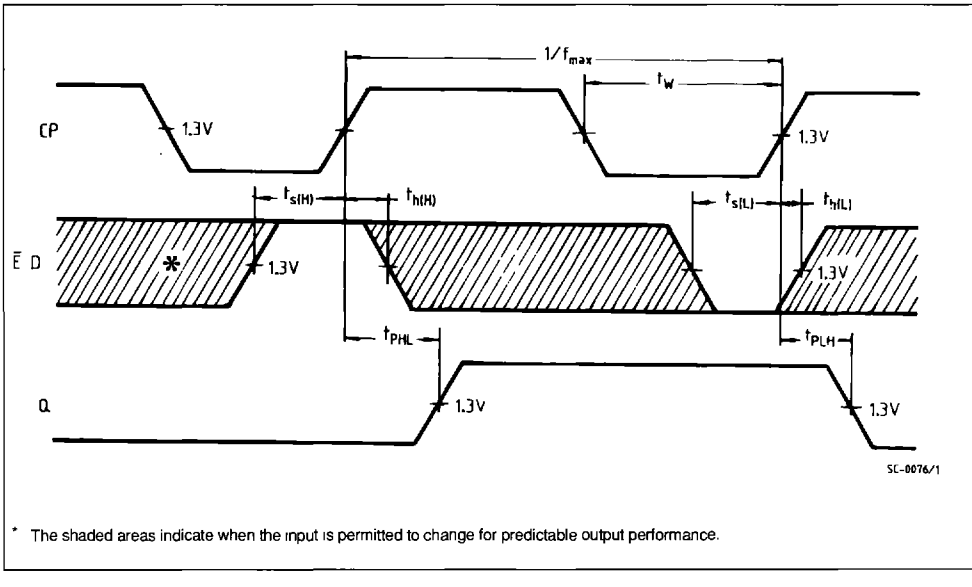
| Symbol | Parameter | Limits | | | Test Conditions | | Unit |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| $t_{PLH}$ | CP to Output | | 17 | 27 | Fig. 1 | $V_{CC}$ = 5.0 V<br>$C_L$ = 15 pF | ns |
| $t_{PHL}$ | CP to Output | | 18 | 27 | | | ns |
| $f_{MAX}$ | Maximum Clock Frequency | 30 | 40 | | | | MHz |

## AC SET-UP REQUIREMENTS : $T_A = 25\ ^\circ C$

| Symbol | Parameter | Limits | | | Test Conditions | | Unit |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| $t_s$ | Set-up Time, Data to Clock (HIGH or LOW) | 20 | | | Fig. 1 | $V_{CC} = 5.0$ V | ns |
| $t_h$ | Hold Time, Data to Clock (HIGH or LOW) | 5 | | | Fig. 1 | | ns |
| $t_s$ | Set-up Time, Enable to Clock | 30 | | | Fig. 1 | | ns |
| $t_h$ | Hold Time, Enable to Clock | 5 | | | Fig. 1 | | ns |
| $t_{WCP}$ | Minimum Clock Pulse Width | 17 | 10 | | | | ns |

## AC WAVEFORMS

**Figure 1 : Clock to Output Delays, Clock Pulse Width, Frequency, Set-up and Hold Times Data, Enable to Clock.**




* The shaded areas indicate when the input is permitted to change for predictable output performance.

**DEFINITION OF TERMS :**

SET-UP TIME (ts)- is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD-TIME (th)- is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition.A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.