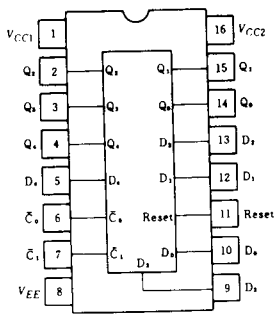
Quintuple Latches

The HD10175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latches on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.

■PIN ARRANGEMENT



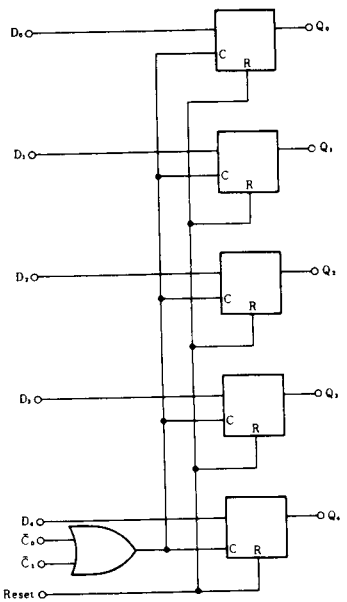
(Top View)

■FUNCTION TABLE

D	$\overline{C_0}$	$\overline{C_1}$	Reset	Q_{n+1}
L	L	L	L	L
H	L	L	L	H
×	H	×	L	Q_n
×	×	H	L	Q_n
×	H	×	H	L
×	×	H	H	L

× : Don't Care

■BLOCK DIAGRAM



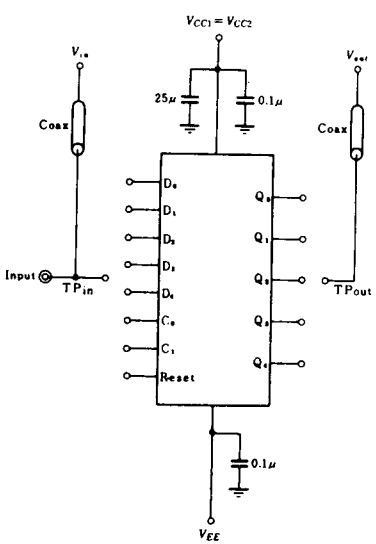
■DC CHARACTERISTICS ($V_{EE}=-5.2V$, $Ta=-30\sim+85°C$)

Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	78	97	mA
Input Current	I_{IH}	$V_{IH}=-0.810V$	Clock, Data	25°C	—	—	290	μA
			Reset		—	—	650	
	I_{IL}	$V_{IL}=-1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH}=-0.890V$, $V_{IL}=-1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH}=-0.810V$, $V_{IL}=-1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH}=-0.700V$, $V_{IL}=-1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL}=-1.890V$, $V_{IH}=-0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL}=-1.850V$, $V_{IH}=-0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL}=-1.825V$, $V_{IH}=-0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA}=-1.205V$		−30°C	−1.080	—	—	V
		$V_{IHA}=-1.105V$		25°C	−0.980	—	—	
		$V_{IHA}=-1.035V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA}=-1.500V$		−30°C	—	—	−1.655	V
		$V_{ILA}=-1.475V$		25°C	—	—	−1.630	
		$V_{ILA}=-1.440V$		85°C	—	—	−1.595	

■AC CHARACTERISTICS ($V_{EE}=-3.2V$, $V_{CC}=+2.0V$, $Ta=-30\sim+85°C$)

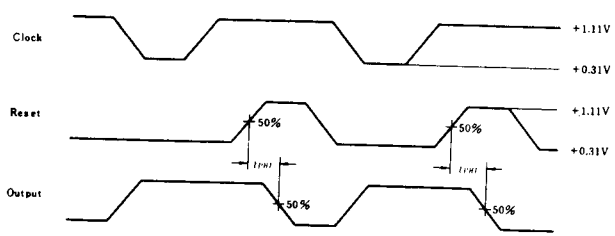
Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	Data	Q	$R_L=50\Omega$	−30°C	1.0	—	3.6	ns
					25°C	1.0	—	3.5	
					85°C	1.0	—	3.6	
	t_{PHL}				−30°C	1.0	—	3.6	ns
					25°C	1.0	—	3.5	
					85°C	1.0	—	3.6	
	t_{PLH}	Clock	Q		−30°C	1.0	—	4.7	ns
					25°C	1.0	—	4.3	
					85°C	1.0	—	4.4	
	t_{PHL}				−30°C	1.0	—	4.7	ns
					25°C	1.0	—	4.3	
					85°C	1.0	—	4.4	
	t_{PHL}	Reset	Q		−30°C	0.9	—	4.0	ns
					25°C	1.0	—	3.9	
					85°C	1.0	—	4.2	
Setup Time	t_{su}	D → C	Q		25°C	—	—	2.5	ns
Hold Time	t_h				25°C	—	—	1.5	ns
Rise/Fall Time	t_{TLH}		Q		−30°C	1.0	—	3.6	ns
					25°C	1.1	—	3.5	
					85°C	1.1	—	3.7	
	t_{THL}				−30°C	1.0	—	3.6	ns
					25°C	1.1	—	3.5	
					85°C	1.1	—	3.7	

■SWITCHING TIME TEST CIRCUIT

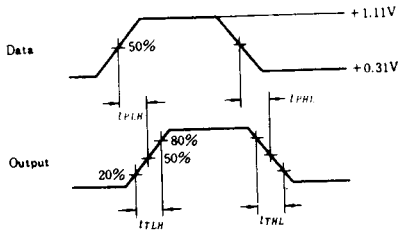


Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. Unused outputs connected to a 50Ω resistor to ground.

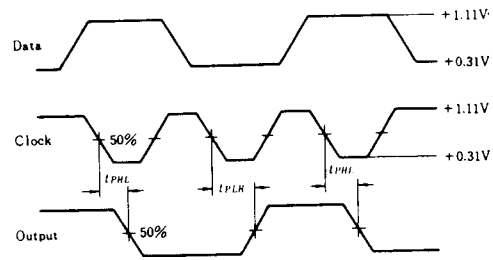
1. Reset



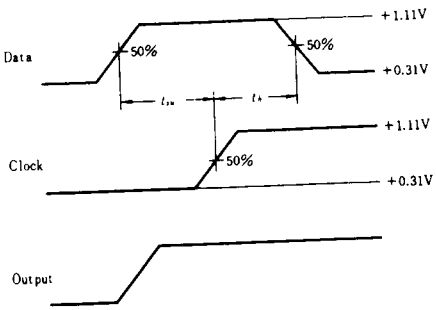
2. Data



3. Clock



4. Setup and Hold



Notes) 1. t_{su} is minimum time before the positive transition of the clock pulse that information must be present at the data.
2. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at the data.