Rochester Electronics

Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
    - Class Q Military
    - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

    - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

MC74AC573, MC74ACT573

Octal Buffer/Line Driver with 3-State Outputs

The MC74AC573/74ACT573 is a high−speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The MC74AC573/74ACT573 is functionally identical to the MC74AC373/74ACT373 but has inputs and outputs on opposite sides.

- Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors
- Useful as Input or Output Port for Microprocessors
- Functionally Identical to MC74AC373/74ACT373
- 3−State Outputs for Bus Interfacing
- Outputs Source/Sink 24 mA
- ′ACT573 Has TTL Compatible Inputs

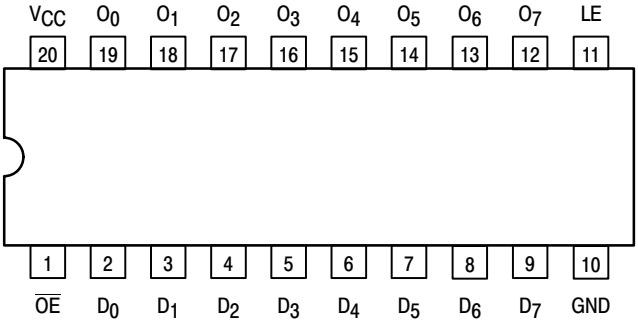


Figure 1. Pinout 20−Lead Packages Conductors
(Top View)

PIN ASSIGNMENT

PIN	FUNCTION
D_0−D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3−State Output Enable Input
O_0−O_7	3−State Latch Outputs

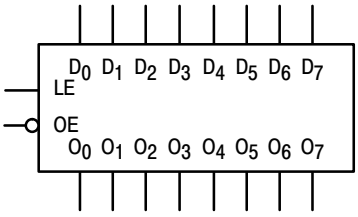
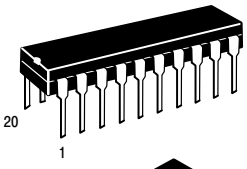


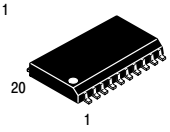
Figure 2. Logic Symbol

ON Semiconductor™

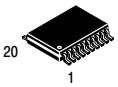
http://onsemi.com



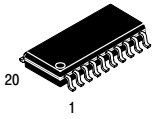
PDIP−20
N SUFFIX
CASE 738



SO−20
DW SUFFIX
CASE 751



TSSOP−20
DT SUFFIX
CASE 948E



EIAJ−20
M SUFFIX
CASE 967

ORDERING INFORMATION

Device	Package	Shipping
MC74AC573N	PDIP−20	18 Units/Rail
MC74ACT573N	PDIP−20	18 Units/Rail
MC74AC573DW	SOIC−20	38 Units/Rail
MC74AC573DWR2	SOIC−20	1000 Tape & Reel
MC74ACT573DW	SOIC−20	38 Units/Rail
MC74ACT573DWR2	SOIC−20	1000 Tape & Reel
MC74AC573DT	TSSOP−20	75 Units/Rail
MC74AC573DTR2	TSSOP−20	2500 Tape & Reel
MC74ACT573DT	TSSOP−20	75 Units/Rail
MC74ACT573DTR2	TSSOP−20	2500 Tape & Reel
MC74AC573M	EIAJ−20	40 Units/Rail
MC74AC573MEL	EIAJ−20	2000 Tape & Reel
MC74ACT573M	EIAJ−20	40 Units/Rail
MC74ACT573MEL	EIAJ−20	2000 Tape & Reel

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 231 of this data sheet.

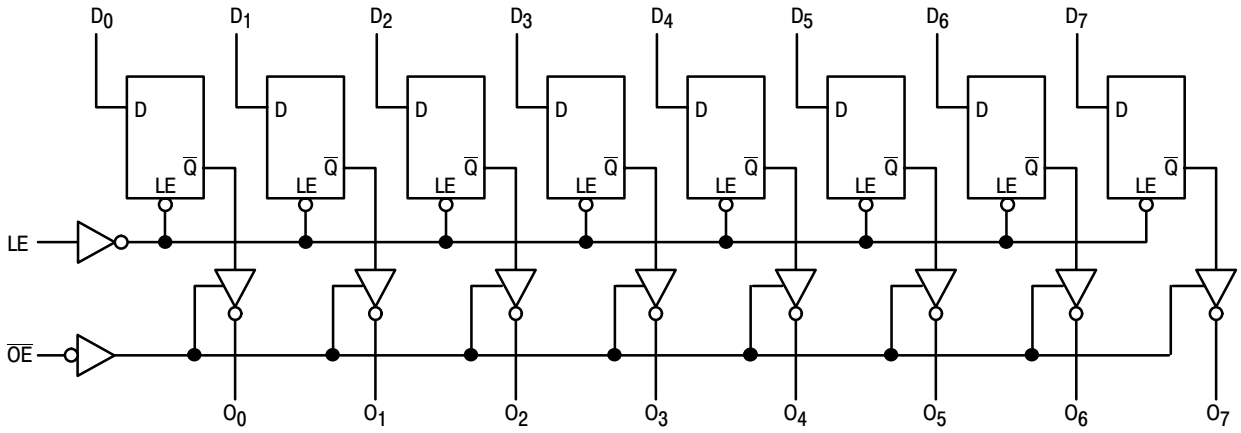
TRUTH TABLE

Inputs			Outputs
$\overline{OE}$	LE	D_n	O_n
L	H	H	H
L	H	L	H
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before LOW−to−HIGH Transition of Clock

FUNCTIONAL DESCRIPTION

The MC74AC573/74ACT574 contains eight D−type latches with 3−state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH−to−LOW transition of LE. The 3−state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.



NOTE: That this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	−0.5 to +7.0	V
V_{IN}	DC Input Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	−0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±20	mA
I_{OUT}	DC Output Sink/Source Current, per Pin	±50	mA
I_{CC}	DC V_{CC} or GND Current per Output Pin	±50	mA
T_{stg}	Storage Temperature	−65 to +150	°C

*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	′AC	2.0	5.0	6.0	V
		′ACT	4.5	5.0	5.5	
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)		0	−	V_{CC}	V
t_r, t_f	Input Rise and Fall Time (Note 1) ′AC Devices except Schmitt Inputs	V_{CC} @ 3.0 V	−	150	−	ns/V
		V_{CC} @ 4.5 V	−	40	−	
		V_{CC} @ 5.5 V	−	25	−	
t_r, t_f	Input Rise and Fall Time (Note 2) ′ACT Devices except Schmitt Inputs	V_{CC} @ 4.5 V	−	10	−	ns/V
		V_{CC} @ 5.5 V	−	8.0	−	
T_J	Junction Temperature (PDIP)		−	−	140	°C
T_A	Operating Ambient Temperature Range		−40	25	85	°C
I_{OH}	Output Current − High		−	−	−24	mA
I_{OL}	Output Current − Low		−	−	24	mA

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74AC		74AC	Unit	Conditions
			T_A = +25°C		T_A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	2.1 3.15 3.85	2.1 3.15 3.85	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	3.0 4.5 5.5	1.5 2.25 2.75	0.9 1.35 1.65	0.9 1.35 1.65	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	3.0 4.5 5.5	2.99 4.49 5.49	2.9 4.4 5.4	2.9 4.4 5.4	V	I_{OUT} = −50 μA
		3.0 4.5 5.5	− − −	2.56 3.86 4.86	2.46 3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} −12 mA I_{OH} −24 mA −24 mA
V_{OL}	Maximum Low Level Output Voltage	3.0 4.5 5.5	0.002 0.001 0.001	0.1 0.1 0.1	0.1 0.1 0.1	V	I_{OUT} = 50 μA
		3.0 4.5 5.5	− − −	0.36 0.36 0.36	0.44 0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} 12 mA I_{OL} 24 mA 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OZ}	Maximum 3−State Current	5.5	−	±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	−	−	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	−	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3)

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF			74AC T_A = −40°C to +85°C, C_L = 50 pF		Unit	Fig. No.
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0	2.5 2.5	− −	13.0 10.0	2.0 2.0	15.0 11.5	ns	3−5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0	2.5 2.5	− −	12.0 9.5	2.0 2.0	14.0 11.0	ns	3−5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0	2.5 2.5	− −	13.0 9.5	2.0 2.0	15.0 11.0	ns	3−6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0	2.5 2.5	− −	12.0 8.5	2.0 2.0	14.0 10.0	ns	3−6
t_{PZH}	Output Enable Time	3.3 5.0	2.5 2.5	− −	11.0 9.0	2.0 2.0	12.0 10.0	ns	3−7
t_{PZL}	Output Enable Time	3.3 5.0	2.5 2.5	− −	11.0 8.5	2.0 2.0	12.5 9.5	ns	3−8
t_{PHZ}	Output Disable Time	3.3 5.0	2.5 2.5	− −	12.5 11.0	2.0 2.0	13.5 12.0	ns	3−7
t_{PLZ}	Output Disable Time	3.3 5.0	2.5 2.5	− −	9.5 8.0	2.0 2.0	10.5 9.0	ns	3−8

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74AC T_A = +25°C, C_L = 50 pF		74AC T_A = −40°C to +85°C, C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	− −	3.5 3.0	4.0 3.5	ns	3−9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	− −	2.0 2.0	2.0 2.0	ns	3−9
t_w	LE Pulse Width, HIGH	3.3 5.0	− −	6.0 4.0	7.0 5.0	ns	3−6

*Voltage Range 3.3 V is 3.3 V ±0.3 V.
Voltage Range 5.0 V is 5.0 V ±0.5 V.

DC CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	74ACT		74ACT	Unit	Conditions
			T_A = +25°C		T_A = −40°C to +85°C		
			Typ	Guaranteed Limits			
V_{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	V	V_{OUT} = 0.1 V or V_{CC} − 0.1 V
V_{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V	I_{OUT} = −50 μA
		4.5 5.5	− −	3.86 4.86	3.76 4.76	V	*V_{IN} = V_{IL} or V_{IH} I_{OH} −24 mA I_{OH} −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	I_{OUT} = 50 μA
		4.5 5.5	− −	0.36 0.36	0.44 0.44	V	*V_{IN} = V_{IL} or V_{IH} I_{OL} 24 mA I_{OL} 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	−	±0.1	±1.0	μA	V_I = V_{CC}, GND
ΔI_{CCT}	Additional Max. I_{CC}/Input	5.5	0.6	−	1.5	mA	V_I = V_{CC} − 2.1 V
I_{OZ}	Maximum 3-State Current	5.5	−	±0.5	±5.0	μA	V_I (OE) = V_{IL}, V_{IH} V_I = V_{CC}, GND V_O = V_{CC}, GND
I_{OLD}	†Minimum Dynamic Output Current	5.5	−	−	75	mA	V_{OLD} = 1.65 V Max
I_{OHD}		5.5	−	−	−75	mA	V_{OHD} = 3.85 V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	−	8.0	80	μA	V_{IN} = V_{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.
†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS (For Figures and Waveforms − See Section 3)

Symbol	Parameter	V_{CC}* (V)	74ACT			74ACT		Unit	Fig. No.
			T_A = +25°C C_L = 50 pF			T_A = −40°C to +85°C C_L = 50 pF			
			Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0	2.5	−	10.5	2.0	12	ns	3−5
t_{PHL}	Propagation Delay D_n to O_n	5.0	2.5	−	10.5	2.0	12	ns	3−5
t_{PLH}	Propagation Delay LE to O_n	5.0	3.0	−	10.5	2.5	12	ns	3−6
t_{PHL}	Propagation Delay LE to O_n	5.0	2.5	−	9.5	2.0	10.5	ns	3−6
t_{PZH}	Output Enable Time	5.0	2.0	−	10	1.5	11	ns	3−7
t_{PZL}	Output Enable Time	5.0	1.5	−	9.5	1.5	10.5	ns	3−8
t_{PHZ}	Output Disable Time	5.0	2.5	−	11	1.5	12.5	ns	3−7
t_{PLZ}	Output Disable Time	5.0	1.5	−	8.5	1.0	9.5	ns	3−8

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC}* (V)	74ACT T_A = +25°C C_L = 50 pF		74ACT T_A = −40°C to +85°C C_L = 50 pF	Unit	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	−	3.0	3.5	ns	3−9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	−	0	0	ns	3−9
t_w	LE Pulse Width, HIGH	5.0	−	3.5	4.0	ns	3−6

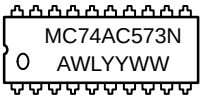
*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 5.0 V
C_{PD}	Power Dissipation Capacitance	25	pF	V_{CC} = 5.0 V

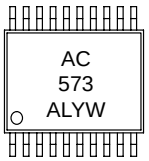
MARKING DIAGRAMS

PDIP−20

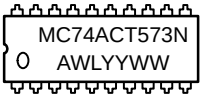


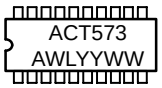
SO−20

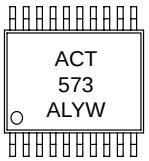
TSSOP−20



EIAJ−20







A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week