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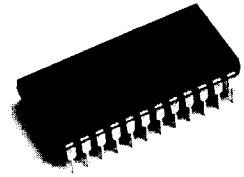


DAC65

AVAILABLE IN DIE

12-Bit High Speed DIGITAL-TO-ANALOG CONVERTER

FEATURES

- FAST SETTLING: 35ns
- INTEGRAL LINEARITY ERROR: ±0.25LSB
- DIFFERENTIAL LINEARITY ERROR: ±0.25LSB
- HIGH SPECTRAL PURITY: –70dBc, f_o = 1MHz
- INTERNAL REFERENCE
- 24-PIN PLASTIC DIP PACKAGE

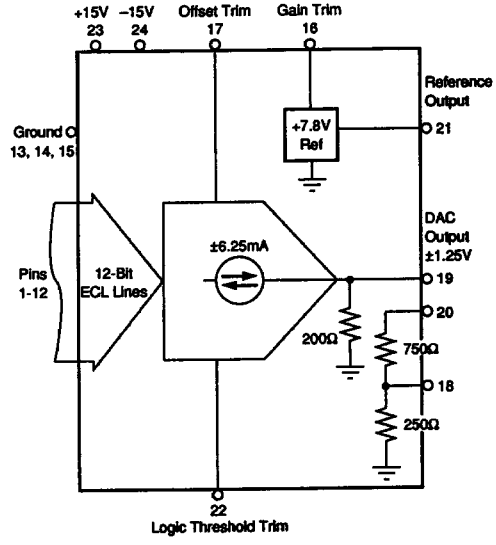
APPLICATIONS

- DIRECT DIGITAL FREQUENCY SYNTHESIZERS
- FAST ATE SYSTEMS
- ARBITRARY WAVEFORM GENERATORS
- HIGH-RESOLUTION VIDEO GRAPHICS
- DIGITAL-TO-ANALOG RECONSTRUCTION
- SPREAD SPECTRUM LOCAL OSCILLATOR

DESCRIPTION

The DAC65 is a fast-settling monolithic 12-bit digital-to-analog converter. OFF-chip bypass capacitors are included in the package for higher performance and user convenience. Excellent linearity and accuracy are achieved with laser-trimmed thin film nichrome resistors. The DAC features bipolar output voltage or current and internal voltage reference. The internal precision resistor network can be used with an external op amp to give an output greater than ±1.25V.

Low harmonic distortion and spurious products together with a low quantizing noise floor make the DAC65 an excellent choice for direct digital frequency synthesizer applications. High accuracy and low gain drift allow its use in precision high-speed test equipment designs. Low-noise ECL logic is used to preserve clean analog output spectral performance.



International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (602) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (602) 889-1510 • Immediate Product Info: (800) 548-6132

SPECIFICATIONS

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = ±15V, and 5-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	DAC65JP MIN	DAC65JP TYP	DAC65JP MAX	DAC65KP MIN	DAC65KP TYP	DAC65KP MAX	UNITS
DIGITAL INPUTS								
Logic	12 Parallel Input Lines			ECL Compatible				
Resolution			12			•		Bits
ECL Logic Input Levels[1]: V_{IL}	Logic "0"	–0.81	–0.9	–0.98	•	•	•	V
I_{IL}		0.5	1.2	2	•	•	•	mA
V_{IH}	Logic "1"	–1.95	–1.79	–1.63	•	•	•	V
I_{IH}		0.5	1.2	2	•	•	•	mA
Logic Threshold: Voltage		–1.2	–1.3	–1.4	•	•	•	V
Current		1.5	2.3	3.2	•	•	•	mA
ANALOG OUTPUT								
Bipolar Output Current[2]	R_L = 0Ω		±6.25			•		mA
Bipolar Output Voltage[2]	R_L = ∞		±1.25			•		V
Output Resistance			200			•		Ω
Output Capacitance			3			•		pF
Internal Resistors: R_1	Pin 18 to Pin 20		750			•		Ω
R_2	Pin 18 to Pin 15		250			•		Ω
Ratio Accuracy	R_1/R_2		±0.05	±0.25		•	•	%
Absolute Accuracy	R_1, R_2		±0.25	±0.5		•	•	%
Output Noise	Static, All Bits On, BW = 10MHz		10			•		µVrms
TRANSFER CHARACTERISTICS								
Integral Linearity Error	V_O = ±1.25V		±0.25	±0.75		•	±0.5	LSB
			±0.006	±0.018		•	±0.012	% of FSR[3]
Differential Linearity Error	V_O = ±1.25V		±0.25	±0.75		•	±0.55	LSB
			±0.006	±0.018		•	±0.012	% of FSR
Bipolar Gain Error[4]	V_O = ±1.25V		±0.1	±0.25		•	•	%FSR
Trim Range	R_{TRIM} = 10kΩ		±5			•		mV
Bipolar Offset Error[4]	V_O = ±1.25V		±0.1	±0.15		•	•	%FSR
Trim Range	R_{TRIM} = 10kΩ		±3			•		mV
Monotonic	12 Bit		Guaranteed			Guaranteed		
Power Supply Rejection	Δ ±V_{CC} = ±14V to ±16V		±0.0012	±0.1		•	•	%FSR/%V_{CC}
SETTLING TIME								
Voltage Output:	R_L = 200Ω (Internal)							
1LSB Change	Settling to ±0.024% FSR		30	40		•	35	ns
Full Scale Change	Settling to ±1% FSR		17			•		ns
	±0.1% FSR		23			•		ns
	±0.024% FSR		30			•		ns
	±0.012% FSR		35			•		ns
Glitch Energy[5]	Major Carry		250			•		LSB-ns
REFERENCE								
Reference Output Voltage	No External Load	+7	+7.8	+8.6	•	•	•	V
Reference Temperature Drift	T_{MIN} to T_{MAX}		±40			•		ppm/°C
DYNAMIC PERFORMANCE[6]								
Spurious Free Dynamic Range	f_{CLOCK} = 20MHz							
f_C = 100kHz			–73			•		dBc
f_C = 1MHz			–70			•		dBc
f_C = 5MHz			–66			•		dBc
f_C = 100kHz	f_{CLOCK} = 35MHz		–71			•		dBc
f_C = 1MHz			–68			•		dBc
f_C = 5MHz			–61			•		dBc
Total Harmonic Distortion (THD)	f_{CLOCK} = 20MHz							
f_C = 1MHz			–68			•		dBc
Signal-to-Noise Ratio (SNR)	f_{CLOCK} = 20MHz							
f_C = 1MHz	BW = 10MHz		–70			•		dBc
Temperature DRIFT								
Bipolar Gain	T_{MIN} to T_{MAX}		±20	±40		•	•	ppm FSR/°C
Bipolar Offset	T_{MIN} to T_{MAX}		±10	±15		•	•	ppm FSR/°C
Integral Linearity Error	T_{MIN} to T_{MAX}		±0.5	±1		•	±0.75	LSB
			±0.012	±0.024		•	±0.018	% of FSR
Differential Linearity Error	T_{MIN} to T_{MAX}		±0.8	±1		•	±0.75	LSB
			±0.019	±0.024		•	±0.018	% of FSR
Ratio Accuracy, Internal R_1 and R_2	T_{MIN} to T_{MAX}		±20			•		ppm/°C
POWER SUPPLIES								
Rated Voltage	±V_{CC}		±15			•		V
Derated Performance	±V_{CC}	±13		±16	•		•	V
Current Quiescent: $+I_{CC}$	V_O = + Full Scale		+24	+30		•	•	mA
$-I_{CC}$	V_O = + Full Scale		–54	–65		•	•	mA
Power Dissipation	V_O = + Full Scale		1.2	1.43		•	•	W

SPECIFICATIONS (CONT)

ELECTRICAL

T_A = +25°C, $\pm V_{CC}$ = ±15V, and 5-minute warm-up in a normal convection environment unless otherwise noted.

PARAMETER	CONDITIONS	DAC65JP			DAC65KP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TEMPERATURE RANGE								
Specification	Ambient Temperature	0		+70	*		*	°C
Operating	Ambient Temperature	–40		+85	*		*	°C
θ_{JA} (7)			40			*		°C/W

* Same specification as for DAC65JP.

NOTES: (1) Logic input voltages and currents are dependent on the logic threshold voltage. The logic input values given in each column are correct for the logic threshold voltage given in that column. (2) The DAC65 is internally trimmed for ±1.25V output. The accuracy of ±6.25mA is about ±30% and its drift is about the same as the voltage output. (3) FSR is Full Scale Range, which is ±1.25V or 2.5V total. (4) Offset error is measured with all bits off (positive full scale = +1.25V) and is calculated as a percent of FSR = 2.5V. (5) Refer to Output Glitch section. (6) Measured in direct digital synthesizer (see Figure 9, application section). (7) Thermal resistance depends on many factors, such as whether or not DAC65 is mounted directly to a ground plane, how it is placed on the PC board, or if forced air cooling is used. (8) Specifications were characterized at +25°C and over temperature with an air flow of 8 cu ft/min.

ORDERING INFORMATION

MODEL	PACKAGE	TEMPERATURE RANGE
DAC65JP	24-Pin Plastic DIP	0°C to +70°C
DAC65KP	24-Pin Plastic DIP	0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

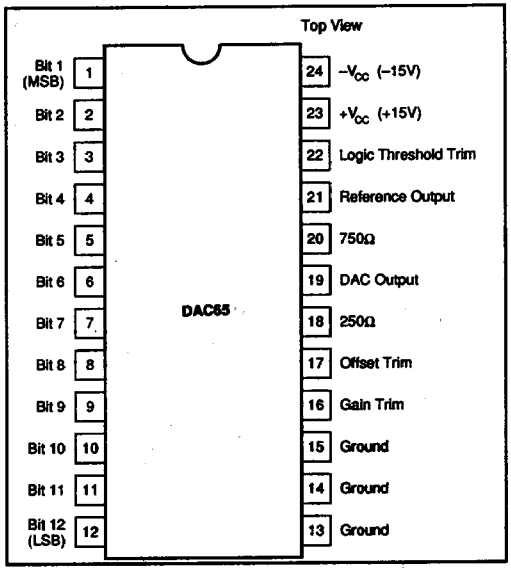
$\pm V_{CC}$	±18V
Logic Input	0V to –5.2V
Case Temperature	–40°C to +85°C
Junction Temperature	+150°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

Stresses above these ratings may permanently damage the device.

ELECTROSTATIC DISCHARGE SENSITIVITY

Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that this integrated circuit be handled and stored using appropriate ESD protection methods.

PIN CONFIGURATION

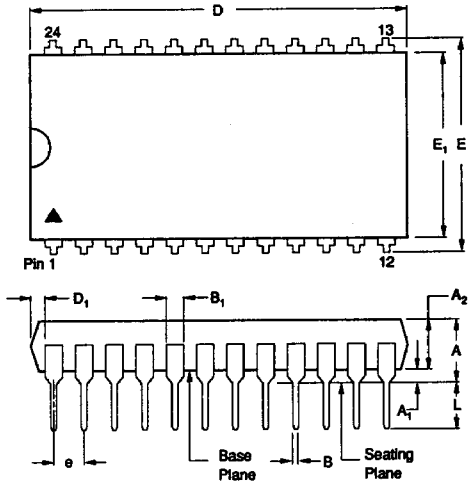


PIN DEFINITIONS

PIN NO	DESIGNATION	DESCRIPTION
1-12	ECL Data Input	12 parallel input data lines, ECL compatible.
13,14,15	Grounds	
16	Gain Trim	Input for externally adjusting gain error.
17	Offset Trim	Input for externally adjusting offset error.
18	250Ω	Internal resistor ratio matched to an internal 750Ω resistor for amplifying DAC output voltage with an external op amp.
19	DAC Output	DAC output voltage of ±1.25V or output current of ±6.25mA.
20	750Ω	Internal resistor ratio matched to an internal 250Ω resistor for amplifying DAC output voltage with an external op amp.
21	Reference Out	Reference output voltage of +7.8V.
22	Logic Threshold Trim	Input voltage for adjusting logic threshold.
23	$+V_{CC}$	Plus power supply, +15V.
24	$-V_{CC}$	Minus power supply, –15V.

MECHANICAL

P Package — 24-Pin Plastic, Double-Wide DIP



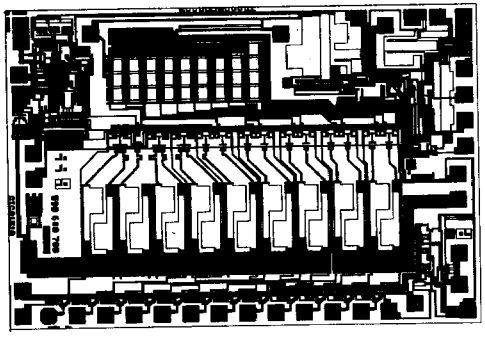
DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.155	.250	3.94	6.35
A_1	.015	.070	.381	1.78
A_2	.140	.185	3.57	4.70
B	.014	.022	.356	.559
B_1	.040	.070	1.02	1.78
C	.008	.015	.20	.381
D	1.235	1.265	31.37	32.13
D_1	.040	.100	1.020	2.540
E	.600	.625	15.24	15.88
E_1	.525	.565	13.34	14.35

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
e	.100 BASIC		2.54 BASIC	
eA	.600 BASIC		15.24 BASIC	
eB	.600	.700	15.24	17.78
L	.115	.200	2.91	5.08

NOTES:
(1) Not JEDEC Standard.
(2) Controlling dimension: INCH.
(3) Dimensioning and tolerancing per ANSI Y14.5M-1982.
(4) Dimensions A, A_1 and L are measured with package seated in JEDEC Seating Plane Gauge GS-3.
(5) D and E_1 does not include mold flash. Mold flash shall not exceed .010 inches, 0.25mm.
(6) eB and eC are measured at the lead tips with the leads unconstrained. eC must be zero or greater.

NOTE: Leads in true position within 0.01" (0.25mm) R at MMC at seating plane.

DICE INFORMATION



DAC65 DIE TOPOGRAPHY

PAD	FUNCTION	PAD	FUNCTION
1	Bit 1	20	Reference Filter
2	Bit 2	21	NC
3	Bit 3	22	NC
4	Bit 4	23	Gain Trim
5	Bit 5	24	Ground (Reference)
6	Bit 6	25	Ground (Power)
7	Bit 7	26	Reference Out
8	Bit 8	27	NC
9	Bit 9	28	$+V_{CC}$
10	Bit 10	29	Offset Trim
11	Bit 11	30	Ground (Analog)
12	Bit 12	31	DAC Output
13	Logic Bypass Cap	32	Ground (Op Amp)
14	$-V_{CC}$ (Logic)	33	Op Amp Compensation
15	Ground (Digital)		
16	Threshold Trim (Logic Low)	34	I_{SWITCH} Threshold Bypass
17	Threshold Trim (Logic High)	35	NC
		36	$-V_{CC}$ (Analog)
18	$-V_{CC}$ (Analog)	37	$-V_{CC}$ (Logic)
19	NC	38	NC

NC: Do not connect. Ground: All ground connections should be returned to a ground plane. VCC: All supplies should be bypassed using good high frequency techniques.

MECHANICAL INFORMATION

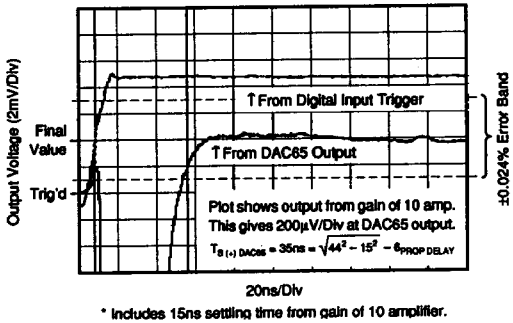
	MILS (0.001")	MILLIMETERS
Die Size	150 x 103 ±5	—
Die Thickness	20 ±3	—
Min. Pad Size	5 x 5	—
Backing	Gold	

See "DICE PRODUCTS" Section 17 in Data Book Supplement Volume 33c, or contact Burr-Brown for current information.

TYPICAL PERFORMANCE CURVES

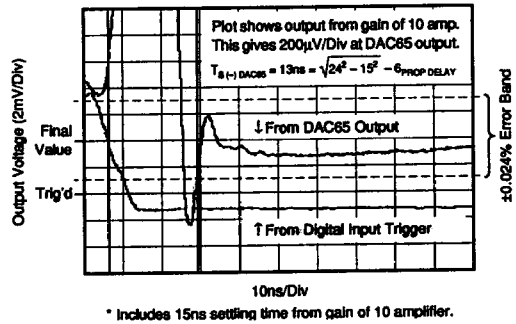
$\pm V_{CC}$ = ±15V, 5-minute warmup, and T_A = +25°C, unless otherwise noted.

POSITIVE FULL SCALE SETTLING TIME
(SEE SETTLING TIME SECTION CIRCUIT)



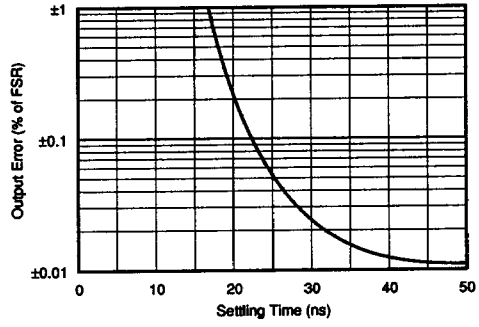
* Includes 15ns settling time from gain of 10 amplifier.

NEGATIVE FULL SCALE SETTLING TIME
(SEE SETTLING TIME SECTION CIRCUIT)

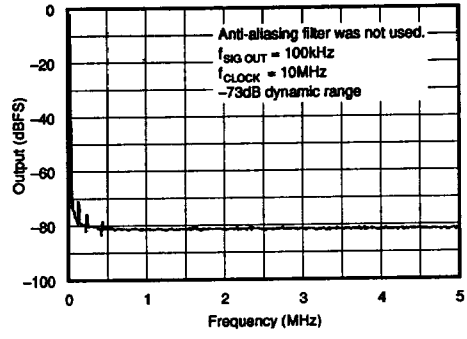


* Includes 15ns settling time from gain of 10 amplifier.

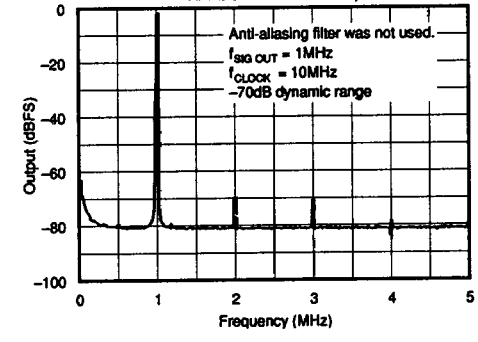
ACCURACY vs SETTLING TIME



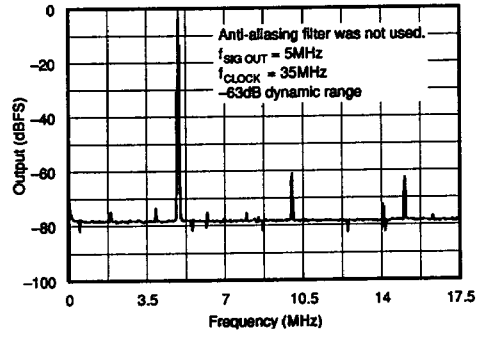
100kHz SPECTRAL PURITY
DIRECT DIGITAL FREQUENCY SYNTHESIZER CIRCUIT
(SEE DIRECT DIGITAL SYNTHESIZER
APPLICATION SECTION)



1MHz SPECTRAL PURITY
DIRECT DIGITAL FREQUENCY SYNTHESIZER CIRCUIT
(SEE DIRECT DIGITAL SYNTHESIZER
APPLICATION SECTION)



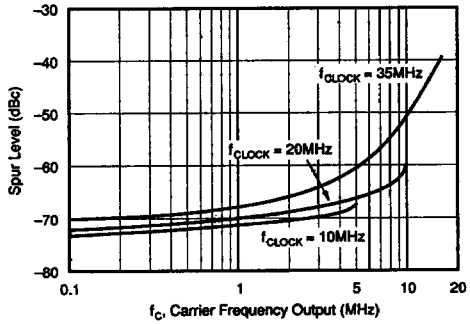
5MHz SPECTRAL PURITY
DIRECT DIGITAL FREQUENCY SYNTHESIZER CIRCUIT
(SEE DIRECT DIGITAL SYNTHESIZER
APPLICATION SECTION)



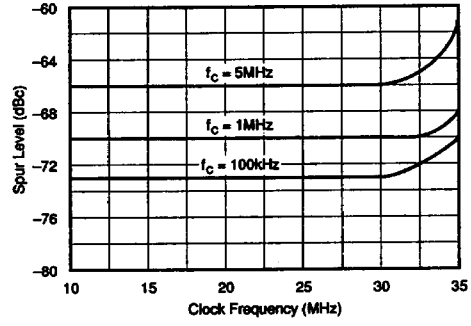
TYPICAL PERFORMANCE CURVES (CONT)

$\pm V_{CC}$ = ±15V, 5-minute warmup, and T_A = +25°C, unless otherwise noted.

SPURIOUS-FREE DYNAMIC RANGE vs CARRIER OUTPUT DIRECT DIGITAL SYNTHESIZER CIRCUIT WITH OUTPUT DEGLITCHER



SPURIOUS-FREE DYNAMIC RANGE vs CLOCK FREQUENCY DIRECT DIGITAL SYNTHESIZER CIRCUIT WITH OUTPUT DEGLITCHER (SEE APPLICATION SECTION)



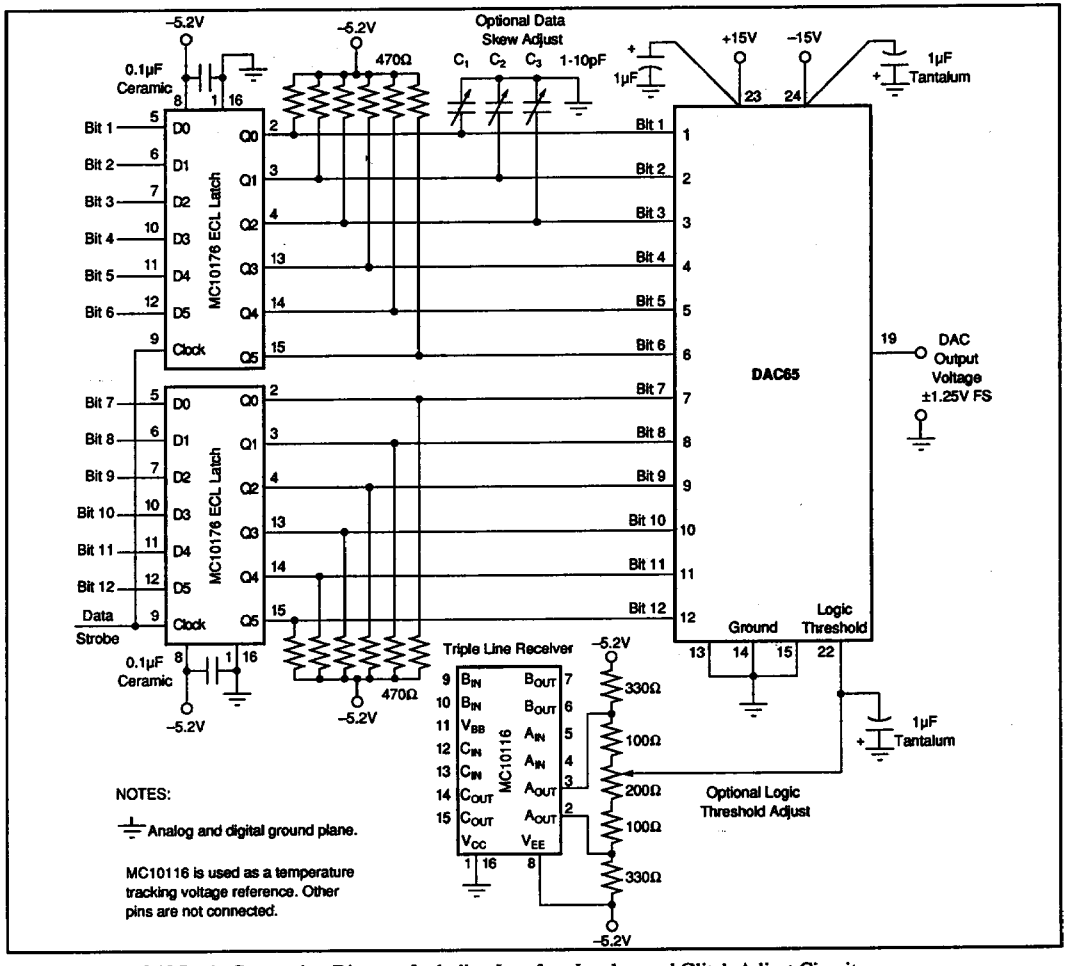


FIGURE 1. DAC65 Basic Connection Diagram Including Interface Latches and Glitch Adjust Circuitry.

THEORY OF OPERATION

The DAC65 is a laser-trimmed high-speed monolithic circuit. Internal capacitors are used to reduce the amount of external filtering required.

The DAC65 is comprised of 12 high-speed current switches which steer a reference current, of approximately ±6.25mA, into a 200Ω R-2R resistor ladder network. An accurate ±1.25V output voltage is produced at pin 19 by laser-trimming the reference voltage and ladder.

The reference voltage and output current have low drift. Integral linearity is trimmed to 14 bits.

INSTALLATION AND OPERATING INSTRUCTIONS

Figure 1 shows the basic connection for the DAC65.

Input ECL buffer latches shown are required and can also be used to adjust data skew to reduce output glitch energy (see output glitch section). In addition, logic threshold can be adjusted to optimize glitch and noise immunity (see logic threshold section). One ground plane is recommended for analog and digital signal returns as shown (see grounding section).

OPTIONAL OFFSET AND GAIN ADJUSTMENT

The offset and gain errors can be optionally adjusted to zero by using potentiometers shown in Figure 2. These points can be driven by low speed DACs to servo these errors to zero. If desired the trim pins maybe left unconnected.

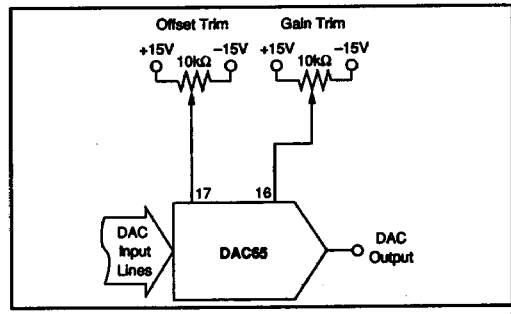


FIGURE 2. Optional External Offset and Gain Adjust.

LOGIC CODING TABLE, BOB, Bipolar Offset Binary

ECL Logic Coding	ECL Logic Voltage	V_{OUT} Bipolar	I_{OUT} Bipolar
000000000000	More Pos than −0.9V	−1.25V	−6.25mA
011111111111		0V	0mA
111111111111	More Neg than −1.79V	+1.25V	+6.25mA

ECL Logic Threshold is −1.3V.

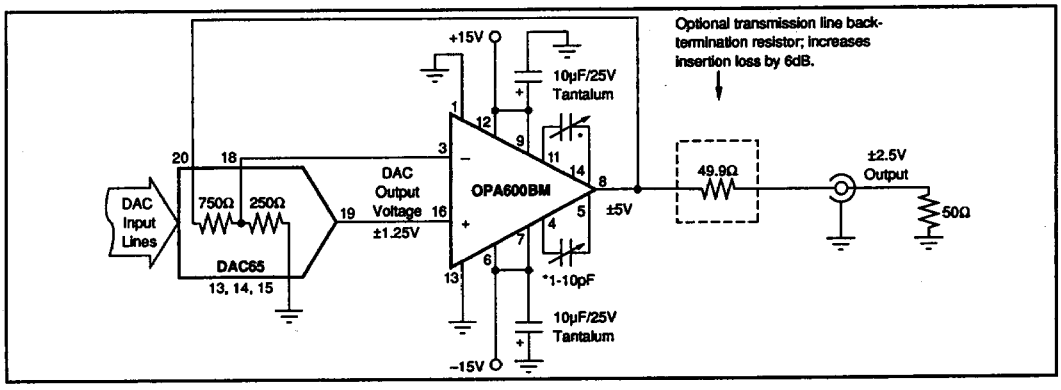


FIGURE 3. Optional Use of DAC65 Internal Resistors with External Amplifier/Cable Driver.

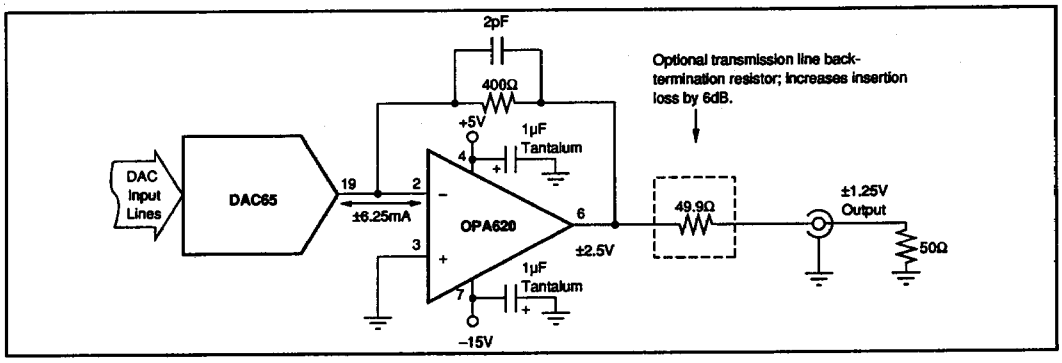


FIGURE 4. Using DAC65 Current Output with Transimpedance Amplifier/Cable Driver.

OPTIONAL EXTERNAL AMPLIFICATION

The ±1.25V at the output of the DAC65 can be accurately amplified by using the two thin film internal resistors with an external op amp shown in Figure 3. These resistors have been ratio-trimmed to high precision and are very stable over temperature. Also, since they will temperature-track the DAC65 internal ladder network, good overall temperature stability is achievable. Alternatively, the ±6.25mA can be converted to a voltage by a transimpedance amplifier such as the OPA600, or OPA620 circuit shown in Figure 4. This potentially gives higher speed due to the "virtual" ground load compared to the high impedance load of the circuit in Figure 3. Achieving settling times consistent with the DAC65 current output requires an exceptionally high performance op amp.

DISCUSSION OF SPECIFICATIONS

ACCURACY

Linearity of a digital-to-analog converter is one of the true measures of its performance. The linearity error of the DAC65 is specified over its entire temperature range. The analog output will not vary by more than ±1/2LSB from a best fit straight line over the specified temperature range.

Differential linearity error of a digital-to-analog converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over the specified temperature range is guaranteed.

DRIFT

Gain drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point difference for the DAC65 at t_{MIN} = +25°C, and t_{MAX}; 2) calculating the gain error with respect to the +25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm FSR/°C and is given in the electrical specifications (includes drift of internal reference).

Offset drift is a measure of the actual change in output around zero over the specified temperature range. The offset is measured at t_{MIN} = +25°C, and t_{MAX}. The maximum change in offset is referenced to the offset at +25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm FSR/°C).

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the digital-to-analog converter output. It is defined as a percent of FSR per percent of change in either the positive or negative supplies about the nominal power supply voltage. To improve high frequency noise rejection, each supply lead should be bypassed to ground as close to the unit as possible with a 1µF CS-type tantalum capacitor.

GROUNDING

Care must be exercised when grounding the DAC65 (pins 13, 14, and 15). In order to preserve the stated linearity and accuracy specifications, it is necessary to use the ground pins as the analog ground reference point. Any voltage drop that develops between any of these three pins and the actual ground reference point will degrade the performance of the DAC65. To achieve fast settling performance, it is recommended that pins 13, 14, and 15 be returned directly to a heavy copper ground plane. The analog ground should be located as close to the DAC65 as possible.

DIGITAL INTERFACE, LOGIC THRESHOLD, AND NOISE IMMUNITY

The DAC65 is compatible with conventional ECL logic families such as ECL 10k and 100k. Each DAC65 digital input is connected to the base of one side of a differential amplifier. The logic 0 input voltage is –1.79V with an input current of 1.2mA. The logic 1 input voltage is –0.9V with an input current of 1.2mA.

The logic threshold function of the DAC65 can be used to deal with noise in the ECL input-driving circuitry. The ECL 10k logic family has a noise immunity of 125mV maximum. It has a temperature coefficient of –1.4mV/°C and a power supply sensitivity of 16mV/%ΔV. With a realistic condition of a 5% power supply variation and a 25°C temperature change, the noise immunity would be degraded to 10mV. In addition, a precision high-speed digital-to-analog converter analog output is more susceptible to noise than is the ECL logic. Noise at levels acceptable to the digital logic can

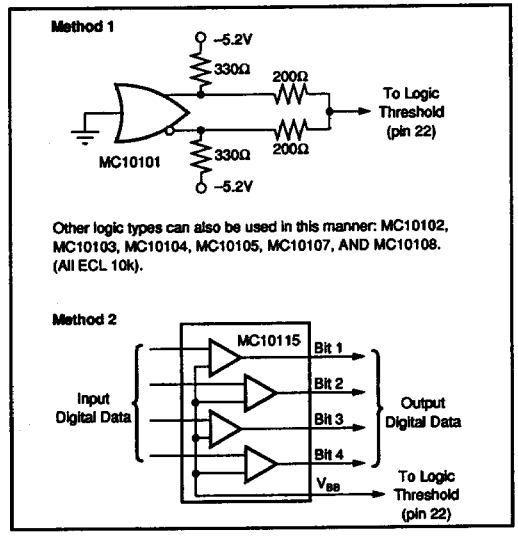


FIGURE 5. Driving the Logic Threshold Input.

couple through the D/A, resulting in an unacceptably noisy analog output. Low spurious output requires a clean digital input.

By making use of the logic threshold input feature, the threshold voltage of the DAC65 can be dynamically adjusted as the temperature and power supplies vary to give maximum noise immunity at the analog output over a wide range of conditions.

The MC10115 line receiver (or similar logic function) can be used to drive the DAC65 logic threshold, pin 22 (driven by the V_{BB} output of the ECL gate as shown in Figure 1). Refer to an ECL 10k data book for more detail. Figure 5 shows alternate methods for generating a logic threshold voltage.

SETTLING TIME

Settling time for the DAC65 is the total time required for the output to settle within an error band around its final value after a digital input change. This includes the digital delay of the internal switches.

The settling time of the DAC65 is determined by digitizing the output waveform produced by toggling the inputs between 011111111111 and 100000000000 continuously and verifying that the output settles to within ±1/2LSB in the specified time. The testing technique used is described in detail in Burr-Brown Application Note AN-115. Figure 6 shows a settling time circuit. The output amplifier, set to a gain of 10, is used to more easily observe the fast settling signal. Its gain, settling time, and propagation delay must be removed to arrive at the DAC65 performance.

Typical settling time curves of the DAC65 versus output error is shown in the Typical Performance Curves section. These curves are for digital code changes around the major carry. Typical output response characteristics of the DAC65 are also shown in the Typical Performance Curves section. Notice that these curves display the output of the gain of 10 amplifier from Figure 6. The unamplified DAC65 output is actually ten times smaller and is more difficult to observe due to noise.

In order to achieve minimum settling time, it is necessary to observe the following good high-frequency construction techniques:

1. The power supplies, including the logic threshold input (pin 22), should be bypassed by 1µF CS-type tantalum capacitors connected directly to the pins.
2. Use a heavy 2 ounce ground plane to connect common ground points.
3. Remove the ground plane beneath signal lines where it would add capacitance.
4. Separate analog and digital signal leads to avoid coupling of the digital signal into the analog paths.
5. Bring the source of the digital driving signal as close to the inputs of the DAC65 as possible. If the digital inputs are not clean, it will be necessary to reshape them using a latch or line drivers. Figure 1 shows how to interface the DAC65 to input latches. It is recommended that the logic power line be bypassed near the digital logic circuitry to achieve clean logic signals.
6. If possible, the DAC65 should be soldered directly into the printed circuit board although low profile sockets are acceptable.

OUTPUT GLITCH

"Glitch" is defined as the difference in the waveforms at the output of the DAC when data skew is present and when it is not. The measurement of glitch is accomplished by measuring the area between these two waveforms.

An output glitch of less than 250LSBns is achievable with the DAC65 because it employs ECL circuitry and current switches that have virtually identical delay times for input signals, making either positive or negative logic transitions. A glitch results when the digital data changes from one code to the next and the bits do not all switch at the same time. The delay time between the earliest and latest switching bits is called skew time. Typically during the skew time of the digital data, which includes the DAC switching, the digital code is undefined and the DAC output can go to any voltage between the full scale extremes. The glitch creates noisy output spurs and harmonics which can be troublesome in

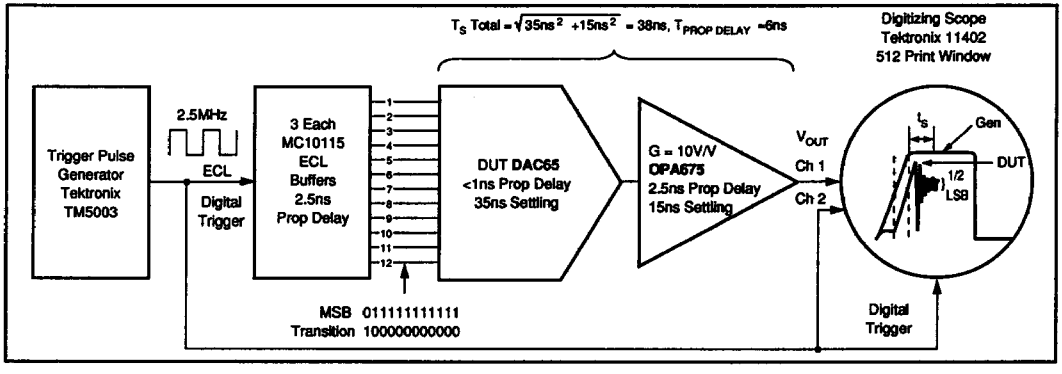


FIGURE 6. High Speed DAC65 Settling Time Test Circuit.

applications such as precision displays and complex waveform generation. Figure 7 is a photograph of a scope trace of the DAC output with a glitch occurring at the major carry transition.

The DAC65 design has been optimized for low glitch energy. However, a further reduction in the output glitch can be achieved by adjusting the skew of the higher order bits of the driving circuitry and by adjusting the logic threshold. This can be done by connecting a variable capacitor from the data lines to ground on each of the first three significant bits, as shown in Figure 1. More than three lines may be adjusted if desired. It will be necessary to create a driving digital code pattern that causes a major carry transition around these bits. It is convenient to use a digital ramp from a counter for this purpose. Initially set the logic threshold exactly half-way between logic 1 and a logic 0. This will be about –1.3V. Then examine the major carry transition associated with bit 3 and adjust the capacitor for minimum glitch. Make the same adjustment to bit 1. If done in this order, interactions will be minimized. Finally, fine tune the response by adjusting the logic threshold voltage (pin 22) for minimum glitch. It may be necessary to repeat this procedure once or twice for complete optimization.

Another approach is to apply a sinewave of amplitude that just toggles bit 3 with bits 32 and 1 at zero. Observe the spectrum on an analog spectrum analyzer and adjust C_3 for minimum amplitude of frequency spurs. Successively increase the sinewave amplitude and stop at each bit (bit 2 and bit 1) to adjust C_2 and C_1 for minimum spurs. This method assures lowest distortion by minimizing spurs caused by DAC output glitch.

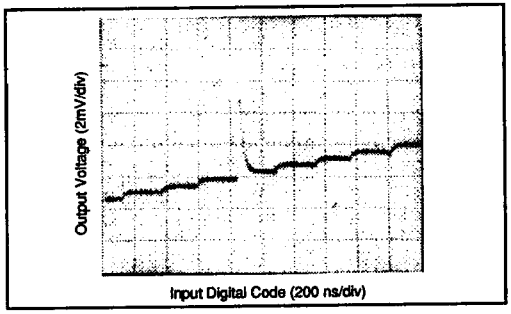


FIGURE 7. Typical Glitch Response at Major Carry Transition.

APPLICATIONS INFORMATION

The DAC65 can be used to reconstruct an analog signal at the output of a digital arbitrary waveform generator. It can be used without an external output amplifier or can be used with a 50Ω coaxial cable driver amplifier such as the OPA620, OPA621, or OPA600. ECL buffers can be used in addition to latches on the digital input to reduce high frequency noise on the ECL inputs from leaking through to the analog output.

TWO CHANNEL SWITCHED OUTPUT

Higher speed can be obtained from a direct digital frequency synthesizer by using two DAC65s in the circuit shown in Figure 8. DACs are ping-ponged and each DAC samples every other data point. While one DAC is settling on one sample, the other is being applied to the OPA675 (a switched input op amp used as a high speed buffered multiplexer). This circuit can be used to produce higher bandwidth signals or can be used as an output deglitcher when timed properly. Trimming or matching the two DACs may be required.

DIRECT DIGITAL SYNTHESIZER

The DAC65 can be used to construct a high quality direct digital synthesizer (DDS). Figures 9 and 10 show a Stanford Telecom STEL-1173 numerical controlled oscillator (NCO) with internal sinewave weighed ROM. DAC deglitching is done with a SHC600 sample/hold in Figure 9. Five potentiometers are used for skew timing adjust at the input in Figure 10. Test results shown in the Typical Performance Curves were generated by circuits shown in Figure 9. Output deglitching and data skew adjust can be used together for somewhat lower spur levels.

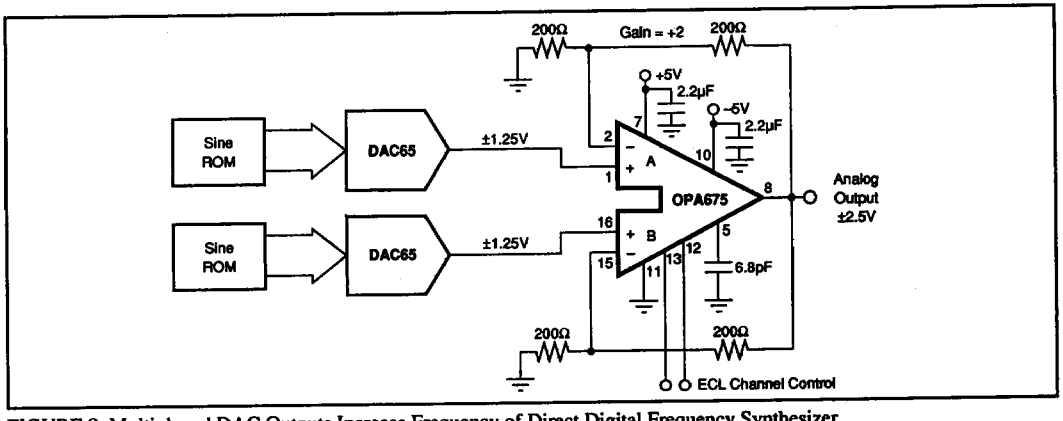


FIGURE 8. Multiplexed DAC Outputs Increase Frequency of Direct Digital Frequency Synthesizer.

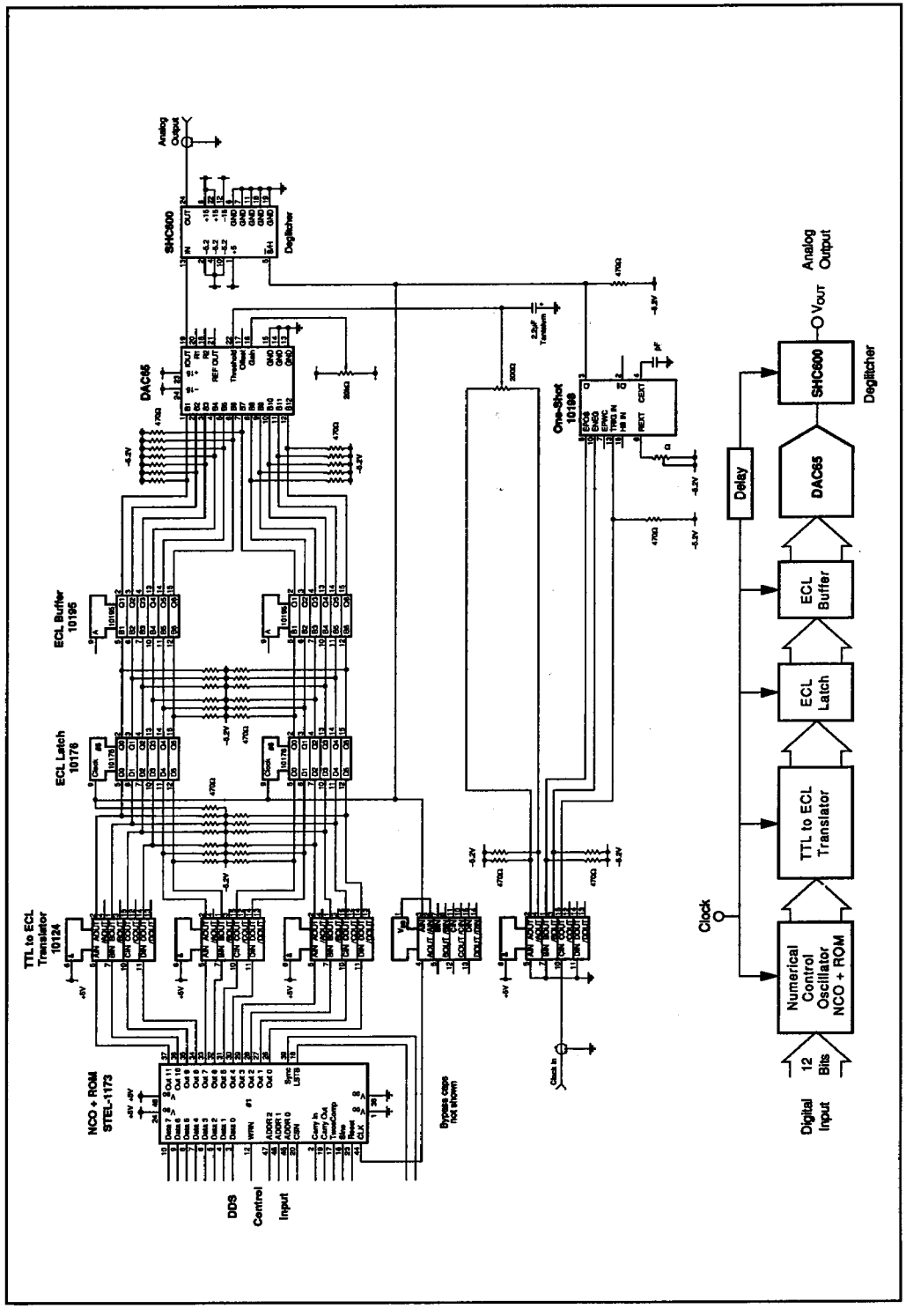


FIGURE 9. Schematic and Block Diagram of Direct Digital Frequency Synthesizer (DDFS) with Deglitched Output.

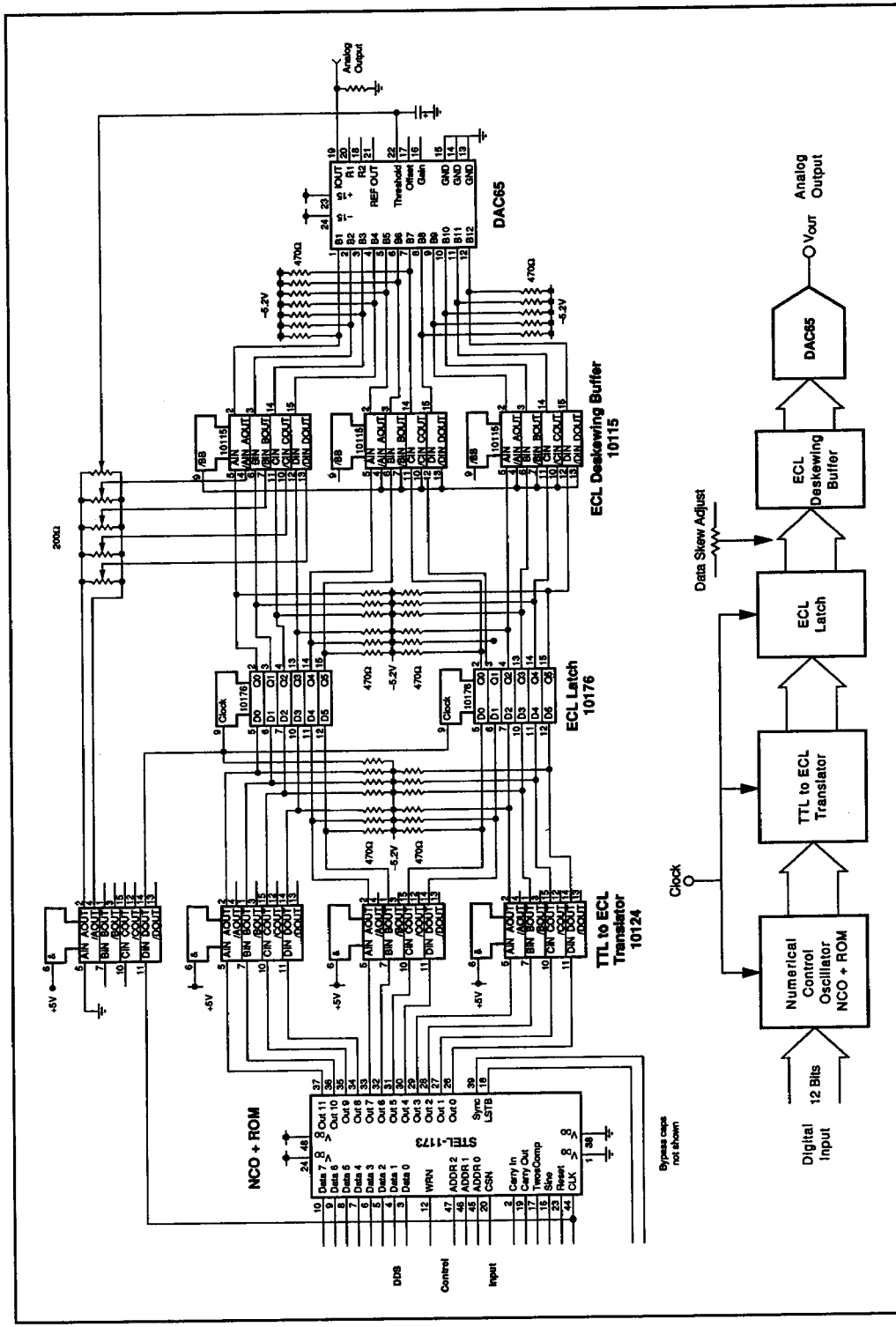


FIGURE 10. Schematic and Block Diagram of Direct Digital Frequency Synthesizer (DDFS) with Data Skew Adjust.