

T-46-23-DS



MT5C6401

SRAM

64K x 1 SRAM

FAST SRAM

FEATURES

- High speed: 12, 15, 20, 25, 30 and 35ns
- High-performance, low-power, CMOS double metal process
- Single +5V ($\pm 10\%$) power supply
- Easy memory expansion with \overline{CE} option
- All inputs and outputs are TTL compatible

OPTIONS

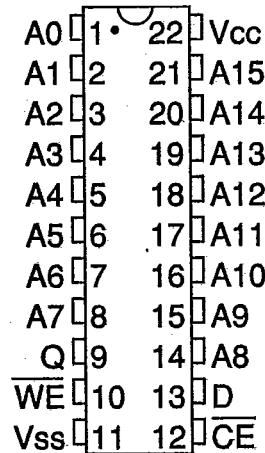
- Timing
 - 12ns access
 - 15ns access
 - 20ns access
 - 25ns access
 - 30ns access
 - 35ns access
- Packages
 - Plastic DIP (300 mil)
 - Ceramic DIP (300 mil)
 - Plastic SOJ (300 mil)
 - Ceramic LCC
- Two Volt Data Retention

MARKING

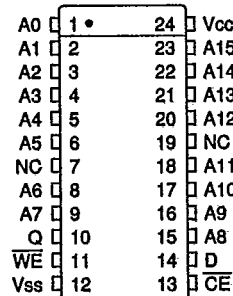
- 12
- 15
- 20
- 25
- 30
- 35
- None
- C
- DJ
- EC
- L

PIN ASSIGNMENT (Top View)

22L/300 DIP
(A-6, B-6)



24L/300 SOJ
(E-4)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

For flexibility in high speed memory applications, Micron offers chip enable (\overline{CE}) on all organizations. This enhancement can place the outputs in a high impedance state for additional flexibility in system design. The x1 configuration features separate data input and output.

Writing to these devices is accomplished when write enable (\overline{WE}) and \overline{CE} inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH and \overline{CE} goes to LOW. The device offers a reduced power standby mode when disabled. This allows system designs to achieve low standby power requirements.

All devices operate from a single +5V power supply and all inputs and outputs are fully TTL compatible.

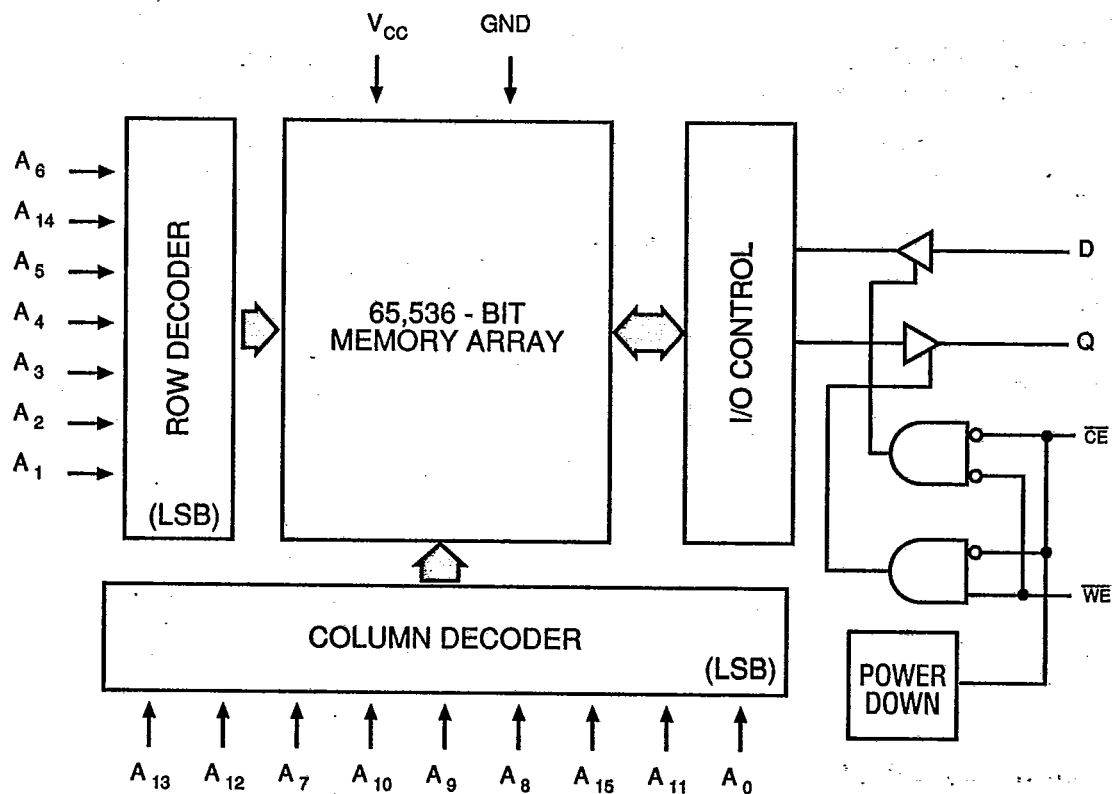
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FUNCTIONAL BLOCK DIAGRAM

FAST SRAM



TRUTH TABLE

MODE	\overline{CE}	WE	DQ	POWER
STANDBY	H	X	HIGH-Z	STANDBY
READ	L	H	Q	ACTIVE
WRITE	L	L	HIGH-Z	ACTIVE



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ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc supply relative to Vss	-1.0V to +7.0V
Storage Temperature (Ceramic)	-65°C to +150°C
Storage Temperature (Plastic)	-55°C to +150°C
Power Dissipation	1W
Short Circuit Output Current	50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; Vcc = 5.0V ± 10%)

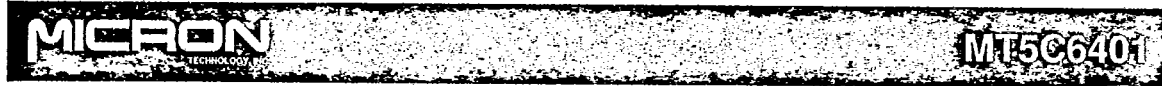
DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{CC} + 1	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{CC}	I _{LI}	-5	5	μA	
Output Leakage Current	Output(s) Disabled, 0V ≤ V _{OUT} ≤ V _{CC}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1

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DESCRIPTION	CONDITIONS	SYMBOL	MAX						UNITS	NOTES
			-12	-15	-20	-25	-30	-35		
Power Supply Current: Operating	$\overline{CE} \leq V_{IL}; V_{CC} = \text{MAX}$ f = MAX = 1/4RC, Outputs Open	I _{CC}	140	130	120	110	100	100	mA	3
Power Supply Current: Standby	$\overline{CE} \geq V_{IH}; V_{CC} = \text{MAX}$ f = MAX = 1/4RC, Outputs Open	I _{SB1}	60	50	40	30	30	30	mA	
	$\overline{CE} \geq V_{CC} - 0.2V; V_{CC} = \text{MAX}$ V _{IL} ≤ V _{SS} + 0.2V; V _{IH} ≥ V _{CC} - 0.2V; f = 0	I _{SB2}	5	5	5	5	5	5	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance	T _A = 25°C; f = 1MHz V _{CC} = 5V	C _I		7	pF	4
Output Capacitance		C _O		7	pF	4



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ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5, 13) (0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ± 10%)

FAST SRAM

DESCRIPTION	SYM	-12		-15		-20		-25		-30		-35		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle															
READ cycle time	t _{RC}	12		15		20		25		30		35		ns	
Address access time	t _{AA}		12		15		20		25		30		35	ns	
Chip Enable access time	t _{ACE}		12		12		15		20		25		30	ns	
Output hold from address change	t _{OH}	3		3		3		3		3		3		ns	
Chip Enable to output in Low-Z	t _{LZCE}	3		3		5		5		5		5		ns	
Chip Disable to output in High-Z	t _{HZCE}		7		7		10		10		15		20	ns	6, 7
Chip Enable to power-up time	t _{PU}	0		0		0		0		0		0		ns	
Chip Disable to power-down time	t _{PD}		12		15		20		25		30		35	ns	
WRITE Cycle															
WRITE cycle time	t _{WC}	12		15		20		25		30		35		ns	
Chip Enable to end of write	t _{CW}	10		12		15		20		25		25		ns	
Address valid to end of write	t _{AW}	12		12		15		20		25		25		ns	
Address setup time	t _{AS}	0		0		0		0		0		0		ns	
Address hold from end of write	t _{AH}	0		0		0		0		0		0		ns	
Write pulse width	t _{WP}	10		12		15		20		25		25		ns	
Data setup time	t _{DS}	8		8		10		10		15		15		ns	
Data hold time	t _{DH}	0		0		0		0		0		0		ns	
Write Disable to output in Low-Z	t _{LZWE}	2		2		2		2		2		2		ns	
Write Enable to output in High-Z	t _{HZWE}		6		6		8		10		12		15	ns	6

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AC TEST CONDITIONS

Input pulse levels	V _{SS} to 3.0V
Input rise and fall times	5ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

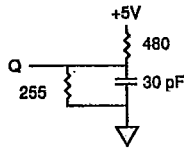


Fig. 1 OUTPUT LOAD EQUIVALENT

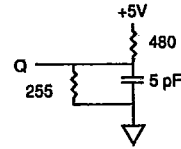


Fig. 2 OUTPUT LOAD EQUIVALENT

NOTES

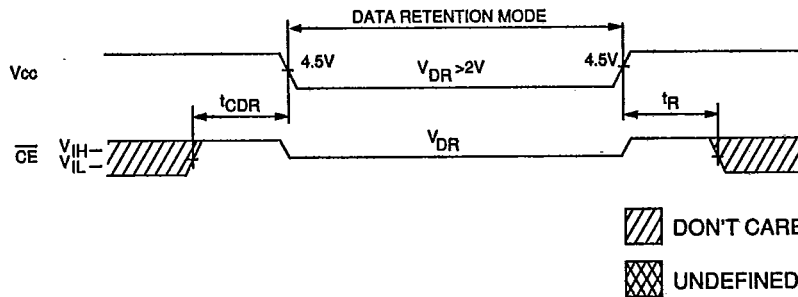
1. All voltages referenced to V_{SS} (GND).
2. -3.0V for pulse width < 20ns.
3. I_{CC} is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. ^tHZCE and ^tHZWE are specified with CL = 5pF as in Fig. 2. Transition is measured ± 500mV from steady state voltage.
7. At any given temperature and voltage condition, ^tHZCE is less than ^tLZCE.
8. \overline{WE} is HIGH for READ cycle.
9. Device is continuously selected. All chip enables held in their active state.
10. Address valid prior to or coincident with latest occurring chip enable.
11. ^tRC = Read Cycle Time.
12. Chip enable (\overline{CE}) and write enable (\overline{WE}) can initiate and terminate a WRITE cycle.
13. For automotive, industrial and extended temperature specifications refer to page 4-167.

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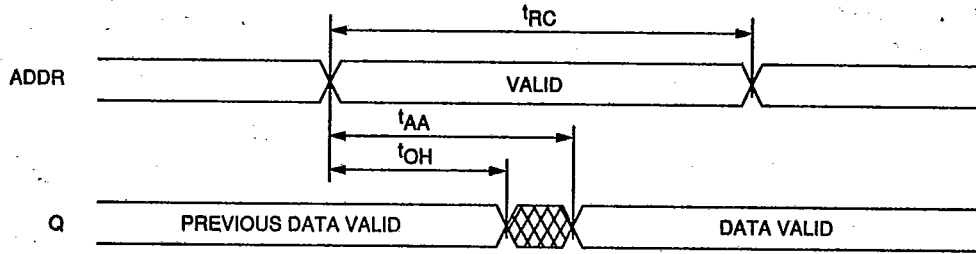
DATA RETENTION ELECTRICAL CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS	NOTES	
V _{CC} for Retention Data		V _{DR}	2		—	V		
Data Retention Current	$\overline{CE} \geq (V_{CC} - 0.2V)$ $V_{IN} \geq (V_{CC} - 0.2V)$ or $\leq 0.2V$	I _{CCDR}	V _{CC} = 2V		95	250	μA	
	V _{CC} = 3V			300	400	μA		
Chip Deselect to Data Retention Time		^t CDR	0		—	ns	4	
Operation Recovery Time		^t R	^t RC			ns	4, 11	

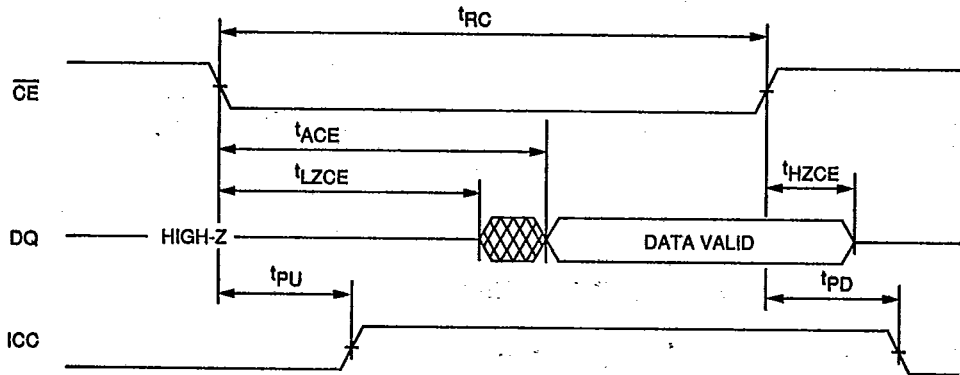
LOW V_{CC} DATA RETENTION WAVEFORM



READ CYCLE NO. 1 8, 9



READ CYCLE NO. 2 7, 8, 10



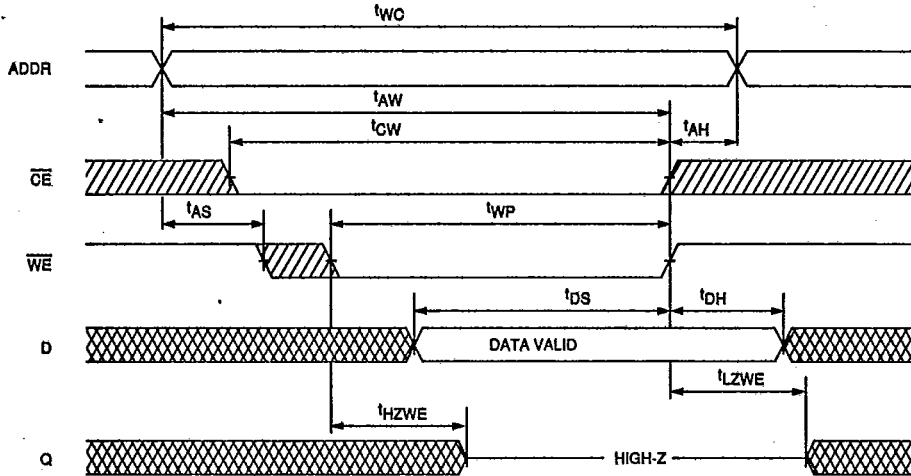
 DON'T CARE
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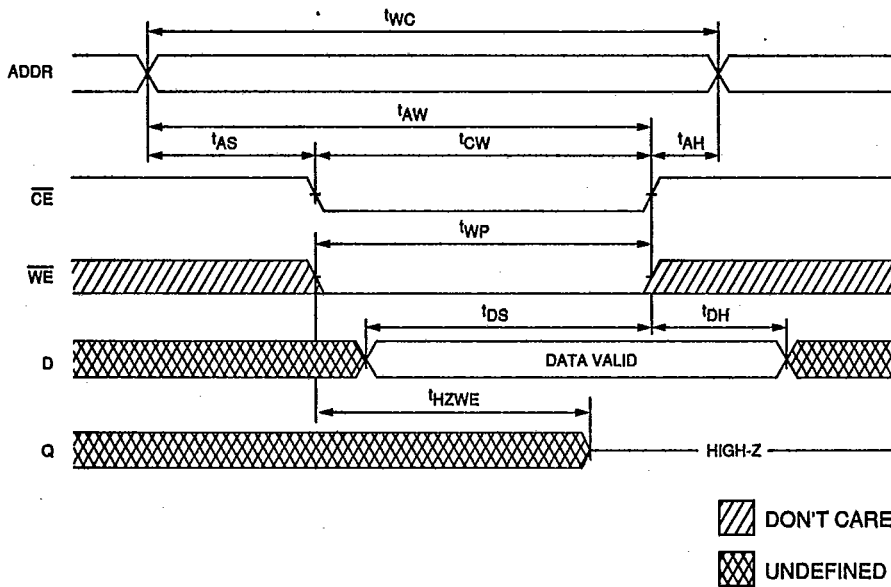
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WRITE CYCLE NO. 1
(Write Enable Controlled) 7, 12



WRITE CYCLE NO. 2
(Chip Enable Controlled) 12



▨ DON'T CARE
▩ UNDEFINED

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