

### Features

- 100% Tested Low Voltage Noise:  $2.7\text{nV}/\sqrt{\text{Hz}}$  Typ  
 $4.2\text{nV}/\sqrt{\text{Hz}}$  Max
- Slew Rate:  $4.5\text{V}/\mu\text{s}$  Typ
- Gain Bandwidth Product:  $12.5\text{MHz}$  Typ
- Offset Voltage, Prime Grade:  $70\mu\text{V}$  Max  
Low Grade:  $100\mu\text{V}$  Max
- High Voltage Gain: 5 Million Min
- Supply Current Per Amplifier:  $2.75\text{mA}$  Max
- Common Mode Rejection:  $112\text{dB}$  Min
- Power Supply Rejection:  $116\text{dB}$  Min
- Available in 8-Pin SO Package

### Applications

- Two and Three Op Amp Instrumentation Amplifiers
- Low Noise Signal Processing
- Active Filters
- Microvolt Accuracy Threshold Detection
- Strain Gauge Amplifiers
- Direct Coupled Audio Gain Stages
- Tape Head Preamplifiers
- Infrared Detectors

### Description

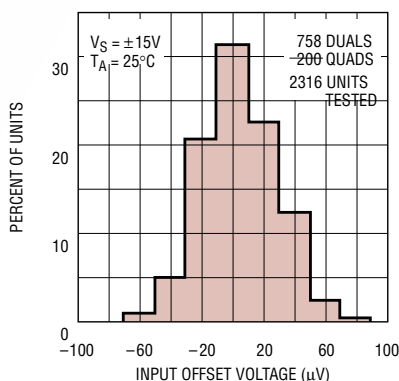
The FT1124 dual and FT1125 quad are high performance op amps that offer higher gain, slew rate and bandwidth than the industry standard OP-27 and competing OP-270/OP-470 op amps. In addition, the FT1124/FT1125 have lower  $I_B$  and  $I_{OS}$  than the OP-27; lower  $V_{OS}$  and noise than the OP-270/OP-470.

In the design, processing and testing of the device, particular attention has been paid to the optimisation of the entire distribution of several key parameters. Slew rate, gain bandwidth and  $1\text{kHz}$  noise are 100% tested for each individual amplifier. Consequently, the specifications of even the lowest cost grades (the FT1124C and the FT1125C) have been spectacularly improved compared to equivalent grades of competing amplifiers.

Power consumption of the FT1124 is one half of two OP-27s. Low power and high performance in an 8-pin SO package make the FT1124 a first choice for surface mounted systems and where board space is restricted.

For a decompensated version of these devices, with three times higher slew rate and bandwidth, please see the FT1126/FT1127 data sheet.

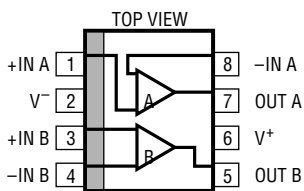
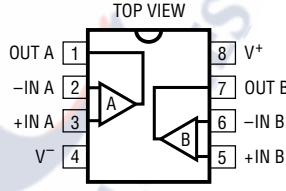
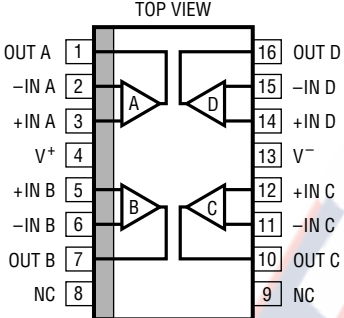
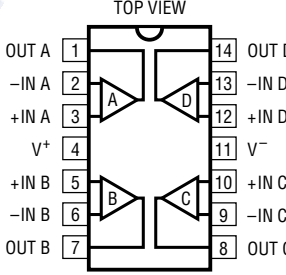
### Input Offset Voltage Distribution (All Packages, FT1124 and FT1125)



### Absolute Maximum Ratings (Note 1)

Supply Voltage .....  $\pm 22V$   
 Input Voltages ..... Equal to Supply Voltage  
 Output Short-Circuit Duration ..... Indefinite  
 Differential Input Current (Note 6) .....  $\pm 25mA$   
 Lead Temperature (Soldering, 10 sec) .....  $300^{\circ}C$   
 Storage Temperature Range .....  $-65^{\circ}C$  to  $150^{\circ}C$

Operating Temperature Range  
 FT1124AC/FT1124C .....  
 FT1125AC/FT1125C (Note 10) .....  $-40^{\circ}C$  to  $85^{\circ}C$   
 FT1124AI/FT1124I .....  $-40^{\circ}C$  to  $85^{\circ}C$   
 FT1124AM/FT1124M .....  
 FT1125AM/FT1125M .....  $-55^{\circ}C$  to  $125^{\circ}C$

 <p>S8 PACKAGE 8-LEAD PLASTIC SO <math>T_{JMAX} = 140^{\circ}C, \theta_{JA} = 190^{\circ}C/W</math></p> <p>NOTE: THIS PIN CONFIGURATION DIFFERS FROM THE 8-PIN PDIP CONFIGURATION. INSTEAD, IT FOLLOWS THE INDUSTRY STANDARD FT1013DS8 SO PACKAGE PIN LOCATIONS</p>	<p>ORDER PART NUMBER</p> <p>FT1124CS8 FT1124AIS8 FT1124IS8</p> <p>S8 PART MARKING</p> <p>1124 1124AI 1124I</p>	 <p>TOP VIEW</p> <p>N8 PACKAGE 8-LEAD PDIP <math>T_{JMAX} = 140^{\circ}C, \theta_{JA} = 130^{\circ}C/W</math></p> <p>J8 PACKAGE 8-LEAD CERAMIC DIP <math>T_{JMAX} = 160^{\circ}C, \theta_{JA} = 100^{\circ}C/W</math></p>	<p>ORDER PART NUMBER</p> <p>FT1124ACN8 FT1124CN8</p> <p>FT1124CJ8 FT1124AMJ8 FT1124MJ8</p>
 <p>TOP VIEW</p> <p>SW PACKAGE 16-LEAD PLASTIC SO WIDE <math>T_{JMAX} = 140^{\circ}C, \theta_{JA} = 130^{\circ}C/W</math></p>	<p>FT1125CSW</p>	 <p>TOP VIEW</p> <p>N PACKAGE 14-LEAD PDIP <math>T_{JMAX} = 140^{\circ}C, \theta_{JA} = 110^{\circ}C/W (N)</math></p> <p>J PACKAGE 14-LEAD CERAMIC DIP <math>T_{JMAX} = 160^{\circ}C, \theta_{JA} = 80^{\circ}C/W</math></p>	<p>FT1125ACN FT1125CN</p> <p>FT1125CJ FT1125AMJ FT1125MJ</p>

# ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_S = \pm 15\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	FT1124AC/AI/AM FT1125AC/AM			FT1124C/I/M FT1125C/M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	FT1124 FT1125	20 25	70 90		25 30	100 140	$\mu\text{V}$ $\mu\text{V}$	
$\frac{\Delta V_{OS}}{\Delta \text{Time}}$	Long-Term Input Offset Voltage Stability		0.3			0.3		$\mu\text{V}/\text{Mo}$	
$I_{OS}$	Input Offset Current	FT1124 FT1125	5 6	15 20		6 7	20 30	nA nA	
$I_B$	Input Bias Current		$\pm 7$	$\pm 20$		$\pm 8$	$\pm 30$	nA	
$e_n$	Input Noise Voltage	0.1Hz to 10Hz (Notes 8, 9)	70	200		70		$\text{nV}_{\text{P-P}}$	
	Input Noise Voltage Density	$f_0 = 10\text{Hz}$ (Note 5) $f_0 = 1000\text{Hz}$ (Note 3)	3.0 2.7	5.5 4.2		3.0 2.7	5.5 4.2	$\text{nV}/\sqrt{\text{Hz}}$ $\text{nV}/\sqrt{\text{Hz}}$	
$i_n$	Input Noise Current Density	$f_0 = 10\text{Hz}$ $f_0 = 1000\text{Hz}$	1.3 0.3			1.3 0.3		$\text{pA}/\sqrt{\text{Hz}}$ $\text{pA}/\sqrt{\text{Hz}}$	
$V_{CM}$	Input Voltage Range		$\pm 12$	$\pm 12.8$		$\pm 12$	$\pm 12.8$	V	
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 12\text{V}$	112	126		106	124	dB	
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$	116	126		110	124	dB	
$A_{VOL}$	Large-Signal Voltage Gain	$R_L \geq 10\text{k}$ , $V_{OUT} = \pm 10\text{V}$ $R_L \geq 2\text{k}$ , $V_{OUT} = \pm 10\text{V}$	5 2	17 4		3.0 1.5	15 3	$\text{V}/\mu\text{V}$ $\text{V}/\mu\text{V}$	
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2\text{k}$	$\pm 13$	$\pm 13.8$		$\pm 12.5$	$\pm 13.8$	V	
SR	Slew Rate	$R_L \geq 2\text{k}$ (Notes 3, 7)	3	4.5		2.7	4.5	$\text{V}/\mu\text{s}$	
GBW	Gain Bandwidth Product	$f_0 = 100\text{kHz}$ (Note 3)	9	12.5		8	12.5	MHz	
$Z_O$	Open-Loop Output Resistance	$V_{OUT} = 0$ , $I_{OUT} = 0$		75			75	$\Omega$	
$I_S$	Supply Current per Amplifier			2.3	2.75		2.3	2.75	mA
	Channel Separation	$f \leq 10\text{Hz}$ (Note 9) $V_{OUT} = \pm 10\text{V}$ , $R_L = 2\text{k}$	134	150		130	150	dB	

The ● denotes the specifications which apply over the  $-55^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$  temperature range,  $V_S = \pm 15\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS (Note 2)	FT1124AM FT1125AM			FT1124M FT1125M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$V_{OS}$	Input Offset Voltage	FT1124 FT1125	● ●	50 55	170 190		60 70	250 290	$\mu\text{V}$ $\mu\text{V}$
$\frac{\Delta V_{OS}}{\Delta \text{Temp}}$	Average Input Offset Voltage Drift	(Note 5)	●	0.3	1.0		0.4	1.5	$\mu\text{V}/^\circ\text{C}$
$I_{OS}$	Input Offset Current	FT1124 FT1125	● ●	18 18	45 55		20 20	60 70	nA nA
$I_B$	Input Bias Current		●	$\pm 18$	$\pm 55$		$\pm 20$	$\pm 70$	nA
$V_{CM}$	Input Voltage Range		●	$\pm 11.3$	$\pm 12$		$\pm 11.3$	$\pm 12$	V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 11.3\text{V}$	●	106	122		100	120	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$	●	110	122		104	120	dB
$A_{VOL}$	Large-Signal Voltage Gain	$R_L \geq 10\text{k}$ , $V_{OUT} = \pm 10\text{V}$ $R_L \geq 2\text{k}$ , $V_{OUT} = \pm 10\text{V}$	● ●	3 1	10 3		2.0 0.7	10 2	$\text{V}/\mu\text{V}$ $\text{V}/\mu\text{V}$
$V_{OUT}$	Maximum Output Voltage Swing	$R_L \geq 2\text{k}$	●	$\pm 12.5$	$\pm 13.6$		$\pm 12$	$\pm 13.6$	V
SR	Slew Rate	$R_L \geq 2\text{k}$ (Notes 3, 7)	●	2.3	3.8		2	3.8	$\text{V}/\mu\text{s}$
$I_S$	Supply Current per Amplifier		●	2.5	3.25		2.5	3.25	mA



Ashley Crt, Henley,  
Marlborough, Wilts, SN8 3RH UK  
**Tel: +44(0)1264 731200**  
**Fax: +44(0)1264 731444**  
E-mail  
[info@forcetechnologies.co.uk](mailto:info@forcetechnologies.co.uk)  
[tech@forcetechnologies.co.uk](mailto:tech@forcetechnologies.co.uk)  
[sales@forcetechnologies.co.uk](mailto:sales@forcetechnologies.co.uk)

**[www.forcetechnologies.co.uk](http://www.forcetechnologies.co.uk)**

Unless otherwise stated in this SCD/Data sheet, Force Technologies Ltd reserve the right to make changes, without notice, in the products, including circuits, cells and/or software, described or contained herein in order to improve design and/or performance. Force Technologies resumes no responsibility or liability for the use of any of these products, conveys no licence or any title under patent, copyright, or mask work to these products, and makes no representation or warranties that that these products are free from patent, copyright or mask work infringement, unless otherwise specified.

**Life Support Applications**

Force Technologies products are not designed for use in life support appliances, devices or systems where malfunction of a Force Technologies product can reasonably be expected to result in a personal injury. Force Technologies customers using or selling Force Technologies products for use in such applications do so at their own risk and agree to fully indemnify Force Technologies for any damages resulting from such improper use or sale.

All trademarks acknowledged

Copyright Force Technologies Ltd 2007

**[Click here to request full data sheet](#)**