300mA Ultra-low Noise, Ultra-Fast
CMOS LDO Regulator

LR9193

FEATURES

- Ultra-low Noise for RF Application
- Ultra-Fast Respose in Line/Load Transient
- Quick Start-Up (Typically 50μS)
- <0.01μA Standby Current When Shutdown.
- Low Dropout:220mV@300mA
- Wide Operating Voltage Ranges:2.5V to 5.5V
- TTL-logic-Controlled Shutdown Input
- Low Temperature Coefficient
- Current Limiting Protection
- Thermal Shutdown Protection
- Only 1μF Output Capacitor Required for Stability
- High Power Supply Rejection Ratio
- Custom Voltage Available
- Fast output discharge
- Available in 5-Lead SOT-23 and SC-70 Package

APPLICATIONS

- Cellular and Smart Phones
- Battery-Powered Equipment
- Laptop, Palmtops,Notebook Computers
- Hand-Held Instruments
- PCMCIA Cards
- MP3 Players
- Portable Information Appliances

DESCRIPTION

The LR9193 is designed for portable RF and wireless applications with demanding performance and space requirements. The LR9193 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. A noise bypass pin is available for further reduction of output noise. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The LR9193 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LR9193 consumes less than 0.01μA in shutdown mode and has fast turn-on time less than 50μs. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. Available in the 5-lead of SC-70,SOT-23,packages.

ORDERING INFORMATION

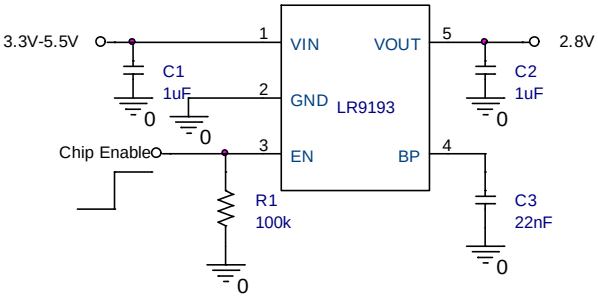
LR9193-XX XX

Package:
RN:SOT-23-5
URN:SC-70-5

Output Voltage:

12:1.2V 15:1.5V
18:1.8V 28:2.8V
33:3.3V CT: custom fixed output(50mv step)
AD:Adjustable

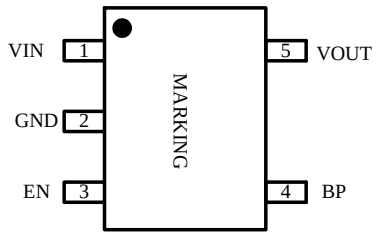
TYPICAL APPLICATION



Absolute Maximum Rating (Note 1)

Input Supply Voltage (V_{CC})	-0.3V to +6V	Maximum Junction Temperature	125°C
EN Input Voltage	-0.3V to $+V_{in}$	Operating Temperature Range **(Note2)**	-40°C to 85°C
Output Voltage	-0.3V to Vin+0.3V	Storage Temperature Range	-65°C to 125°C
BP Voltage	-0.3V to +6V	Lead Temperature (Soldering, 10s)	300°C
Output Current	300mA		

Package Information



SOT23-5

Part Number	Top Mark	Temp Range
LR9193-1.2	X V Y M **(Note 3)**	-40°C to +85°C
LR9193-2.8	X V Y M	-40°C to +85°C

Thermal Resistance (Note 4):

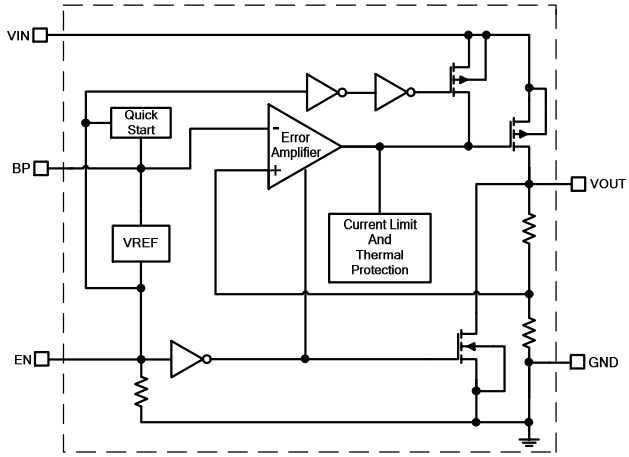
Package	Θ_{JA}	Θ_{JC}
SOT23-5	250°C/W	130°C/W

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.
Note 2: The LR9193 is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.
Note 3: X:Product Code V:Voltage Code Y:Year M:Month.
Note 4: Thermal Resistance is specified with approximately 1 square of 1 oz copper.

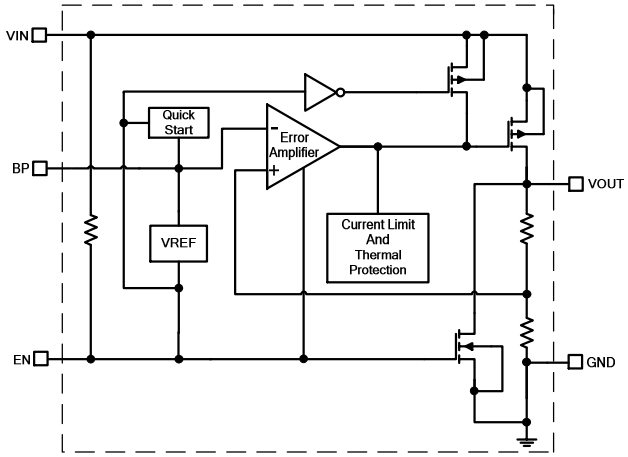
Pin Description

PIN	NAME	FUNCTION
3	EN	Chip Enable(Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
4	BP	Reference Noise Bypass.
2	GND	Ground.
5	VOUT	Output Voltage.
1	VIN	Power Input Voltage.

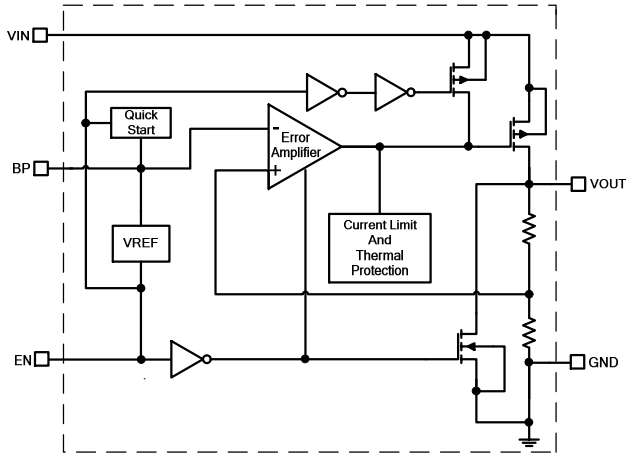
Block Diagram



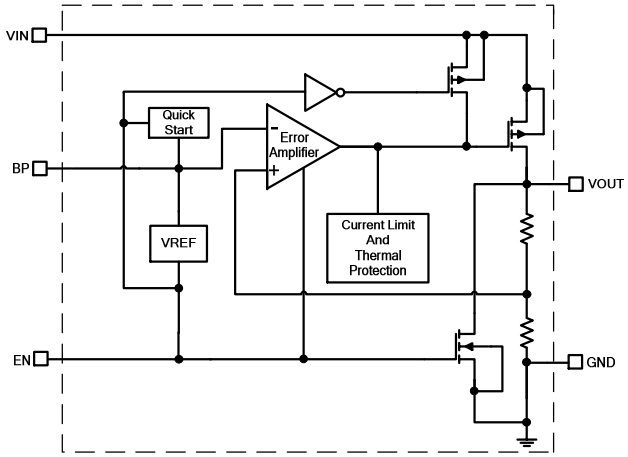
LR9193- X.X A



LR9193- X.X C



LR9193- X.X B



LR9193- X.X D

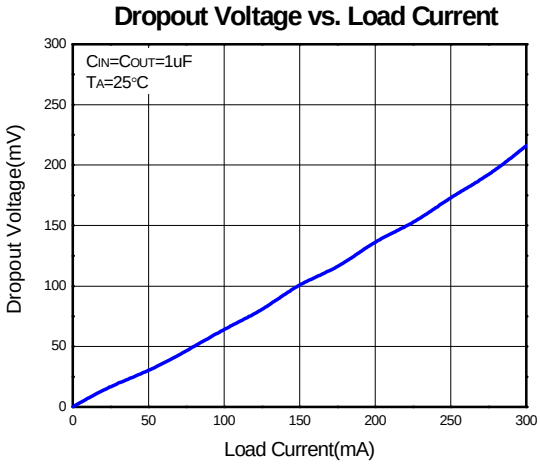
Electrical Characteristics (Note 5)

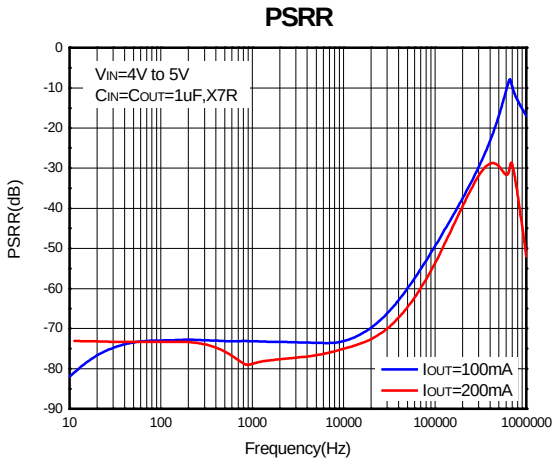
(V_{IN}=3.6V , EN=V_{IN}, C_{IN}=C_{OUT}=1uF ,C_{BP}=22nF ,T_A=25℃,unless otherwise noted.)

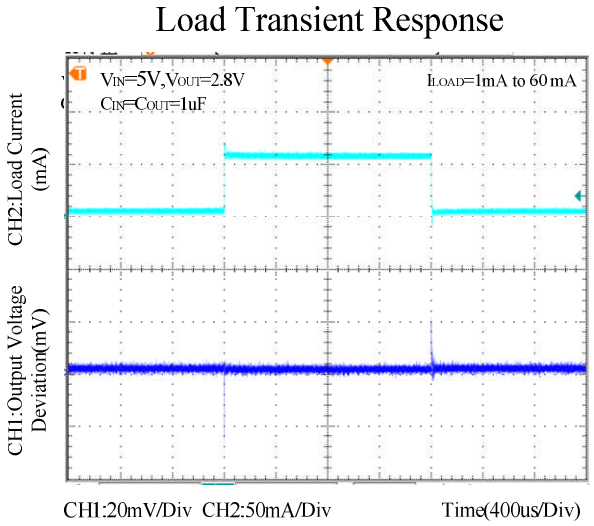
Parameter		Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage		V_{IN}		2.5		5.5	V
Output Voltage Accuracy(Note 6)		ΔV_{OUT}	$V_{IN=}$3.6V, I_{OUT}=1mA	-1		+1	%
				-2		+2	
Current Limit		I_{LIM}	R_{LOAD}=1Ω	400	430		mA
Quiescent Current		I_Q	V_{EN}>1.2V, I_{OUT}=0mA		90	130	uA
Dropout Voltage		V_{DROP}	I_{OUT}=200mA, V_{OUT}=2.8V		130	180	mV
			I_{OUT}=300mA, V_{OUT}=2.8V		210	300	
Line Regulation		ΔV_{LINE}	V_{IN}=3.6V to 5.5V I_{OUT}=1mA			0.2	%
Load Regulation		ΔV_{LOAD}	1mA<I_{OUT}<300mA			0.5	%
Standby Current		I_{STBY}	V_{EN}=GND, Shutdown		0.01	1	uA
EN Input Bias Current		I_{IBSD}	V_{EN}=GND or V_{IN}		0	100	nA
EN Input Threshold	Logic Low	V_{IL}	V_{IN}=3V to 5.5V, Shutdown			0.4	V
	Logic High	V_{IH}	V_{IN}=3V to 5.5V, Start up	1.2			V
Power Supply Rejection Ratio	f=217Hz	PSRR	Cout=1uF, Iout=100mA		-72		dB
	f=10KHz				-70		
Thermal Shutdown Temperature		T_{SD}	Shutdown,Temp increasing		165		℃
Thermal Shutdown Hysteresis		T_{SDHY}			30		℃

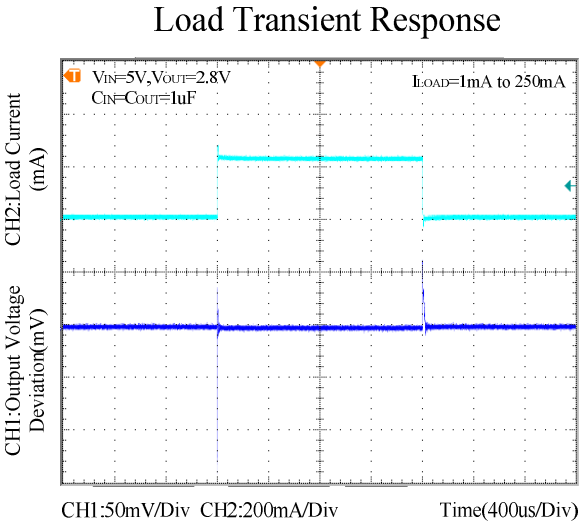
Note 5: 100% production test at +25°C. Specifications over the temperature range are guaranteed by design and characterization.
Note 6: This IC includes two kinds of output voltage accuracy versions.A：±1%, B：±2%.

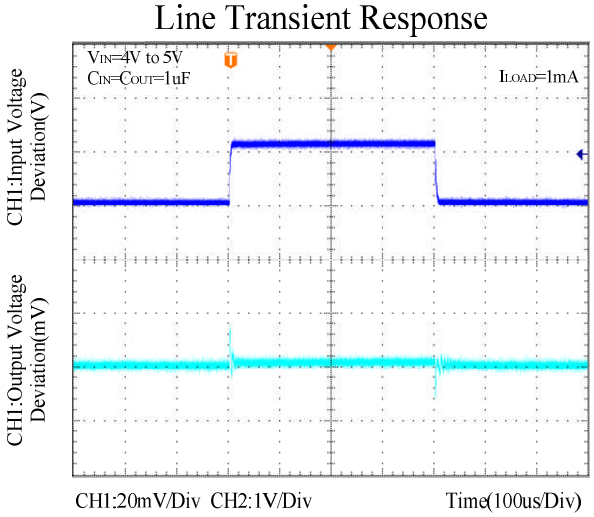
Typical Performance Characteristics

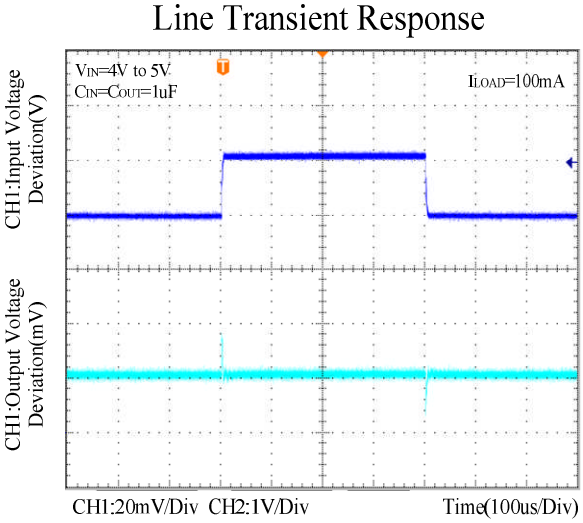






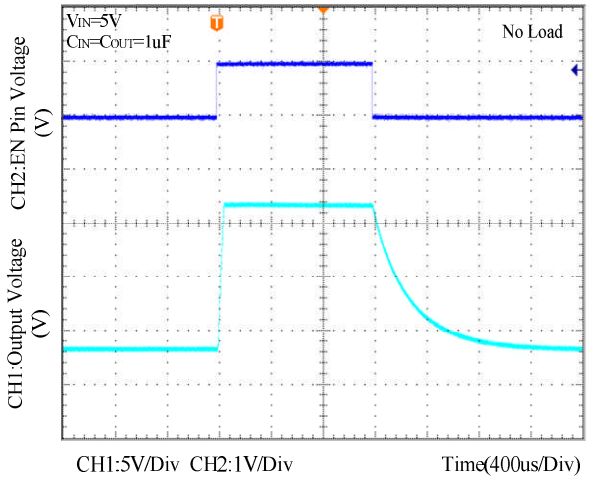




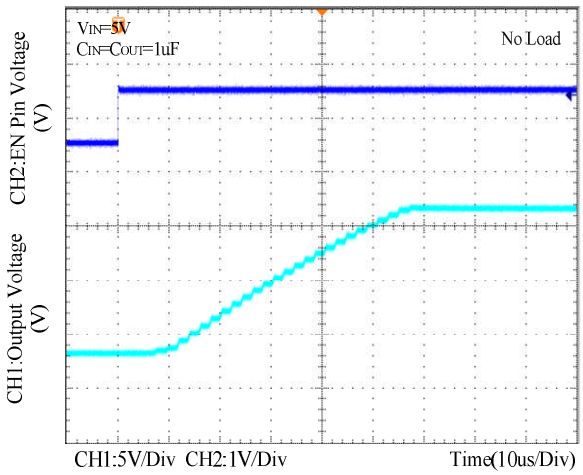


Typical Performance Characteristics

EN Pin Shutdown Response



Start Up



Applications Information

Like any low-dropout regulator, the external capacitors used with the LR9193 must be carefully selected for regulator stability and performance. Using a capacitor whose value is > 1μF on the LR9193 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LR9193 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF with ESR is > 25mΩ on the LR9193 output ensures stability. The LR 9193 still works well with output capacitor of other types due to the wide stable ESR range . Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LR9193 and returned to a clean analog ground.

Bypass Capacitor and Low Noise

Connecting a 22nF between the BP pin and GND pin significantly reduces noise on the regulator output, it is critical that the capacitor connection between the BP pin and GND pin be direct and PCB traces should be as short as possible. There is a relationship between the bypass capacitor value and the LDO regulator turn on time. DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance.

Enable Function

The LR9193 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For to protect the system, the LR9193 have a quick

discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

Thermal Considerations

Thermal protection limits power dissipation in LR9193. When the operation junction temperature exceeds 165°C, the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turn on again after the junction temperature cools by 30°C.
For continue operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$$P_D = (V_{IN}-V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_D(\max) = (T_J(\max) - T_A) / \theta_{JA}$$

Where $T_J(\max)$ is the maximum operation junction temperature 125°C, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance. For recommended operating conditions specification of LR9193, where $T_J(\max)$ is the maximum junction temperature of the die (125°C) and T_A is the maximum ambient temperature. The junction to ambient thermal resistance (θ_{JA} is layout dependent) for SOT -23-5 package is 250°C/W, SC-70-5 package is 333°C/W, on standard JEDEC 51- 3 thermal test board. The maximum power dissipation at T_A= 25° C can be calculatedby following formula :

$P_D(\max)$ = (125°C−25°C) / 333 = 300mW (SC-70-5)

$P_D(\max)$ = (125°C −25°C) / 250 = 400mW (SOT-23-5)

The maximum power dissipation depends on operating ambient temperature for fixed $T_J(\max)$ and thermal resistance θ_{JA}. It is also useful to calculate the junction of temperature of the LR9193 under a set of specific condtions.In this exmaple let the Input voltage V_{IN} =3.3V,the output current Io=300mA and the case temperature T_A=40 °C measured by a thermalcouple during operation. The power dissipation for the Vo=2.8V version of the LR9193 can be calculated as:

P_D =(3.3V−2.8V)*300mA+3.6V*100uA
=150mW

And the junction temperature,T_J ,can be calculated as follows:

$T_J=T_A+P_D*\theta_{JA}$=40°C+0.15W*250°C/W
=40°C+37.5°C=77.5°C<$T_J(\max)$=125°C

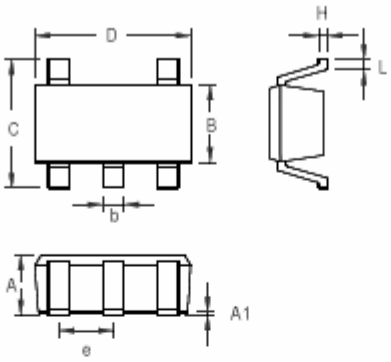
For this operating condition,TJ is lower than the absolute maximum operating junction temperature,125°C, so it is safe to use the LR9193 in this configuration.

Layout considerations

To improve ac performance such as PSRR, output noise,and transient response, it is recommended that the PCB be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addidion, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

Package Description

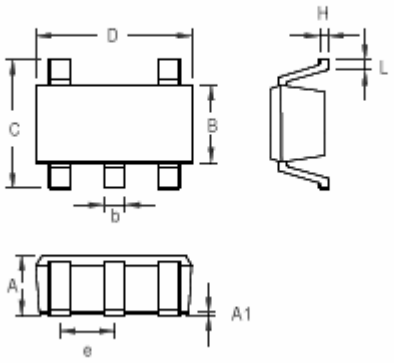
SC70-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.044
A1	0.000	0.100	0.000	0.004
B	1.150	1.350	0.045	0.054
b	0.150	0.400	0.006	0.016
C	1.800	2.450	0.071	0.096
D	1.800	2.250	0.071	0.089
e	0.650		0.026	
H	0.080	0.260	0.003	0.010
L	0.210	0.460	0.008	0.018

SC-70-5 Surface Mount Package

SOT23-5



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5 Surface Mount Package