

- Designed to be Interchangeable with AMD AM29821 and AM29822
- Ideal for Data Synchronization of Wider Data Paths
- Provide Extra Data Width Necessary for Wider Address/Data Paths or Buses with Parity
- Outputs Have Undershoot Production Circuitry
- Power-Up High Impedance State
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Buffered Control Inputs to Reduce DC Loading Effects
- Dependable Texas Instruments Quality and Reliability

**description**

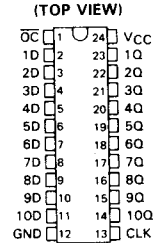
These 10-bit flip-flops feature three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. They are particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The ten flip-flops are edge-triggered D-type flip-flops. On the positive transition of the clock the Q outputs on the 'AS29821 will be true, and on the 'AS29822 will be complementary, to the data input.

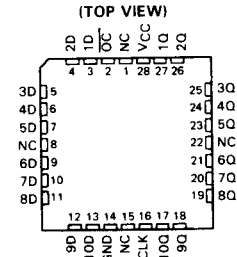
A buffered output control input can be used to place the ten outputs in either a normal logic state (high or low levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive the bus lines in a bus-organized system without need for interface or pull-up components.

The output control ( $\overline{OC}$ ) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

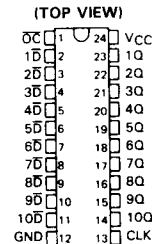
SN54AS29821 . . . JT PACKAGE  
SN74AS29821 . . . DW OR NT PACKAGE



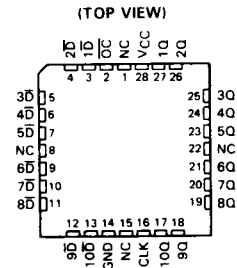
SN54AS29821 . . . FK PACKAGE  
SN74AS29821 . . . FN PACKAGE



SN54AS29822 . . . JT PACKAGE  
SN74AS29822 . . . DW OR NT PACKAGE



SN54AS29822 . . . FK PACKAGE  
SN74AS29822 . . . FN PACKAGE



NC—No internal connection

PRODUCT PREVIEW documents contain information on products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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# SN54AS29821, SN54AS29822, SN74AS29821, SN74AS29822

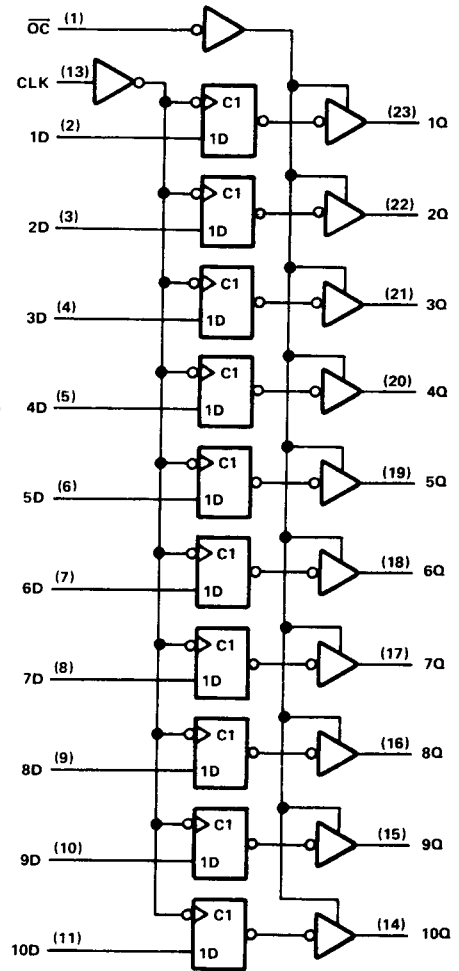
## 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

The SN54AS29821 and SN54AS29822 are characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74AS29821 and SN74AS29822 are characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

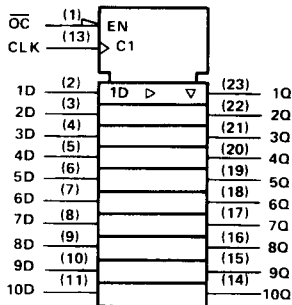
'AS29821 FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{\text{OC}}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	$Q_0$
H	X	X	Z

'AS29821 logic diagram (positive logic)



'AS29821 logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.

2

ALS and AS Circuits

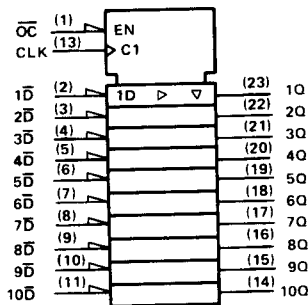
# SN54AS29822, SN74AS29822

## 10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

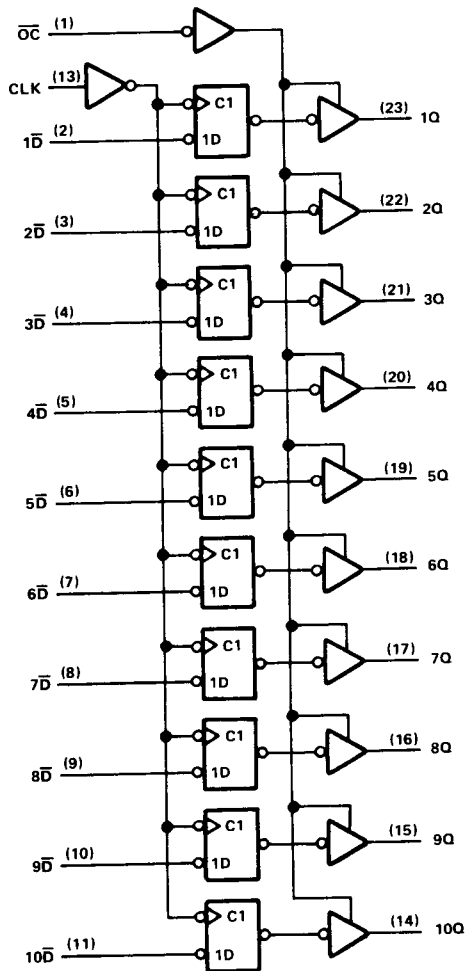
'AS29822 FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{OC}$	CLK	$\overline{D}$	Q
L	1	H	L
L	1	L	H
L	L	X	$Q_0$
H	X	X	Z

'AS29822 logic symbol†



'AS29822 logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for DW, JT, and NT packages.