

DESCRIPTION

This family is a 16M bit dynamic RAM organized 1,048,576 x 16-bit configuration with Extended Data Out mode CMOS DRAMs. Extended Data Out mode offers high speed random access of memory cells within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(60,70 or 80ns) and refresh cycle(1K Ref. or 4K Ref.) and package type(SOJ or TSOP-II) and power consumption(Normal or Low power with self refresh). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

ORDERING INFORMATION

Part Number	Ref.	Power	Pkg.
HY51V18164CJC	1K		SOJ
HY51V18164CSLJC	1K	SL-part	SOJ
HY51V18164CTC	1K		TSOP-II
HY51V18164CSLTC	1K	SL-part	TSOP-II
HY51V16164CJC	4K		SOJ
HY51V16164CSLJC	4K	SL-part	SOJ
HY51V16164CTC	4K		TSOP-II
HY51V16164CSLTC	4K	SL-part	TSOP-II

* Reverse TSOP-II packages are also available

FEATURES

- Part Number Information
 - HY51V18164C: 1K Ref.
 - HY51V16164C: 4K Ref.
- Max. Active Power Dissipation

Speed	1K	4K
60	540 mW	324 mW
70	468 mW	288 mW
80	432 mW	252 mW

- Fast access time and cycle time

Speed	t _{TRAC}	t _{CAC}	t _{HPC}
60ns	60ns	15ns	25ns
70ns	70ns	20ns	30ns
80ns	80ns	20ns	35ns

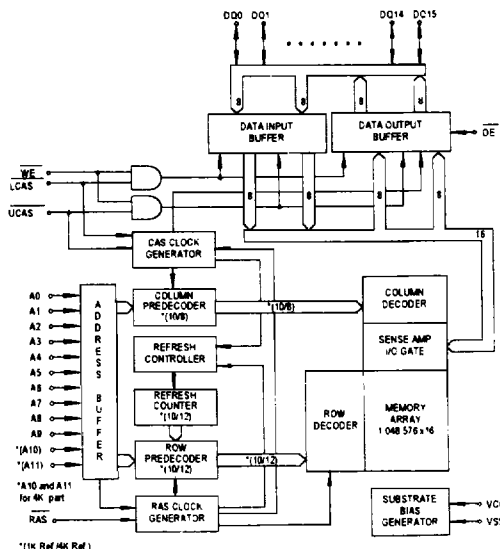
- Extended Data Out Operation
- Single power supply of 3.3V ± 0.3V
- Read-Modify-Write Capability
- Early Write or Output Enable controlled write
- LVTTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self Refresh Capability
- Refresh cycles

Part No.	Ref.	Normal	SL-part
HY51V18164C	1K	16ms	256ms
HY51V16164C	4K	64ms	

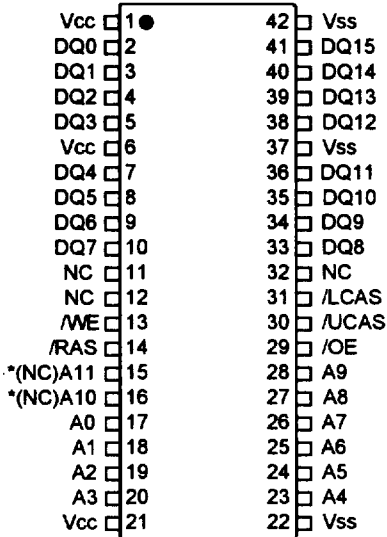
- JEDEC standard pinout
 - 42-pin Plastic SOJ (400 mil)
 - 44/50-pin Plastic TSOP-II (400mil)

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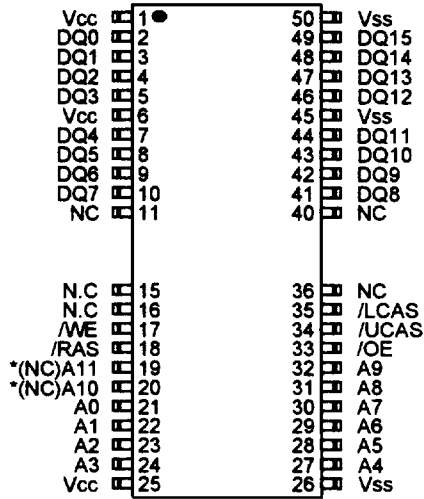
BLOCK DIAGRAM



PIN CONFIGURATION (Marking Side)



42-pin Plastic SOJ (400mil)



44/50-pin Plastic TSOP-II (400mil)

*(N.C) : For 1K Refresh product

PIN DESCRIPTION

/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0-A11	Address Inputs (4K Product)
A0-A9	Address Inputs (1K Product)
DQ0-DQ15	Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground
NC	No Connection

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin relative to Vss	-0.5 to 4.6	V
VCC	Voltage on Vcc relative to Vss	-0.5 to 4.6	V
IOS	Short Circuit Output Current	50	mA
PD	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature · Time	260 · 10	°C · sec

Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA=0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Power Supply Voltage	3.0	3.3	3.6	V
VIH	Input High Voltage	2.0	-	VCC+0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

Note: All voltages are referenced to Vss.

DC CHARACTERISTICS

($T_A=0^{\circ}\text{C}$ to 70°C , $V_{CC}=3.3\text{V} \pm 0.3\text{V}$ and $V_{SS}=0\text{V}$, unless otherwise noted.)

Symbol	Parameter	Test Condition	Speed/ Power	Max. Current		UNIT
				1K Ref	4K Ref	
I _{CC1}	Operating Current	/RAS and /CAS cycling t _{RC} =t _{RC} (min.)	60	150	90	mA
			70	130	80	
			80	120	70	
I _{CC2}	LVTTTL Standby Current	/RAS=/CAS ≥ V _{IH} other inputs ≥ V _{SS}	SL-part	1 1	1 1	mA
I _{CC3}	/RAS-only Refresh Current	/CAS=V _{IH} , /RAS cycling t _{RC} =t _{RC} (min.)	60	150	90	mA
			70	130	80	
			80	120	70	
I _{CC4}	EDO Mode Current	/RAS=V _{IL} , /CAS, Address cycling t _{HPC} =t _{HPC} (min.)	60	100	90	mA
			70	90	80	
			80	80	70	
I _{CC5}	CMOS Standby Current	/RAS = /CAS ≥ V _{CC} -0.2V	SL-part	500 150	500 150	μA μA
I _{CC6}	/CAS-before- /RAS Refresh Current	/RAS and /CAS cycling t _{RC} =t _{RC} (min.)	60	150	90	mA
			70	130	80	
			80	120	70	
I _{CC7}	Battery Back-up Current (SL-part)	t _{RC} =250 μs (1K Ref), 62.5 μs (4KRef) /CAS = CBR cycling or 0.2V /OE & /WE=V _{CC} - 0.2V Address =V _{CC} -0.2V or 0.2V DQ0-DQ15=V _{CC} -0.2V, 0.2V or open	t _{RAS} ≤ 300ns	250	300	μA
I _{CC8}	Self Refresh Current (SL-part)	/RAS & /CAS = 0.2V Other pins are same as I _{CC7}		250	250	μA

Symbol	Parameter	Test condition	Min.	Max.	UNIT
I _{LI}	Input Leakage current (Any Input Pin)	V _{SS} ≤ V _{IN} ≤ V _{CC} + 0.3 All other pins not under test=V _{SS}	-1	1	μA
I _{LO}	Output Leakage current (Any Input Pin)	V _{SS} ≤ V _{OUT} ≤ V _{CC} /RAS & /CAS at V _{IH}	-1	1	μA
V _{OL}	Output Low Voltage	I _{OL} = 2.0mA	-	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -2.0mA	2.4	-	V

NOTE

- I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on output loading and cycle rates(t_{RC} and t_{HPC}).
- Specified values are obtained with outputs unloaded.
- I_{CC} is specified as an average current. In I_{CC1}, I_{CC3}, I_{CC6}, address can be changed only once while /RAS=V_{IL}. In I_{CC4}, address can be changed maximum once while /CAS=V_{IH} within one EDO mode cycle time t_{HPC}.
- Only /RAS(max.) = 1 μs is applied to refresh of battery backup but t_{RAS}(max.) = 10 μs is to applied to normal functional operation.
- I_{CC5}(max.) = 150 μA, I_{CC7} and I_{CC8} are applied to SL-part only.
- /CAS means /LCAS or /UCAS cycle.

AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{cc}=3.3V ± 0.3V and V_{ss}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HY51V18164C / HY51V16164C						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t _{RC}	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	t _{RWC}	Read-Modify-Write Cycle Time	150	-	180	-	200	-	ns	
3	t _{HPC}	EDO Mode Cycle Time	25	-	30	-	35	-	ns	2
4	t _{HPRWC}	EDO Mode Read-Modify-Write Cycle Time	80	-	95	-	105	-	ns	2
5	t _{RAC}	Access Time from /RAS	-	60	-	70	-	80	ns	5,6,7
6	t _{CAC}	Access Time from /CAS	-	15	-	20	-	20	ns	5,6
7	t _{AA}	Access Time from Column Address	-	30	-	35	-	40	ns	5,7
8	t _{CPA}	Access Time from Column Precharge	-	35	-	40	-	45	ns	5
9	t _{CLZ}	/CAS to Output Low Impedance	0	-	0	-	0	-	ns	5
10	t _{CEZ}	Out Buffer Turn-Off Delay Time from /CAS	3	15	3	15	3	20	ns	8
11	t _T	Transition Time (Rise and Fall)	2	50	2	50	2	50	ns	3
12	t _{RP}	/RAS Precharge Time	40	-	50	-	60	-	ns	
13	t _{RAS}	/RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	t _{RASP}	/RAS Pulse Width (EDO Mode)	60	100K	70	100K	80	100K	ns	
15	t _{RSH}	/RAS Hold Time	15	-	20	-	20	-	ns	
16	t _{CSH}	/CAS Hold Time	40	-	50	-	60	-	ns	
17	t _{CAS}	/CAS Pulse Width	13	10K	15	10K	20	10K	ns	
18	t _{RCD}	/RAS to /CAS Delay Time	20	45	20	50	20	60	ns	6
19	t _{RAD}	/RAS to Column Address Delay Time	15	30	15	35	15	40	ns	7
20	t _{CRP}	/CAS to /RAS Precharge Time	5	-	5	-	5	-	ns	11
21	t _{CP}	/CAS Precharge Time	7	-	10	-	10	-	ns	16
22	t _{ASR}	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	t _{RAH}	Row Address Hold Time	10	-	10	-	10	-	ns	
24	t _{ASC}	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	t _{CAH}	Column Address Hold Time	15	-	15	-	15	-	ns	
26	t _{RAL}	Column Address to /RAS Lead Time	30	-	35	-	40	-	ns	
27	t _{RCS}	Read Command Set-up Time	0	-	0	-	0	-	ns	
28	t _{RCH}	Read Command Hold Time Referenced to /CAS	0	-	0	-	0	-	ns	9
29	t _{RRH}	Read Command Hold Time Referenced to /RAS	0	-	0	-	0	-	ns	9
30	t _{WCH}	Write Command Hold Time	15	-	15	-	15	-	ns	
31	t _{WP}	Write Command Pulse Width	10	-	15	-	15	-	ns	
32	t _{RWL}	Write Command to /RAS Lead Time	15	-	20	-	20	-	ns	
33	t _{CWL}	Write Command to /CAS Lead Time	15	-	20	-	20	-	ns	16
34	t _{DS}	Data-In Set-up Time	0	-	0	-	0	-	ns	10
35	t _{DH}	Data-In Hold Time	15	-	15	-	15	-	ns	10

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AC CHARACTERISTICS

(Continued)

#	SYMBOL	PARAMETER	HY51V18164C / HY51V16164C						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
36	tREF	Refresh Period (1024 cycles)	16	-	16	-	16	-	ms	
		Refresh Period (4096 cycles)	64	-	64	-	64	-	ms	
		Refresh Period (SL-part)	256	-	256	-	256	-	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	11
38	tCWD	/CAS to /WE Delay Time	35	-	40	-	45	-	ns	11,15
39	tRWD	/RAS to /WE Delay Time	80	-	95	-	105	-	ns	11
40	tAWD	Column Address to /WE Delay Time	50	-	60	-	65	-	ns	11
41	tCSR	/CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	17
42	tCHR	/CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	18
43	tRPC	/RAS to /CAS Precharge Time	5	-	5	-	5	-	ns	
44	tCPT	/CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	14
45	tROH	/RAS Hold Time Reference to /OE	10	-	10	-	10	-	ns	
46	tOEA	/OE Access Time	-	15	-	20	-	20	ns	
47	tOED	/OE to Data Delay Time	15	-	20	-	20	-	ns	
48	tOEZ	Output Buffer Turn Off Delay Time from /OE	3	15	3	15	3	20	ns	8
49	tOEH	/OE Command Hold Time	15	-	20	-	20	-	ns	
50	tCPWD	/WE Delay Time from /CAS Precharge	55	-	65	-	75	-	ns	11
51	tRHCP	/RAS Hold Time from /CAS Precharge	35	-	40	-	45	-	ns	
52	tWRP	/WE to /RAS Precharge Time(CBR cycle)	10	-	10	-	10	-	ns	
53	tWRH	/WE to /RAS Hold Time (CBR cycle)	10	-	10	-	10	-	ns	
54	tRASS	/RAS Pulse Width (Self Refresh)	100	-	100	-	100	-	μs	
55	tRPS	/RAS Precharge Time (Self Refresh)	110	-	130	-	150	-	ns	
56	tCHS	/CAS Hold Time (Self Refresh)	-50	-	-50	-	-50	-	ns	
57	tDOH	Output Data Hold Time	5	-	5	-	5	-	ns	
58	tREZ	Output Buffer Turn Off Delay Time from /RAS	3	15	3	15	3	20	ns	
59	tWEZ	Output Buffer Turn Off Delay Time from /WE	3	15	3	15	3	20	ns	
60	tWED	/WE to Data Delay Time	15	-	15	-	15	-	ns	
61	tOEP	/OE Precharge Time	5	-	8	-	10	-	ns	
62	tWPE	/WE Pulse Width (EDO cycle)	5	-	8	-	10	-	ns	
63	tOCH	/OE to /CAS Hold Time	0	-	0	-	0	-	ns	
64	tCHO	/CAS Hold Time to /OE	5	-	8	-	10	-	ns	

NOTE

1. An initial pause of 200 μs is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS only refresh cycles are required.
2. $t_{ASC} \geq t_{CP}(\text{min.})$, assume $T = 2\text{ns}$
3. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Transition times are measured between $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$
4. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($T_A = 0$ to 70°C) is assured.
5. Measured at $V_{OH} = 2.0\text{V}$ and $V_{OL} = 0.8\text{V}$ with a load equivalent to 1 TTL loads and 100pF.
6. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC}
7. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA}
8. $t_{CEZ}(\text{max.})$, $t_{OEZ}(\text{max.})$, $t_{REZ}(\text{max.})$ and $t_{WEZ}(\text{max.})$ define the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. These parameters are referred to /LCAS or /UCAS leading edge in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
11. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{RWD} \geq t_{RWD}(\text{min.})$ and $t_{CPWD} \geq t_{CPWD}(\text{min.})$, then the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above conditions is satisfied, the condition of the data out is indeterminate.
12. If /RAS goes to high before /CAS high going, the open circuit condition of the output is achieved by /CAS high going. If /CAS goes to high before /RAS high going, the open circuit condition of the output is achieved by /RAS high going.
13. t_{ASC} and t_{CAH} are referred to the earlier /CAS falling edge.
14. t_{CP} and t_{CPT} are measured when both /LCAS and /UCAS are high state.
15. t_{CWD} is referred to the later /CAS falling edge at Read-Modify-Write cycle.
16. t_{CWL} must be satisfied by both /LCAS and /UCAS for 16-bit access cycles.
17. t_{CSR} is referred to the earlier /CAS falling low before /RAS transition low.
18. t_{CHR} is referred to the later /CAS rising high after /RAS transition low.
19. t_{DS} , t_{DH} is independently specified for lower byte DQ(0-7), upper byte DQ(8-15).

CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$, $V_{SS} = 0\text{V}$ and $f = 1\text{MHz}$, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0 - A11)	-	5	pF
CIN2	Input Capacitance (/RAS, /LCAS, /UCAS, /WE, /OE)	-	7	pF
CDQ	Data Input /Output Capacitance (DQ0 - DQ15)	-	7	pF

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