National Semiconductor

January 2006

LM101AJAN
Operational Amplifiers

General Description

The LM101A is a general purpose operational amplifier which features improved performance over industry standards such as the LM709. Advanced processing techniques make possible an order of magnitude reduction in input currents, and a redesign of the biasing circuitry reduces the temperature drift of input current. Improved specifications include:

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/µs as a summing amplifier

This amplifier offers many features which make its application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations and compensation with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

In addition, the device provides better accuracy and lower noise in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators or timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and a drift at a lower cost.

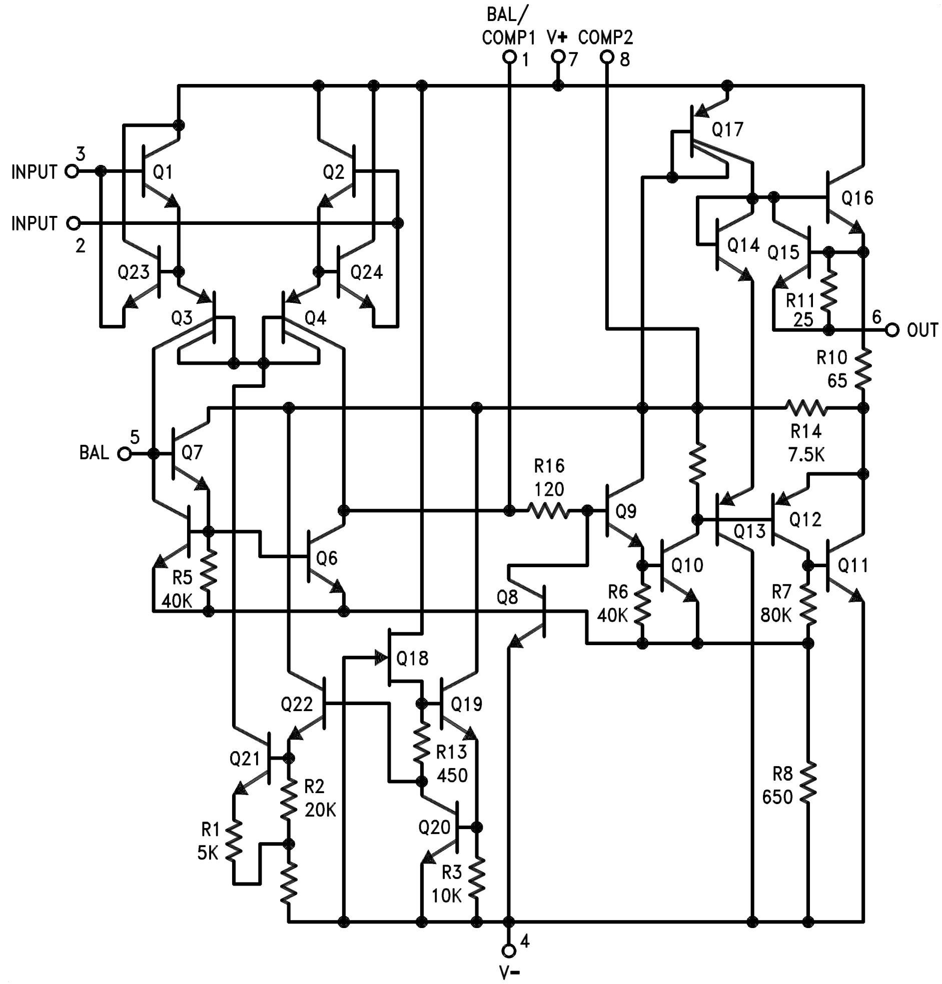
Features

- Offset voltage 3 mV maximum over temperature
- Input current 100 nA maximum over temperature
- Offset current 20 nA maximum over temperature
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10 V/µS as a summing amplifier

Ordering Information

NS Part Number	SMD Part Number	NS Package Number	Package Description
JL101ABGA	JM38510/10103BGA	H08C	8LD Metal Can
JL101ABPA	JM38510/10103BPA	J08A	8LD CERDIP
JL101ABHA	JM38510/10103BHA	W10A	10LD CERPACK
JL101ABCA	JM38510/10103BCA	J14A	14LD CERDIP
JL101ASGA	JM38510/10103SGA	H08C	8LD Metal Can
JL101ASPA	JM38510/10103SPA	J08A	8LD CERDIP

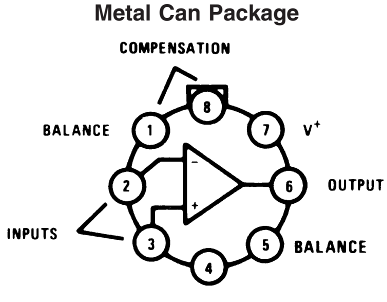
Schematic (Note 8)



20129601

Connection Diagrams

(Top View)
Metal Can Package

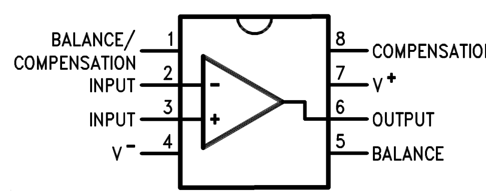


20129602

Note: Pin 4 connected to case.

See NS Package Number H08C

(Top View)
Dual-In-Line Package

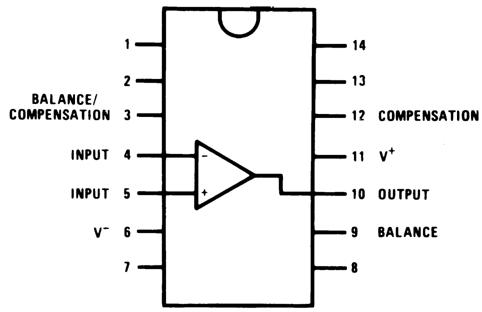


20129604

See NS Package Number J08A

Connection Diagrams (Continued)

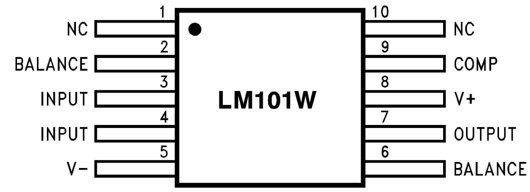
(Top View)
Dual-In-Line Package



20129603

See NS Package Number J14A

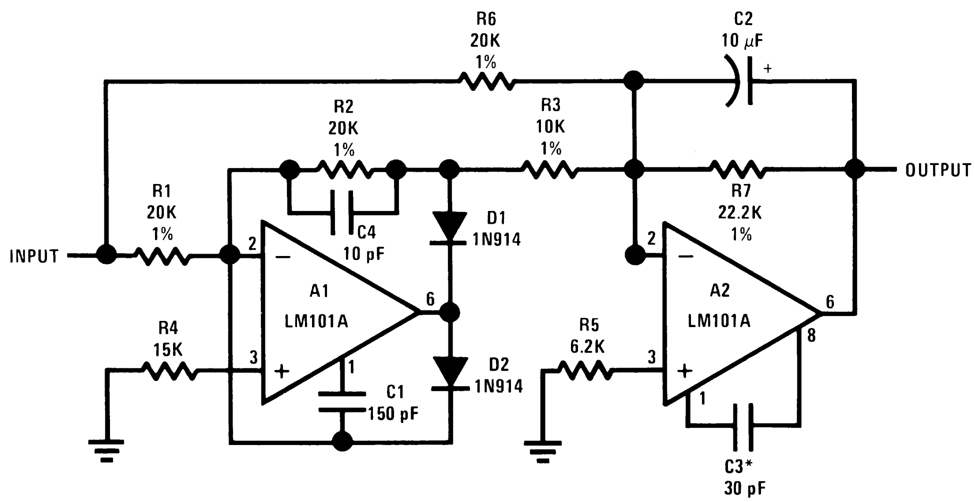
(Top View)
Ceramic Flatpack Package



20129640

See NS Package Number W10A

Fast AC/DC Converter



20129633

Note 1: Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Absolute Maximum Ratings (Note 2)

Supply Voltage	±22V
Differential Input Voltage	±30V
Input Voltage (Note 3)	±15V
Output Short Circuit Duration	Continuous
Operating Ambient Temp. Range	$-55^\circ C \leq T_A \leq +125^\circ C$
T_J Max	150˚C
Power Dissipation at T_A = 25˚C (Note 4)	
H-Package	
(Still Air)	750 mW
(500 LF / Min Air Flow)	1,200 mW
J8-Package	
(Still Air)	1,000 mW
(500 LF / Min Air Flow)	1,500 mW
J14-Package	
(Still Air)	1,200mW
(500 LF / Min Air Flow)	2,000mW
W-Package	
(Still Air)	500mW
(500 LF / Min Air Flow)	800mW
Thermal Resistance	
θ_{JA}	
H-Package	
(Still Air)	165˚C/W
(500 LF / Min Air Flow)	89˚C/W
J8-Package	
(Still Air)	128˚C/W
(500 LF / Min Air Flow)	75˚C/W
J14-Package	
(Still Air)	98˚C/W
(500 LF / Min Air Flow)	59˚C/W
W-Package	
(Still Air)	233˚C/W
(500 LF / Min Air Flow)	155˚C/W
θ_{JC} (Typical)	
H-Package	39˚C/W
J8-Package	26˚C/W
J14-Package	24˚C/W
W-Package	26˚C/W
Storage Temperature Range	$-65^\circ C \leq T_A \leq +150^\circ C$
Lead Temperature (Soldering, 10 sec.)	300˚C
ESD Tolerance (Note 5)	3000V

Quality Conformance Inspection

Mil-Std-883, Method 5005 - Group A

Subgroup	Description	Temp (˚C)
1	Static tests at	25
2	Static tests at	125
3	Static tests at	-55
4	Dynamic tests at	25
5	Dynamic tests at	125
6	Dynamic tests at	-55
7	Functional tests at	25
8A	Functional tests at	125
8B	Functional tests at	-55
9	Switching tests at	25
10	Switching tests at	125
11	Switching tests at	-55

LM101A JAN Electrical Characteristics

DC Parameters

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
V_{IO}	Input Offset Voltage	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = +15V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		V_{CM} = 0V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V		-2.0	+2.0	mV	1
				-3.0	+3.0	mV	2, 3
I_{IO}	Input Offset Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = +15V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		V_{CM} = 0V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V, R_S = 100KΩ		-10	+10	nA	1, 2
				-20	+20	nA	3
$\pm I_{IB}$	Input Bias Current	$+V_{CC}$ = 35V, $-V_{CC}$ = -5V, V_{CM} = -15V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -35V, V_{CM} = +15V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		V_{CM} = 0V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
		$+V_{CC}$ = 5V, $-V_{CC}$ = -5V, V_{CM} = 0V, R_S = 100KΩ		-0.1	75	nA	1, 2
				-0.1	100	nA	3
+PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 10V, $-V_{CC}$ = -20V		-50	+50	μV/V	1
				-100	+100	μV/V	2, 3
-PSRR	Power Supply Rejection Ratio	$+V_{CC}$ = 20V, $-V_{CC}$ = -10V		-50	+50	μV/V	1
				-100	+100	μV/V	2, 3

LM101A JAN Electrical Characteristics (Continued)

DC Parameters (Continued)

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameters	Conditions	Notes	Min	Max	Unit	Sub-groups
CMRR	Common Mode Rejection Ratio	V_{CC} = ±35V to ±5V, V_{CM} = ±15V		80		dB	1, 2, 3
$+V_{IO}$ Adj	Adjustment for Input Offset Voltage			4.0		mV	1, 2, 3
$-V_{IO}$ Adj	Adjustment for Input Offset Voltage				-4.0	mV	1, 2, 3
$+I_{OS}$	Output Short Circuit Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, t ≤ 25mS, V_{CM} = -15V		-60		mA	1, 2, 3
$-I_{OS}$	Output Short Circuit Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V, t ≤ 25mS, V_{CM} = +15V			+60	mA	1, 2, 3
I_{CC}	Power Supply Current	$+V_{CC}$ = 15V, $-V_{CC}$ = -15V			3.0	mA	1
					2.32	mA	2
					3.5	mA	3
ΔV_{IO} / ΔT	Temperature Coefficient of Input Offset Voltage	-55˚C ≤ T_A ≤ +25˚C	(Note 6)	-18	+18	µV/˚C	2
		+25˚C ≤ T_A ≤ +125˚C	(Note 6)	-15	+15	µV/˚C	3
Δ I_{IO} / ΔT	Temperature Coefficient of Input Offset Current	-55˚C ≤ T_A ≤ +25˚C	(Note 6)	-200	+200	pA/˚C	2
		+25˚C ≤ T_A ≤ +125˚C	(Note 6)	-100	+100	pA/˚C	3
$-A_{VS}$	Large Signal (Open Loop) Voltage Gain	R_L = 2KΩ, V_O = -15V	(Note 7)	50		V/mV	4
			(Note 7)	25		V/mV	5, 6
		R_L = 10KΩ, V_O = -15V	(Note 7)	50		V/mV	4
			(Note 7)	25		V/mV	5, 6
$+A_{VS}$	Large Signal (Open Loop) Voltage Gain	R_L = 2KΩ, V_O = +15V	(Note 7)	50		V/mV	4
			(Note 7)	25		V/mV	5, 6
		R_L = 10KΩ, V_O = +15V	(Note 7)	50		V/mV	4
			(Note 7)	25		V/mV	5, 6
A_{VS}	Large Signal (Open Loop) Voltage Gain	V_{CC} = ±5V, R_L = 2KΩ, V_O = ±2V	(Note 7)	10		V/mV	4, 5, 6
		V_{CC} = ±5V, R_L = 10KΩ, V_O = ±2V	(Note 7)	10		V/mV	4, 5, 6
$+V_{OP}$	Output Voltage Swing	R_L = 10KΩ, V_{CM} = -20V		+16		V	4, 5, 6
		R_L = 2KΩ, V_{CM} = -20V		+15		V	4, 5, 6
$-V_{OP}$	Output Voltage Swing	R_L = 10KΩ, V_{CM} = 20V			-16	V	4, 5, 6
		R_L = 2KΩ, V_{CM} = 20V			-15	V	4, 5, 6

AC Parameters

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
+SR	Slew Rate	A_V = 1, V_I = -5V to +5V		0.3		V/µS	7
-SR	Slew Rate	A_V = 1, V_I = +5V to -5V		0.3		V/µS	7
TR_{TR}	Rise Time	A_V = 1, V_I = 50mV			800	nS	7
TR_{OS}	Overshoot	A_V = 1, V_I = 50mV			25	%	7
NI_{BB}	Noise Broadband	BW = 10Hz to 5KHz, R_S = 0Ω			15	$µV_{RMS}$	7
NI_{PC}	Noise Popcorn	BW = 10Hz to 5KHz, R_S = 100KΩ			80	$µV_{PK}$	7

LM101A JAN Electrical Characteristics (Continued)

DC Parameters: Drift Values

The following conditions apply to all parameters, unless otherwise specified

V_{CC} = ±20V, V_{CM} = 0V, R_S = 50Ω

Delta calculations performed on JAN S devices at group B, Subgroup 5 only.

Symbol	Parameter	Conditions	Notes	Min	Max	Units	Sub-groups
V_{IO}	Input Offset Voltage	V_{CM} = 0V		-0.5	0.5	mV	1
± I_{IB}	Input Bias Current	V_{CM} = 0V, R_S = 100KΩ		-7.5	7.5	nA	1

Notes

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions for which the device is intended to be functional, but do no guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{Jmax} (maximum junction temperature), θ_{JA} (package junction to ambient thermal resistance), and T_A (ambient temperature). The maximum allowable power dissipation at any temperature is $P_{Dmax} = (T_{Jmax} - T_A) / \theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower.

Note 5: Human body model, 100 pF discharged through 1.5 kΩ.

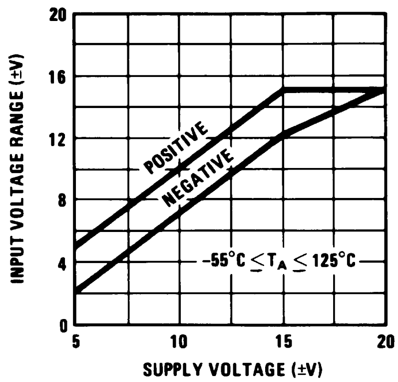
Note 6: Calculated parameter

Note 7: Datalog reading of K = V/mV.

Note 8: Pin connections shown are for 8-pin packages.

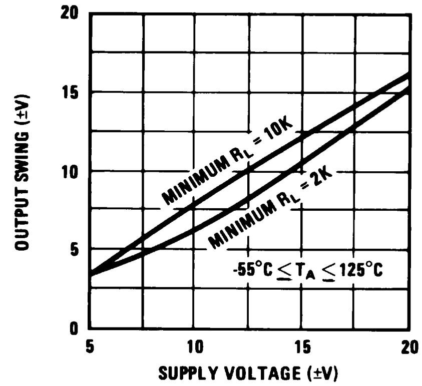
Typical Performance Characteristics LM101A

Input Voltage Range



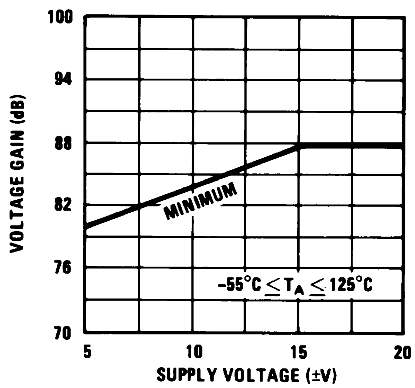
20129641

Output Swing



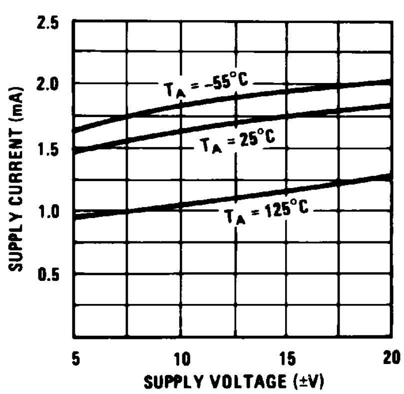
20129642

Voltage Gain



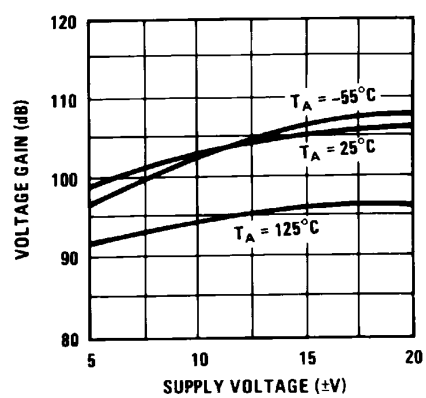
20129643

Supply Current



20129647

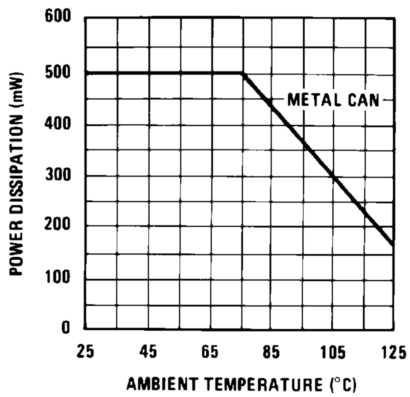
Voltage Gain



20129648

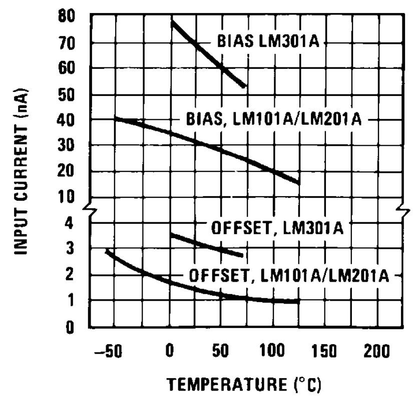
Typical Performance Characteristics LM101A (Continued)

Maximum Power Dissipation



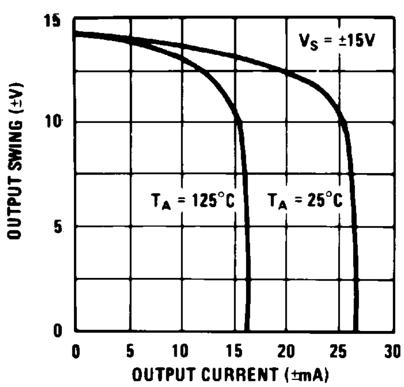
20129649

Input Current, LM101A



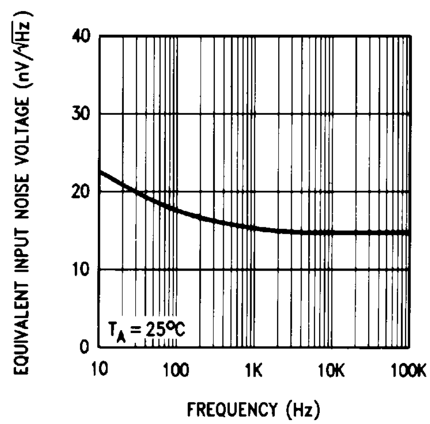
20129650

Current Limiting



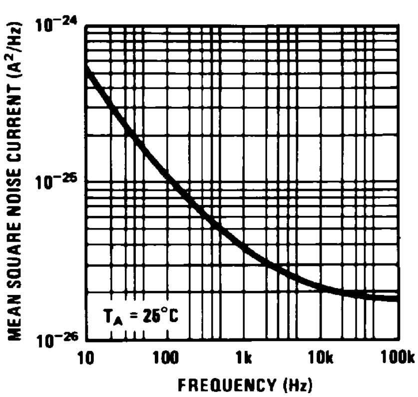
20129651

Input Noise Voltage



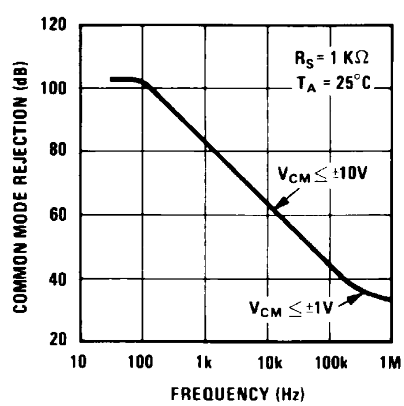
20129652

Input Noise Current



20129653

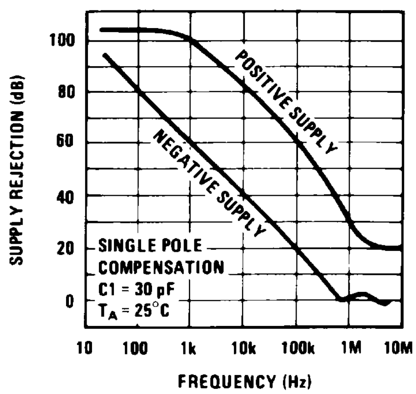
Common Mode Rejection



20129654

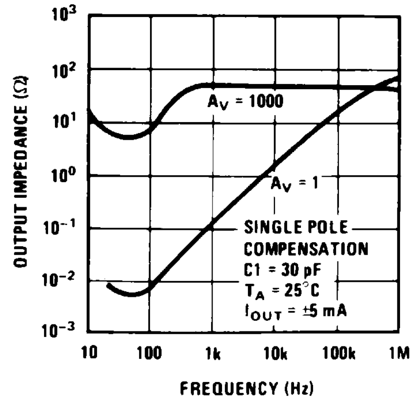
Typical Performance Characteristics LM101A (Continued)

Power Supply Rejection



20129655

Closed Loop Output Impedance

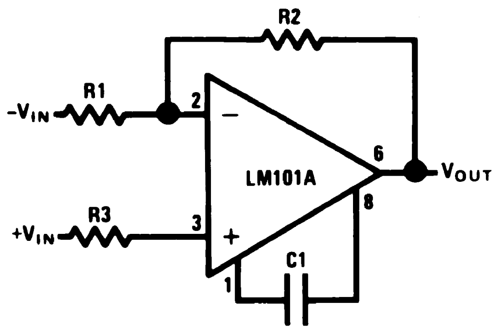


20129656

Typical Performance Characteristics for Various Compensation Circuits

(Note 8)

Single Pole Compensation

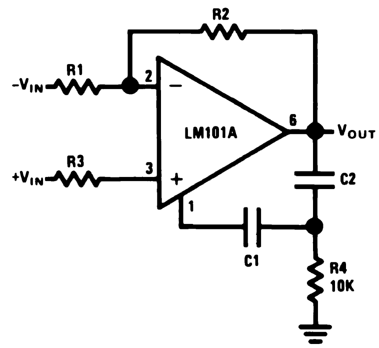


20129608

$$C1 \geq \frac{R1\ C_S}{R1 + R2}$$

C_S= 30 pF

Two Pole Compensation

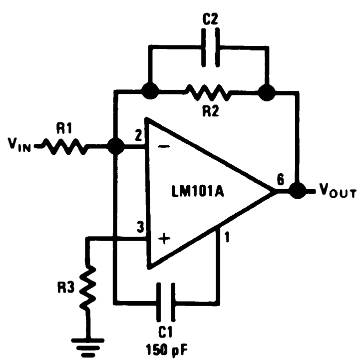


20129612

$$C1 \geq \frac{R1\ C_S}{R1 + R2}$$

C_S= 30 pF
C2 = 10 C1

Feedforward Compensation

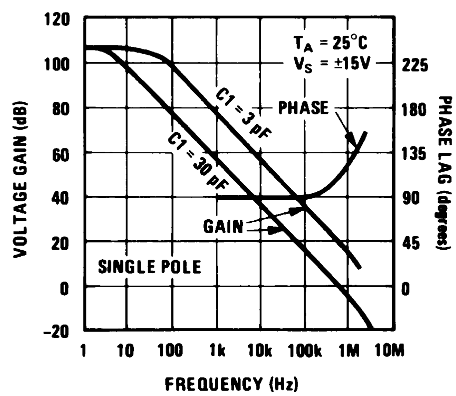


20129616

$$C2 = \frac{1}{2\pi\ f_o\ R2}$$

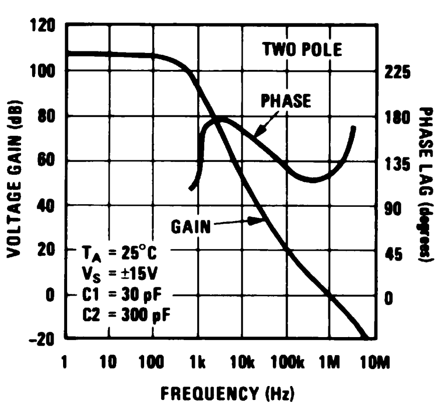
f_o= 3 MHz

Open Loop Frequency Response



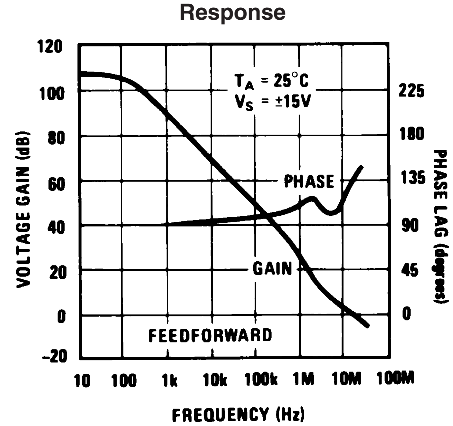
20129609

Open Loop Frequency Response



20129613

Open Loop Frequency Response

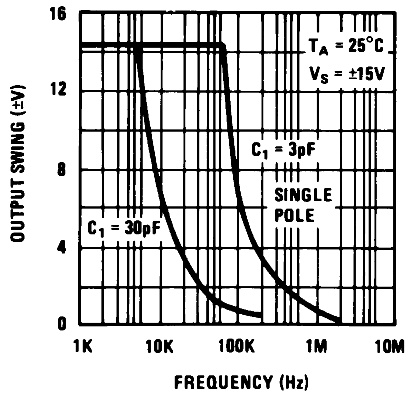


20129617

Typical Performance Characteristics for Various Compensation Circuits

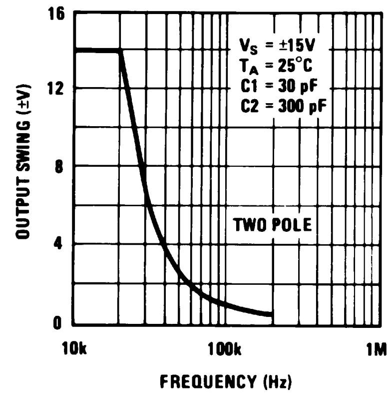
(Note 8) (Continued)

Large Signal Frequency Response



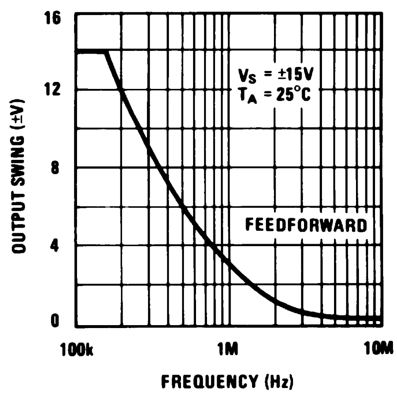
20129610

Large Signal Frequency Response



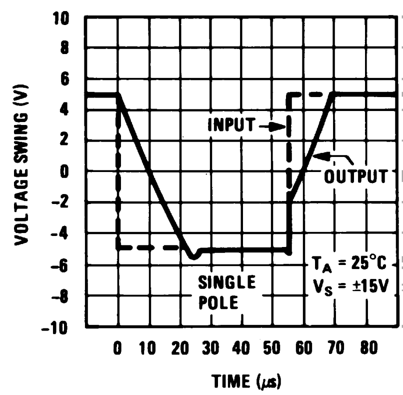
20129614

Large Signal Frequency Response



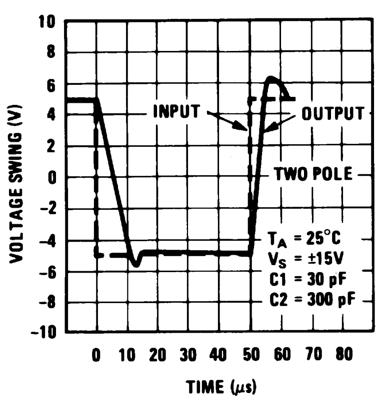
20129618

Voltage Follower Pulse Response



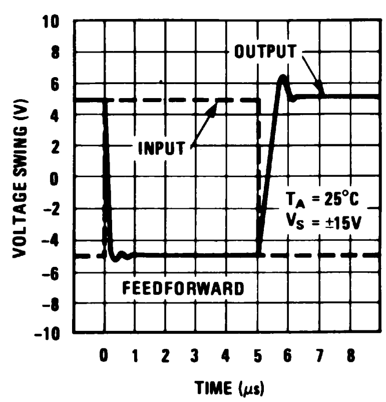
20129611

Voltage Follower Pulse Response



20129615

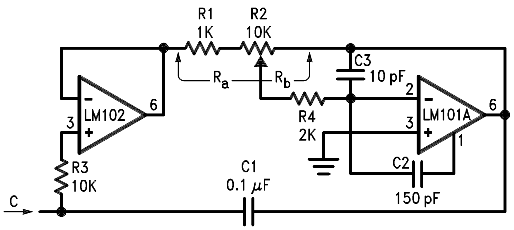
Inverter Pulse Response



20129619

Typical Applications (Note 8)

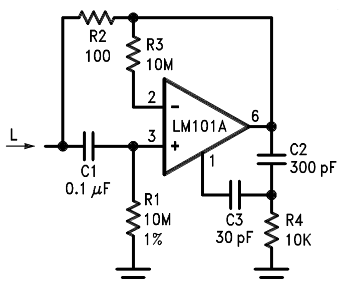
Variable Capacitance Multiplier



20129620

$$C = 1 + \frac{R_b}{R_a} C1$$

Simulated Inductor



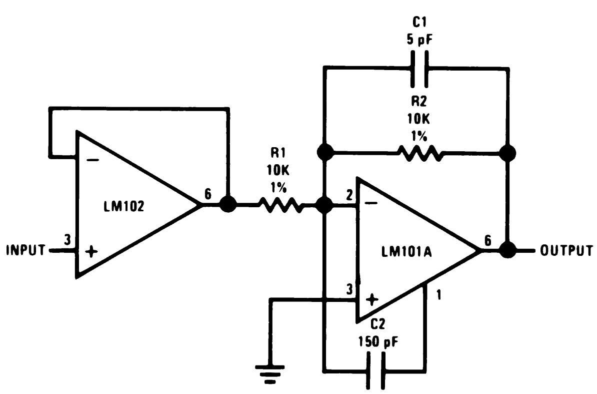
20129621

L ≃ R1 R2 C1

R_S = R2

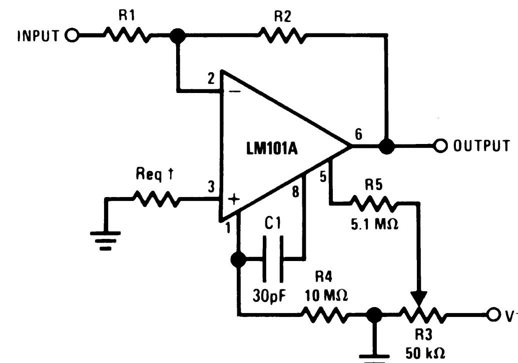
R_P = R1

Fast Inverting Amplifier with High Input Impedance



20129622

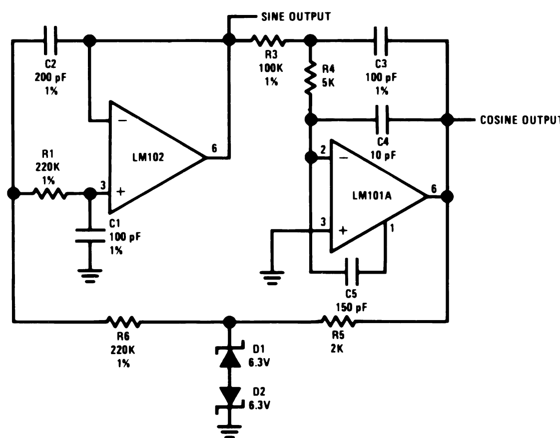
Inverting Amplifier with Balancing Circuit



20129623

†May be zero or equal to parallel combination of R1 and R2 for minimum offset.

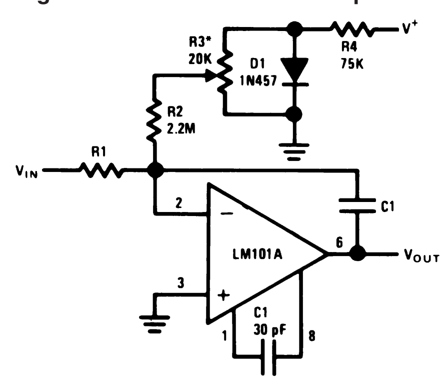
Sine Wave Oscillator



20129624

f_o = 10 kHz

Integrator with Bias Current Compensation

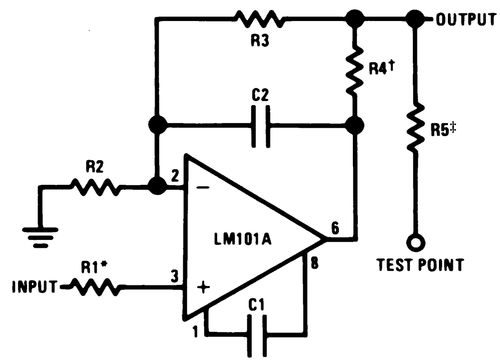


20129625

*Adjust for zero integrator drift. Current drift typically 0.1 nA/˚C over −55˚C to +125˚C temperature range.

Application Hints (Note 8)

Protecting Against Gross Fault Conditions



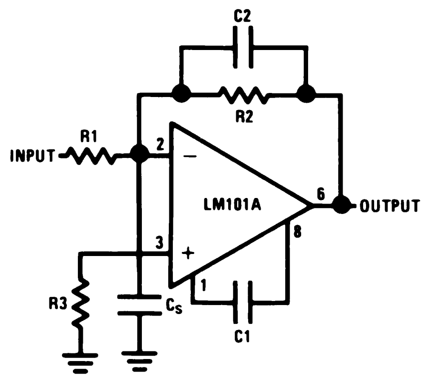
20129626

*Protects input

†Protects output

‡Protects output — not needed when R4 is used.

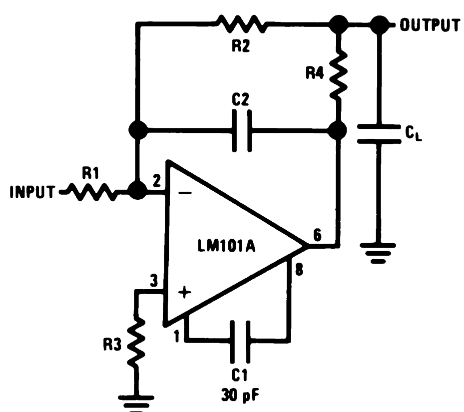
Compensating for Stray Input Capacitances or Large Feedback Resistor



20129627

$$C2 = \frac{R1\ C_S}{R2}$$

Isolating Large Capacitive Loads



20129628

Although the LM101A is designed for trouble free operation, experience has indicated that it is wise to observe certain precautions given below to protect the devices from abnormal operating conditions. It might be pointed out that the advice given here is applicable to practically any IC op amp, although the exact reason why may differ with different devices.

When driving either input from a low-impedance source, a limiting resistor should be placed in series with the input lead to limit the peak instantaneous output current of the source to something less than 100 mA. This is especially important when the inputs go outside a piece of equipment where they could accidentally be connected to high voltage sources. Large capacitors on the input (greater than 0.1 µF) should be treated as a low source impedance and isolated with a resistor. Low impedance sources do not cause a problem unless their output voltage exceeds the supply voltage. However, the supplies go to zero when they are turned off, so the isolation is usually needed.

The output circuitry is protected against damage from shorts to ground. However, when the amplifier output is connected to a test point, it should be isolated by a limiting resistor, as test points frequently get shorted to bad places. Further, when the amplifier drives a load external to the equipment, it is also advisable to use some sort of limiting resistance to preclude mishaps.

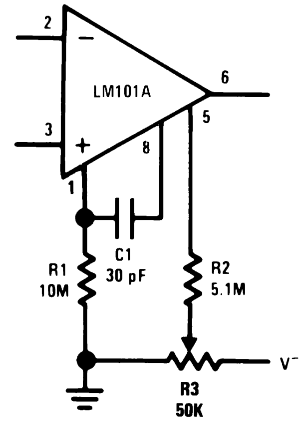
Precautions should be taken to insure that the power supplies for the integrated circuit never become reversed — even under transient conditions. With reverse voltages greater than 1V, the IC will conduct excessive current, fusing internal aluminum interconnects. If there is a possibility of this happening, clamp diodes with a high peak current rating should be installed on the supply lines. Reversal of the voltage between V^+ and V^- will always cause a problem, although reversals with respect to ground may also give difficulties in many circuits.

The minimum values given for the frequency compensation capacitor are stable only for source resistances less than 10 kΩ, stray capacitances on the summing junction less than 5 pF and capacitive loads smaller than 100 pF. If any of these conditions are not met, it becomes necessary to overcompensate the amplifier with a larger compensation capacitor. Alternately, lead capacitors can be used in the feedback network to negate the effect of stray capacitance and large feedback resistors or an RC network can be added to isolate capacitive loads.

Although the LM101A is relatively unaffected by supply bypassing, this cannot be ignored altogether. Generally it is necessary to bypass the supplies to ground at least once on every circuit card, and more bypass points may be required if more than five amplifiers are used. When feed-forward compensation is employed, however, it is advisable to bypass the supply leads of each amplifier with low inductance capacitors because of the higher frequencies involved.

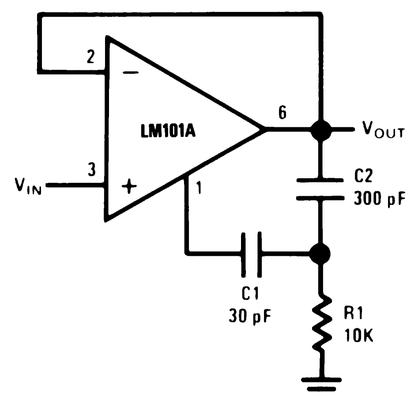
Typical Applications (Note 8)

Standard Compensation and Offset Balancing Circuit



20129629

Fast Voltage Follower

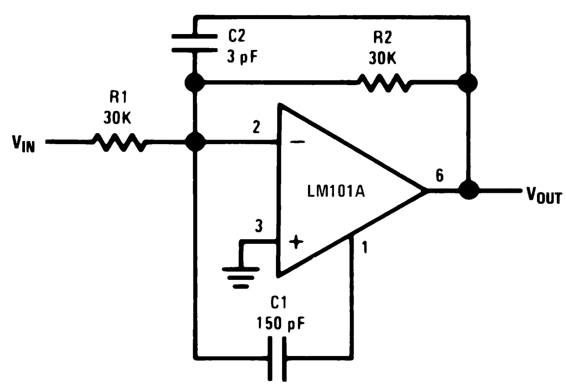


20129631

Power Bandwidth: 15 kHz

Slew Rate: 1V/µs

Fast Summing Amplifier



20129630

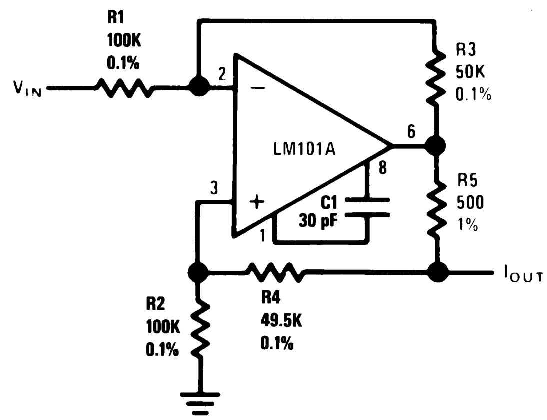
Power Bandwidth: 250 kHz

Small Signal Bandwiidth: 3.5 MHz

Slew Rate: 10V/µs

Typical Applications (Note 8) (Continued)

Bilateral Current Source



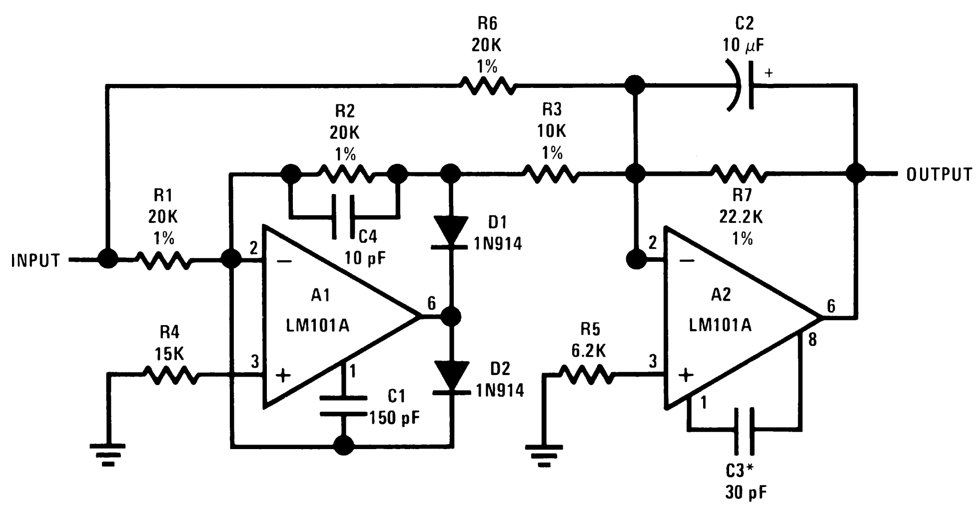
20129632

$$I_{OUT} = \frac{R3\ V_{IN}}{R1\ R5}$$

R3 = R4 + R5

R1 = R2

Fast AC/DC Converter (Note 9)

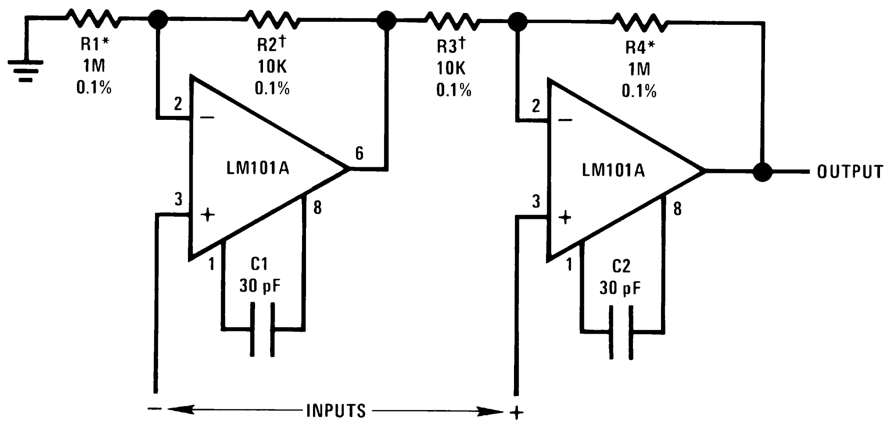


20129633

Note 9: Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Typical Applications (Note 8) (Continued)

Instrumentation Amplifier



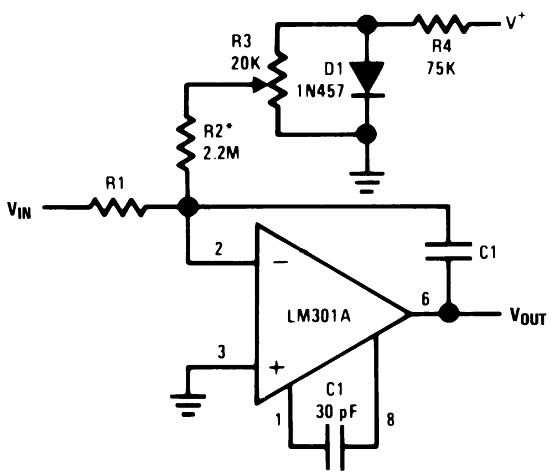
20129634

R1 = R4; R2 = R3

$$A_V = 1 + \frac{R1}{R2}$$

*,† Matching determines CMRR.

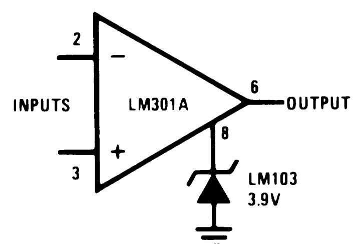
Integrator with Bias Current Compensation



20129635

*Adjust for zero integrator drift. Current drift typically 0.1 nA/˚C over 0˚C to +70˚C temperature range.

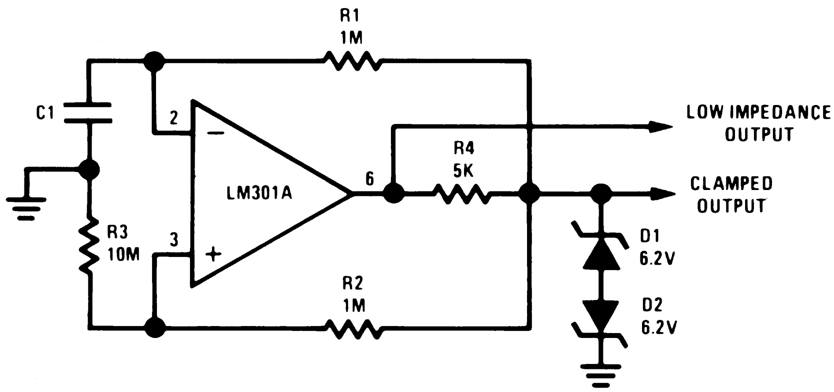
Voltage Comparator for Driving RTL Logic or High Current Driver



20129637

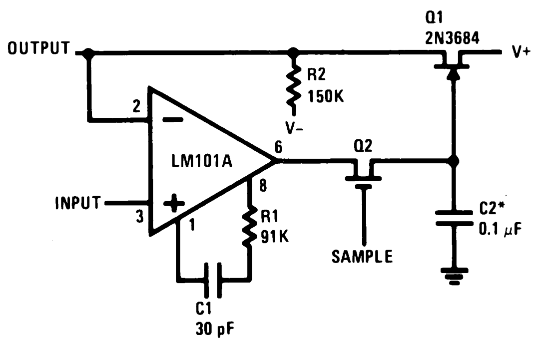
Typical Applications (Note 8) (Continued)

Low Frequency Square Wave Generator



20129636

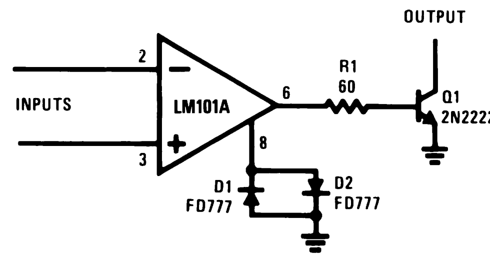
Low Drift Sample and Hold



20129638

*Polycarbonate-dielectric capacitor

Voltage Comparator for Driving DTL or TTL Integrated Circuits

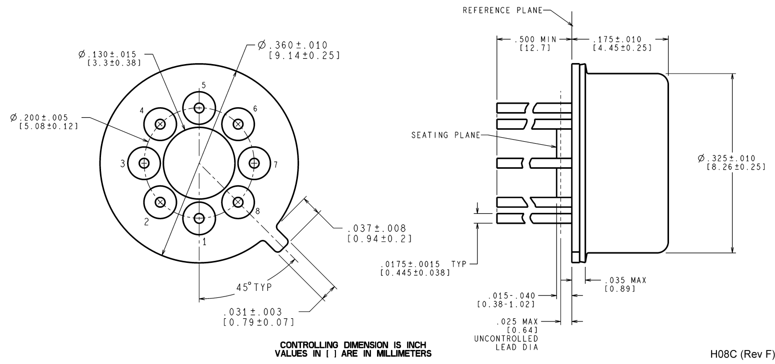


20129639

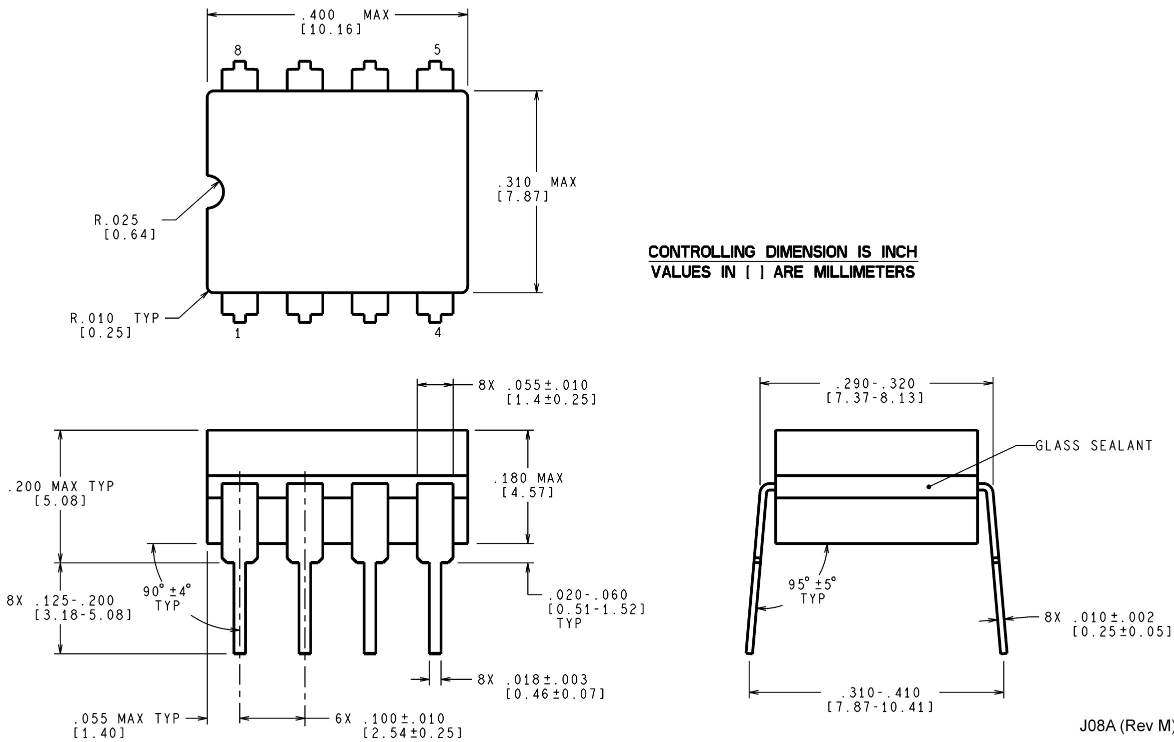
Revision History Section

Date Released	Revision	Section	Originator	Changes
01/05/06	A	New Release to corporate format	L. Lytle	1 MDS datasheets converted into one Corp. datasheet format. MJLM101A-X Rev 1A0 datasheet will be archived.

Physical Dimensions inches (millimeters) unless otherwise noted

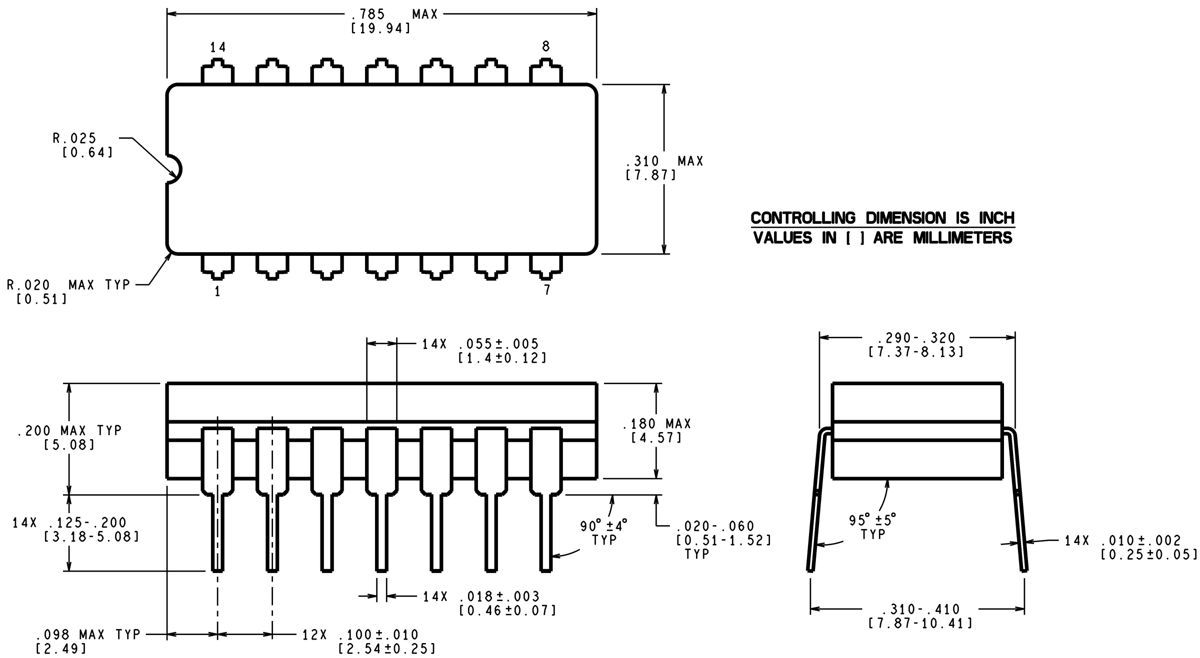


Metal Can Package (H)
NS Package Number H08C



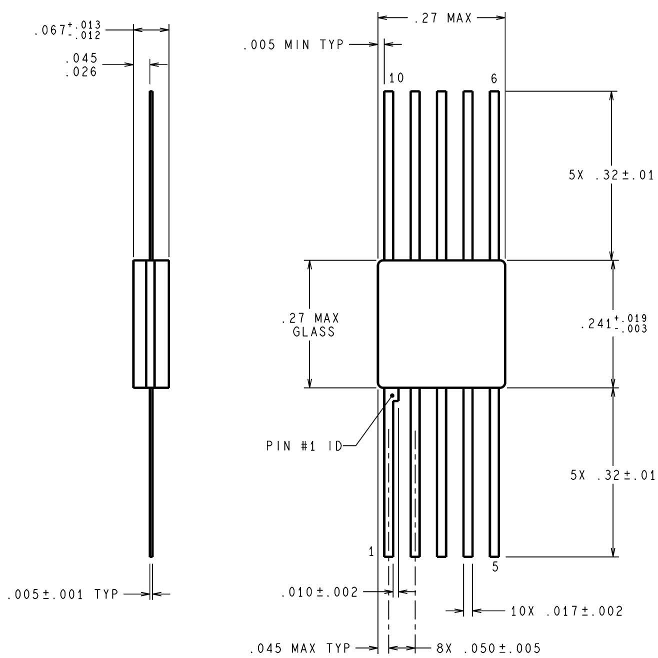
Ceramic Dual-In-Line Package (J)
NS Package Number J08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



J14A (Rev J)

Ceramic Dual-In-Line Package (J)
NS Package Number J14A



DIMENSIONS ARE IN INCHES

W10A (Rev H)

Ceramic Flatpack Package (W)
NS Package Number W10A

Notes

National Semiconductor
Americas Customer
Support Center
Email: new.feedback@nsc.com
Tel: 1-800-272-9959

www.national.com

National Semiconductor
Europe Customer Support Center
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 69 9508 6208
English Tel: +44 (0) 870 24 0 2171
Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer
Support Center
Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
Fax: 81-3-5639-7507
Email: jpn.feedback@nsc.com
Tel: 81-3-5639-7560