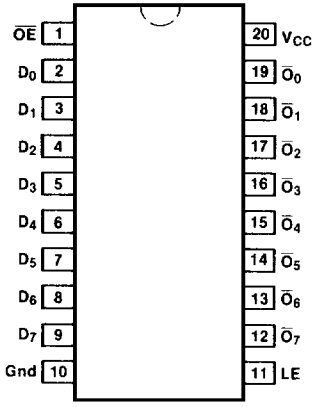
54F/74F563

Octal D-Type Latch
With 3-State Outputs



Pin Assignment for DIP and SOIC

Description

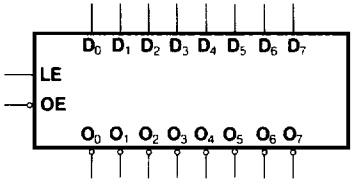
The 'F563 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

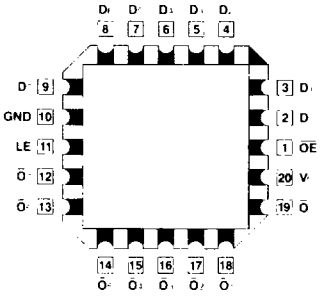
This device is functionally identical to the 'F573, but has inverted outputs.

- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'F573**

Ordering Code: See Section 5

Logic Symbol





Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
D_0-D_7	Data Inputs	0.5/0.375
LE	Latch Enable Input (Active HIGH)	0.5/0.375
$\overline{OE}$	3-State Output Enable Input (Active LOW)	0.5/0.375
$\overline{O_0}$-$\overline{O_7}$	3-State Latch Outputs	75/15 (12.5)

Functional Description

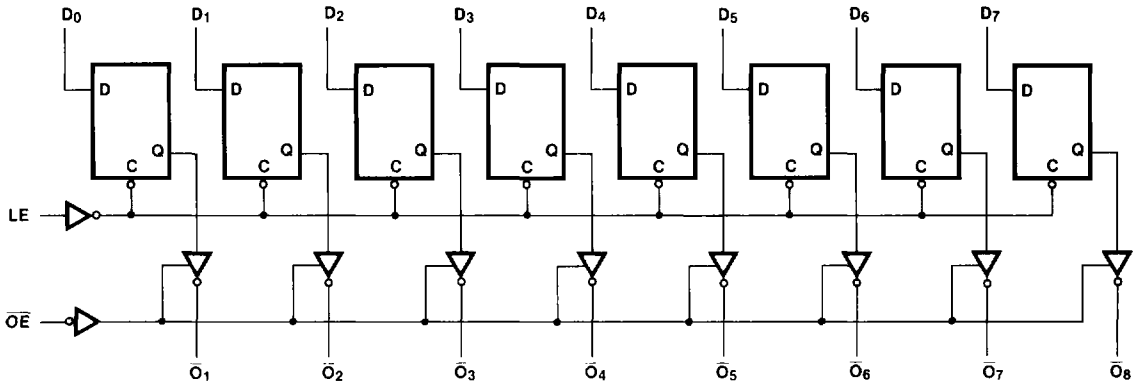
The 'F563 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Function Table

Inputs			Internal	Output	Function
$\overline{OE}$	LE	D	Q	O	
H	X	X	X	Z	High Z
H	H	L	H	Z	High Z
H	H	H	L	Z	High Z
H	L	X	NC	Z	Latched
L	H	L	H	H	Transparent
L	H	H	L	L	Transparent
L	L	X	NC	NC	Latched

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		35	55	mA	V_{CC} = Max, $\overline{OE}$ = HIGH D_n, LE = Gnd (All outputs OFF)

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay D_n to $\overline{O}_n$	4.0 3.0	6.9 5.2	9.0 7.0			3.5 2.5	10.0 8.0	ns	3-1 3-3
t_{PLH} t_{PHL}	Propagation Delay LE to $\overline{O}_n$	5.0 3.0	8.5 5.6	11.0 7.0			4.5 2.5	12.5 8.0	ns	3-1 3-7
t_{PZH} t_{PZL}	Output Enable Time	2.0 2.0	7.7 5.1	10.0 6.5			1.5 1.5	11.5 7.5	ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.7 4.1	6.0 5.5			1.5 1.5	7.0 6.5		

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V			T_A, V_{CC} = Mil		T_A, V_{CC} = Com			
		Min	Typ	Max	Min	Max	Min	Max		
t_s(H) t_s(L)	Setup Time, HIGH or LOW D_n to LE	2.0 2.0					2.5 2.5		ns	3-5
t_h(H) t_h(L)	Hold Time, HIGH or LOW D_n to LE	3.0 3.0					3.5 3.5		ns	3-5
t_w(H)	LE Pulse Width, HIGH	6.0					7.0		ns	3-7