File Number **2338**

D41D Series

T-33-17

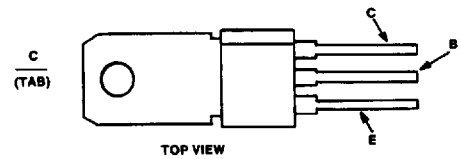
1-Ampere Silicon P-N-P Power Transistors

Complementary to the D40D Series

Features:

- High free-air power dissipation
- Low collector saturation voltage (-0.5V typ. @ -1A I_C).
- Excellent linearity
- Fast switching

TERMINAL DESIGNATIONS



92CS-43222

JEDEC TO-202AB

The D41D-series of silicon p-n-p power transistors are designed for various specific and general purpose applications, such as: output and driver stages of amplifiers operating at frequencies from DC to greater than 1 MHz; series, shunt and switching regulators; and low and high frequency inverters/converters.

These devices are supplied in the JEDEC TO-202AB plastic package.

MAXIMUM RATINGS (T_A = 25° C) (unless otherwise specified)

RATING	SYMBOL	D41D1, 2	D41D4, 5	D41D7, 8	UNITS
Collector-Emitter Voltage	V_{CEO}	-30	-45	-60	Volts
Collector-Emitter Voltage	V_{CES}	-45	-60	-75	Volts
Emitter Base Voltage	V_{EBO}	-5	-5	-5	Volts
Collector Current — Continuous Peak(1)	I_C I_{CM}	-1 -1.5	-1 -1.5	-1 -1.5	A
Base Current — Continuous	I_B	-0.5	-0.5	-0.5	A
Total Power Dissipation @ T_A = 25°C @ T_C = 25C	P_D	1.67 6.25	1.67 6.25	1.67 6.25	Watts
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-55 to +150	-55 to +150	-55 to +150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	75	75	75	°C/W
Thermal Resistance, Junction to Case	$R_{\theta JC}$	20	20	20	°C/W
Maximum Lead Temperature for Soldering Purposes: ⅛" from Case for 5 Seconds	T_L	+260	+260	+260	°C

(1) Pulse Test Pulse Width = 300ms Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (T_C = 25°C) (unless otherwise specified)

CHARACTERISTIC		SYMBOL	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS[1]						
Collector-Emitter Sustaining Voltage (I_C = -10ma)	D41D1, 2 D41D4, 5 D41D7, 8	$V_{CEO(sus)}$	-30 -45 -60	— — —	— — —	Volts
Collector Cutoff Current (V_{CE} = Rated V_{CEO}) T_C = 25°C (V_{CE} = Rated V_{CES}) T_C = 150°C		I_{CES}	— —	— -1	-0.1 —	μA
Emitter Cutoff Current (V_{EB} = -5V)		I_{EBO}	—	—	-0.1	μA
SECOND BREAKDOWN						
Second Breakdown with Base Forward Biased		FBSOA	SEE FIGURE 7			
ON CHARACTERISTICS[1]						
DC Current Gain (I_C = -100mA, V_{CE} = -2V)	D41D1, 4, 7 D41D2, 5, 8	h_{FE}	50 120	— —	150 360	—
(I_C = -1A, V_{CE} = -2V)	D41D1, 4, 7 D41D2 D41D5, 8	h_{FE}	10 20 10	— — —	— — —	—
Collector-Emitter Saturation Voltage (I_C = -500mA, I_B = -50mA)	D41D1, 2, 4, 5 D41D7, 8	$V_{CE(sat)}$	— —	— —	-0.5 -1.0	Volts
Base-Emitter Saturation Voltage (I_C = -500mA, I_B = -50mA)		$V_{BE(sat)}$	—	—	-1.5	Volts
DYNAMIC CHARACTERISTICS						
Collector Capacitance (V_{CB} = -10V, f = 1MHz)		C_{CBO}	—	10	—	pF
Current-Gain — Bandwidth Product (I_C = -20mA, V_{CE} = -10V)		f_T	—	150	—	MHz
SWITCHING CHARACTERISTICS						
Resistive Load						
Delay Time + Rise Time	I_C = -1A, I_{B1} = I_{B2} = -0.1A	$t_d + t_r$	—	50	—	nS
Storage Time	V_{CC} = -30V, t_p = 25 μsec	t_s	—	75	—	
Fall Time		t_f	—	40	—	

(1) Pulse Test PW = 300ms Duty Cycle ≤ 2%.

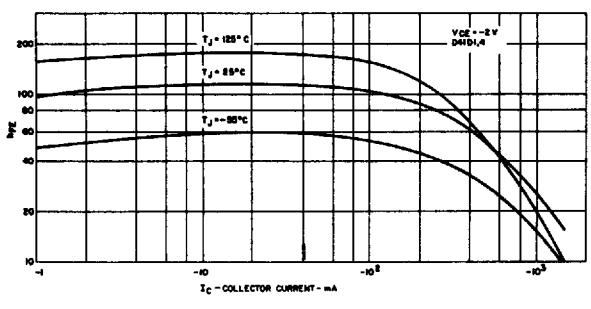


FIG. 1

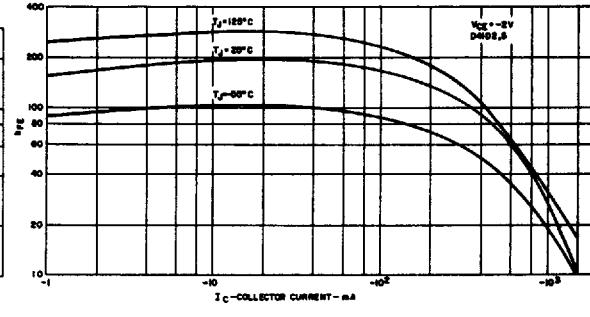


FIG. 2

TYPICAL h_{FE} VS. I_C

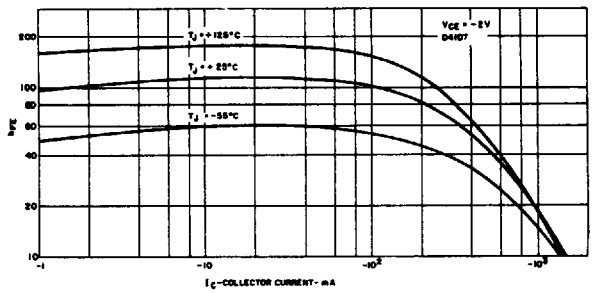


FIG. 3

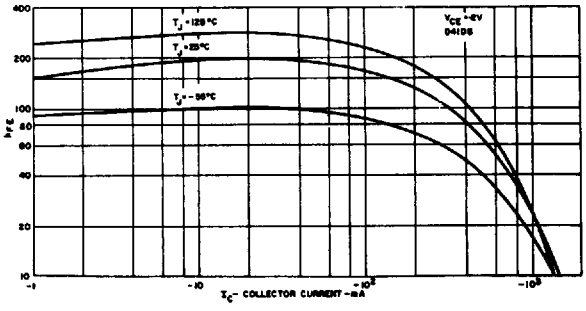


FIG. 4

TYPICAL h_{FE} VS. I_C

T-33-17

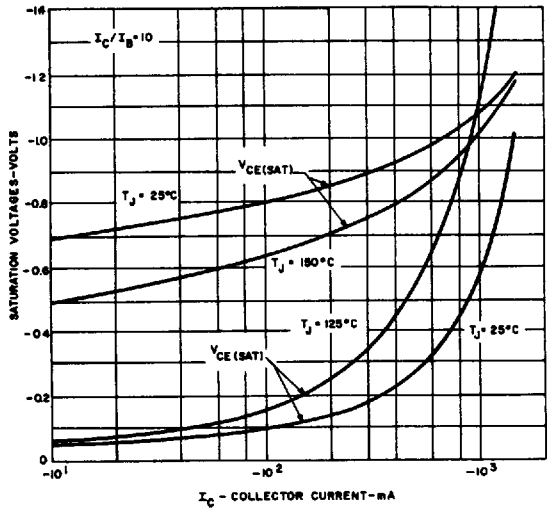


FIG. 5 TYPICAL SATURATION VOLTAGE CHARACTERISTICS

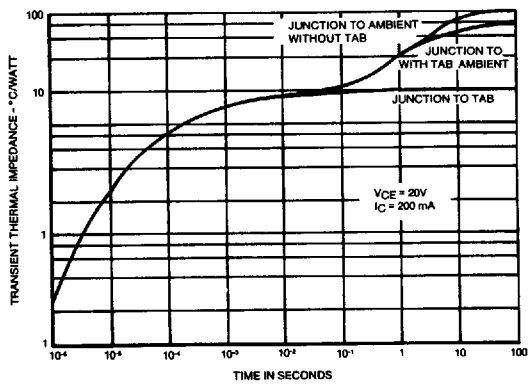


FIG. 6 MAXIMUM TRANSIENT THERMAL IMPEDANCE

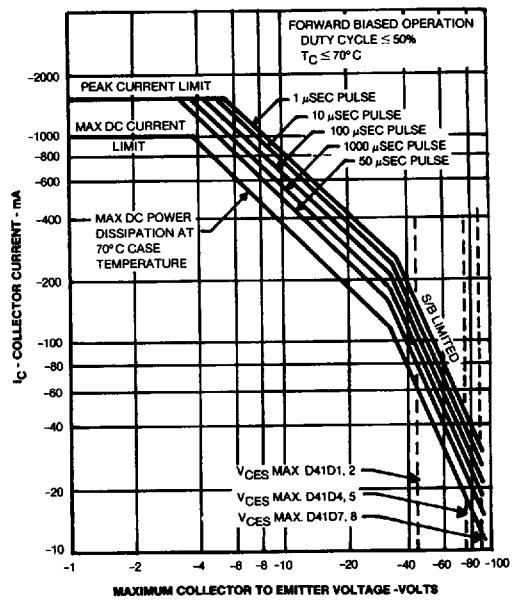


FIG. 7 SAFE REGION OF OPERATION

HARRIS SEMICOND SECTOR