1,024 x 8 DUAL PORT RANDOM ACCESS MEMORY

FEATURES

- 120 ns address access time
- Fully static operation
- Fully TTL compatible
- Interrupt function ($\overline{INT}$): open drain for OR-tied operation
- Easy microprocessor interface
- VM2130—Transparent power-down ($\overline{CE}$)
- VM2131—Non-power-down ($\overline{CS}$)
- Output Enable function ($\overline{OE}$)
- Both ports operate independently.
- Each port accesses entire memory.
- $\overline{BUSY}$ function to handle contention
- 48-pin plastic dual in-line package

DESCRIPTION

The VT2130 and VT2131 are 8,192-bit Dual Port Static Random Access Memories organized 1,024 words by eight bits. They are designed using fully static circuitry and fabricated using n-channel double-poly silicon gate technology.

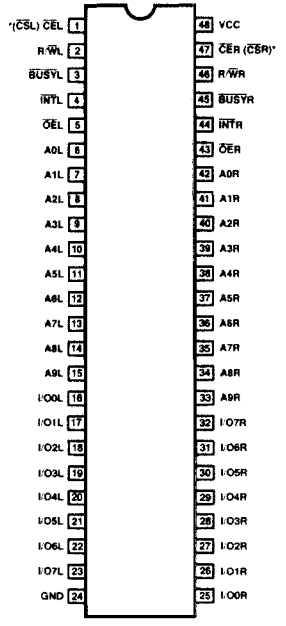
The VT2130 and VT2131 feature two separate I/O ports that each allow independent access for read or write to any location in the memory. The only situation where contention occurs is when both ports are active and both addresses match. Two modes of operation are provided for this situation. In one mode, contention is ignored and both operations are allowed to proceed. In the other mode, on-chip control logic arbitrates delaying one port until the other port's operation is completed. A $\overline{BUSY}$ flag is sent to the side where the operation is delayed. $\overline{BUSY}$ is driven out at speeds that allow the port's processor to preserve its address and data.

An interrupt function ($\overline{INT}$) is provided to allow communication between systems. This function acts like a writable flag. When the flag's location is written from one side, the other side's $\overline{INT}$ pin goes LOW until the flag location is read by that side. The $\overline{INT}$s have open drain drivers to allow OR-tied operation.

The VT 2130 has an automatic power down feature which is controlled by the Chip Enable inputs. Each Chip Enable controls automatic power-down circuitry that allows its respective side of the device to remain in a standby power mode.

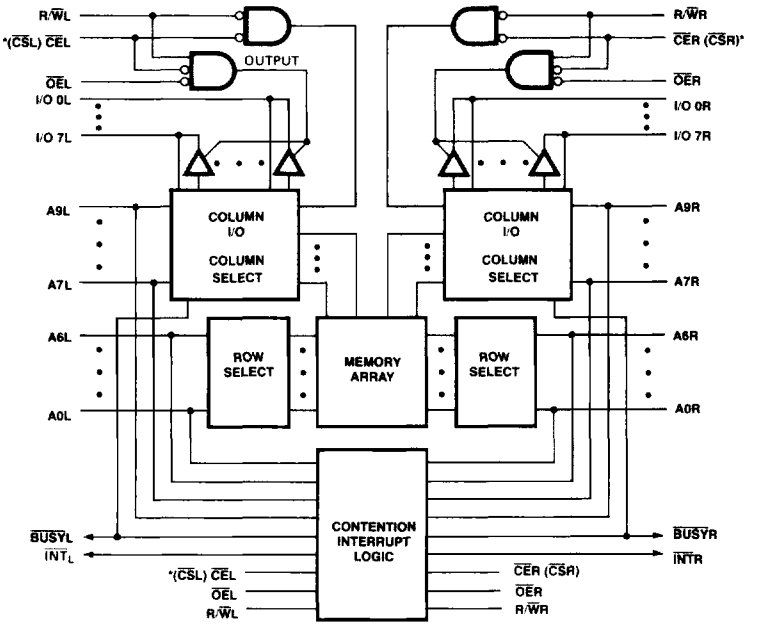
The VT2131 chip select (no power down) access has been designed to be faster than its address access so that the chip select decode time will not add to the memory's overall access time. This feature significantly improves system performance.

PIN CONFIGURATION



*SYMBOL IN (PARENTHESES) APPLIES TO VT2131

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Pin Number	Description
$\overline{CEL}$	1	Left Port Chip Enable—When $\overline{CEL}$ goes HIGH, the left port of the RAM is deselected and the left port control circuitry will automatically power down and remain in a standby power mode as long as $\overline{CEL}$ remains HIGH.
$\overline{CER}$	47	Right Port Chip Enable—When $\overline{CER}$ goes HIGH, the right port of the RAM is deselected and the right port control circuitry will automatically power down and remain in a standby power mode as long as $\overline{CER}$ remains HIGH.
$\overline{CSL}$	1	*Left Port Chip Select—When $\overline{CSL}$ goes HIGH, the left port of the RAM is deselected.*
$\overline{CSR}$	47	Right Port Chip Select—When $\overline{CSR}$ goes HIGH, the right port of the RAM is deselected.
AL	6-15	Left Port Address Inputs—The 10-bit field presented at the left port Address Inputs selects one of the 1024 memory locations to be read from or written into via the left port data Input/Output lines.
AR	33-42	Right Port Address Inputs—The 10-bit field presented at the right port Address Inputs selects one of the 1024 memory locations to be read from or written into via the right port data Input/Output lines.
$\overline{OEL}$	5	*Output Enable for Left Port—When $\overline{OEL}$ is HIGH, the left port outputs are disabled; when $\overline{OEL}$ is* LOW, the left port outputs are enabled. Also controls contention mode for left port.
$\overline{OER}$	43	Output Enable for Right Port—When $\overline{OER}$ is HIGH, the right port outputs are disabled. When $\overline{OER}$ is LOW, the right port outputs are enabled. Also controls contention mode for right port.
I/OL	16-23	Left Port Data Input/Output Lines.
I/OR	25-32	Right Port Data Input/Output Lines.
R/$\overline{WL}$	2	Left Port Read/Write Enable—When $\overline{OEL}$ is LOW and R/$\overline{WL}$ is HIGH, data from the RAM location selected by the left address field is present at the left port Data Input/Output Lines. When R/$\overline{WL}$ is LOW, data present on the left port Data Input/Output Lines is written into the RAM location selected *by the left address field regardless of the state of $\overline{OEL}$. These operations can be affected by* contention. (See Functional Description on page 9).
R/$\overline{WR}$	46	Right Port Read/Write Enable—When $\overline{OER}$ is LOW and R/$\overline{WR}$ is HIGH, data from the RAM location selected by the left address field is present at the right port Data Input/Output Lines. When R/$\overline{WR}$ is LOW, data present on the right port Data Input/Output Lines is written into the RAM location selected by the right address field regardless of the state of $\overline{OER}$. These operations can be affected by contention. (See functional description page 9).
$\overline{BUSYL}$	3	Left Port Busy Flag—$\overline{BUSYL}$ remains HIGH at all times unless both ports initiate an operation to the same address location and the left port is operating in contention mode with the right port receiving priority. When this occurs, the right port operation will be completed first and $\overline{BUSYL}$ will go LOW until the right port operation is completed.
$\overline{BUSYR}$	45	Right Port Busy Flag—$\overline{BUSYR}$ remains HIGH at all times unless both ports initiate an operation to the same address location and the right port is operating in contention mode with the left port receiving priority. When this occurs, the left port operation will be completed first and $\overline{BUSYR}$ will go LOW until the left port operation is completed. Both $\overline{BUSYL}$ and $\overline{BUSYR}$ are open drain outputs allowing OR-tied operation.
$\overline{INTL}$	4	Left Port Interrupt Flag—If the right port writes to memory location 3FE then $\overline{INTL}$ is latched LOW until the left port reads data from memory location 3FE.
$\overline{INTR}$	4	Right Port Interrupt Flag—If the left port writes to memory location 3FF, then $\overline{INTR}$ is latched LOW until the right port reads data from memory location 3FF. Both $\overline{INTL}$ and $\overline{INTR}$ are open drain allowing OR-tied operation.

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ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias	−10 to +85°C
Storage Temperature	−65 to +150°C
Voltage on Any Pin with Respect to Ground	−3.5 to +7V
Power Dissipation	1.0W

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated on the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ± 10%, unless otherwise specified

Symbol	Parameter	VT2130/VT2131 Min	VT2130/VT2131 Max	Unit	Conditions
ILI	Input Load Current (All Input Pins)		10	µA	VCC = Max, VIN = GND to VCC
ILO	Output Leakage Current		10	µA	$\overline{CE}$ = VIH, VCC = Max, VOUT = GND to 4.5 V
ICC	Power Supply Current (Both Ports Active)		150	mA	TA = 25°C, VCC = Max, $\overline{CE}$ = VIL, Outputs Open
ICC	Power Supply Current (Both Ports Active)		170	mA	TA = 0°C, VCC = Max, $\overline{CE}$ = VIL, Outputs Open
ISB1	Standby Current (Both Ports Standby)		40	mA	VCC = Min to Max, $\overline{CEL}$ and $\overline{CER}$ = VIH, Notes 6, 10
ISB2	Standby Current (One Port Standby)		110	mA	VCC = Min to Max, $\overline{CEL}$ and $\overline{CER}$ = VIH, Notes 6, 10
VIL	Input LOW Voltage	-0.5	0.8	V	
VIH	Input HIGH Voltage	2.4	6.0	V	
VOL	Output LOW Voltage		0.4	V	IOL = 3.2 mA, Note 12
VOH	Output HIGH Voltage	2.4		V	IOH = −1.0 mA, Note 12

CAPACITANCE TA = 25°C, f = 1.0 MHz, Note 14

Symbol	Parameter	Typ	Max	Unit
COUT	Output Capacitance		5	pF
CIN	Input Capacitance		5	pF

AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5V ± 10%

Symbol	Parameter	VT2130/31-12 Min	VT2130/31-12 Max	VT2130/31-15 Min	VT2130/31-15 Max	VT2130/31-20 Min	VT2130/31-20 Max	Unit
tRC	Read Cycle Time	120		150		200		ns
tAA	Address Access Time		120		150		200	ns
tACE	Chip Enable Access Time, Note 10		120		150		200	ns
tAOE	Output Enable Access Time		50		60		80	ns
tOH	Output Hold from Address Change	10		10		20		ns
tLZ	Output Low Z Time, Note 5	10		10		20		ns
tHZ	Output High Z Time, Note 5	0	50	0	60	0	80	ns
tPU	Chip Enable to Power Up Time, Note 10	0		0		0		ns
tPD	Chip Disable to Power Down Time, Note 10		60		70		100	ns
tACS	Chip Select Access Time, Note 11		100		110		160	ns

Note:

See notes on next page

AC CHARACTERISTICS TA = 0°C to +70°C, VCC = 5 V ± 10%, Cont.

Symbol	Parameter	VT2130/31-12		VT2130/31-15		VT2130/31-20		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle								
tWC	Write Cycle Time	120		150		200		ns
tEW	Chip Enable to End of Write, Note 10	105		120		180		ns
tSW	Chip Select to End of Write, Note 11	85		90		140		ns
tAW	Address Valid to End of Write	105		120		180		ns
tAS	Address Setup Time	0		0		0		ns
tWP	Write Pulse Width	70		80		120		ns
tWR	Write Recovery Time	0		0		0		ns
tDW	Data Valid to End of Write	50		60		80		ns
tDH	Data Hold Time	0		0		0		ns
tWZ	Write Enabled to Output in HIGH Z, Note 5	0	50	0	60	0	80	ns
tOW	Output Active from End of Write, Note 5	0		0		0		ns
Busy Timing								
tRC	Read Cycle Time	120		150		200		ns
tWC	Write Cycle Time	120		150		200		ns
tOEH	Output Enable Hold Time	25		30		40		ns
tOER	Output Enable Recovery Time	0		0		0		ns
tBAA	$\overline{BUSY}$ Access Time to Address		50		60		80	ns
tBDA	$\overline{BUSY}$ Disable Time to Address		50		60		80	ns
tBAC	$\overline{BUSY}$ Access Time to Chip Enable or Chip Select		50		60		80	ns
tBDC	$\overline{BUSY}$ Disable Time to Chip Enable or Chip Select		50		60		80	ns
tAPS	Arbitration Priority Set Up Time	25		30		40		ns
tAOS	Arbitration Override Set Up Time	25		30		40		ns
Interrupt Timing, Note 12								
tAS	Address Set Up Time	0		0		0		ns
tAW	Write Recovery Time	0		0		0		ns
tINS	Interrupt Set Time		100		120		160	ns
tINR	Interrupt Reset Time		100		120		160	ns

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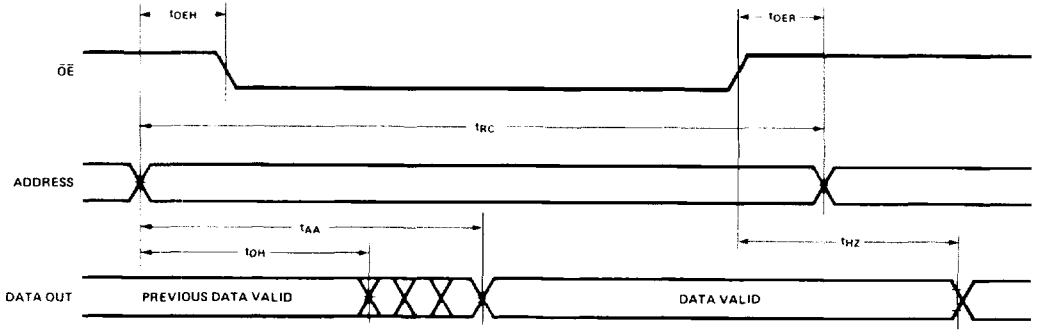
Notes:

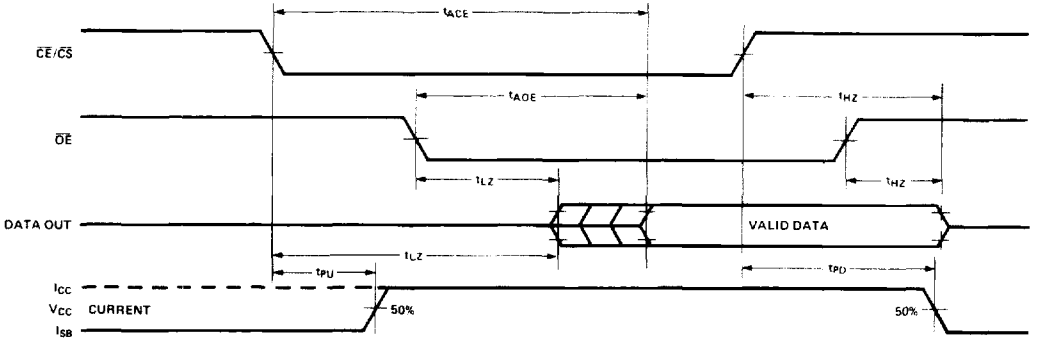
1. R/$\overline{W}$ is HIGH for Read Cycles.
2. Device is continuously enabled/selected, $\overline{CE}$ = VIL or $\overline{CS}$ = VIL.
3. Addresses valid prior to or coincident with $\overline{CE}$ or $\overline{CS}$ transition LOW.
4. If $\overline{CE}$ or $\overline{CS}$ goes HIGH simultaneously with R/$\overline{W}$ HIGH, the outputs remain in the high-impedance state.
5. *Transition is measured ±500 mV from low- or high-impedance voltage with load B. This parameter is sampled and not 100% tested.*
6. A pull-up resistor to VCC on the $\overline{CE}$ or $\overline{CS}$ input is required to keep the device deselected; otherwise, power-on current approaches ICC active.
7. $\overline{OE}$ = VIH when contention occurs.
8. $\overline{CEL}$ = $\overline{CER}$ = VIL or $\overline{CSL}$ = $\overline{CSR}$ = VIL.
9. Busy timing is identical to contention cycles 1 and 2.
10. Applies to 2130 version (power down) only.
11. Applies to 2131 version (non-power down) only.
12. The interrupts (pins 4 and 44) are open-drain outputs. A pull-up resistor is required for system operation. Load C is used for ac testing these pins. All other outputs use load A.
13. *Read or Write Cycle Timing after $\overline{BUSY}$ inactive as shown in previous timing diagrams.*
14. This parameter is periodically sampled but not 100% tested.

TIMING DIAGRAMS

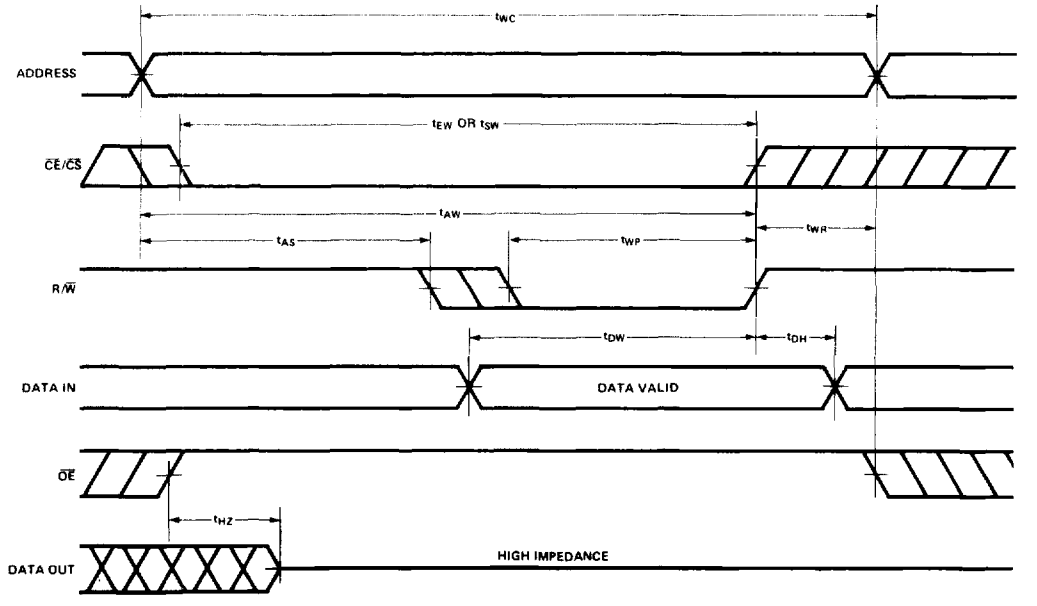
READ CYCLE NO. 1 EITHER SIDE, Notes 1 and 2, Page 5-35



READ CYCLE NO. 2 EITHER SIDE, Notes 1 and 3, Page 5-35

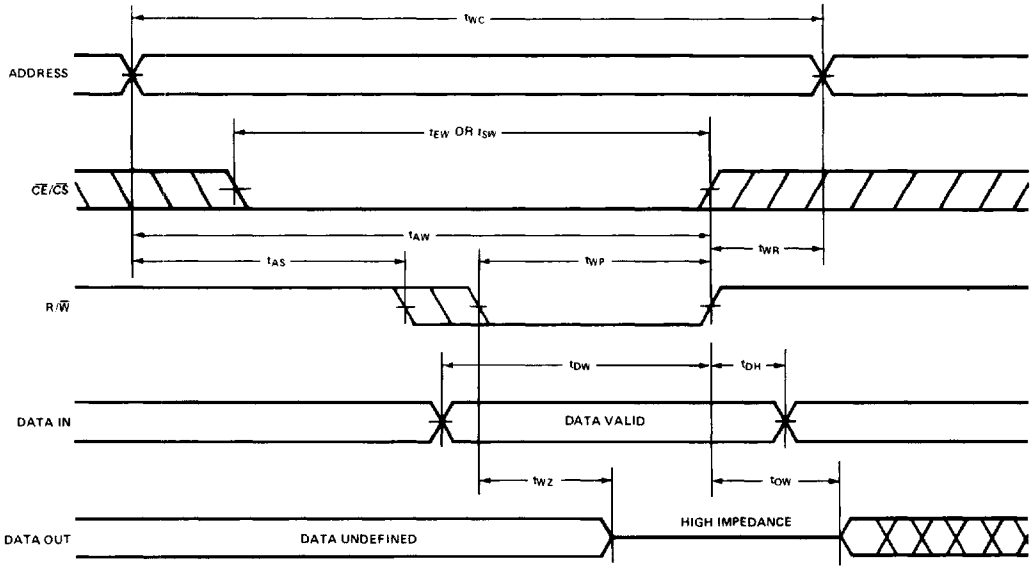


WRITE CYCLE NO. 1 EITHER SIDE, Note 4, Page 5-35



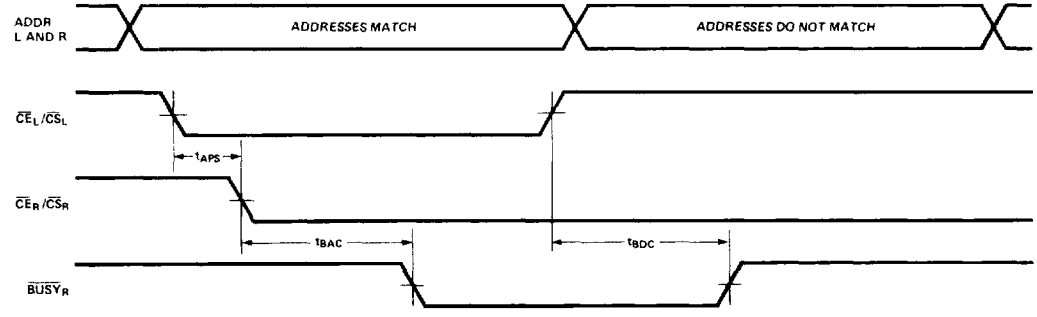
TIMING DIAGRAMS (Cont.)

WRITE CYCLE NO. 2 EITHER SIDE $\overline{OE}$ = VIL, Note 4, Page 5-35

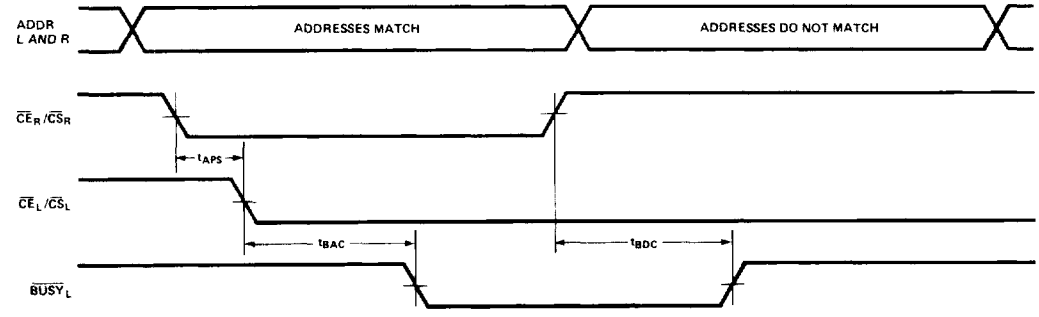


CONTENTION CYCLE NO. 1 $\overline{CE}/\overline{CS}$ CONTENTION ARBITRATION MODE, Note 7, Page 5-35

$\overline{CEL}/\overline{CSL}$ VALID FIRST



$\overline{CER}/\overline{CSR}$ VALID FIRST



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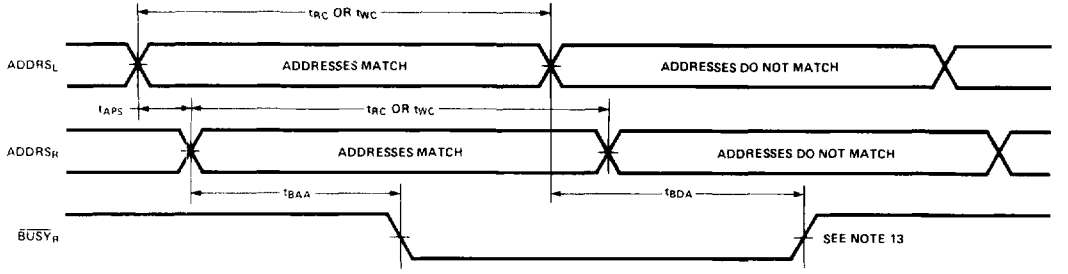
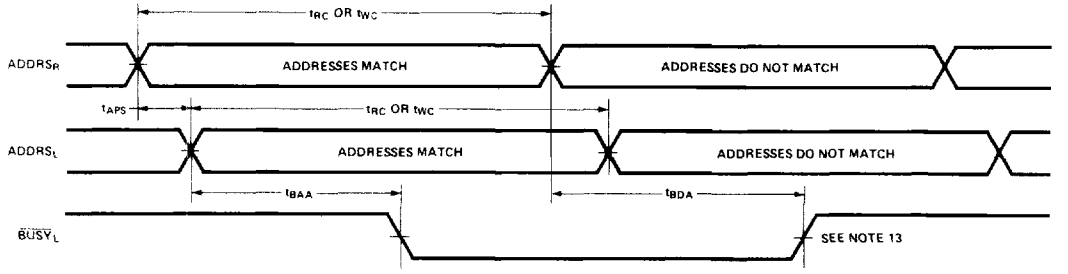
TIMING DIAGRAMS (Cont.)

CONTENTION CYCLE NO. 2 ADDRESS CONTENTION ARBITRATION MODE, Notes 7 and 8, Page 5-35

ADDRESSL VALID FIRST

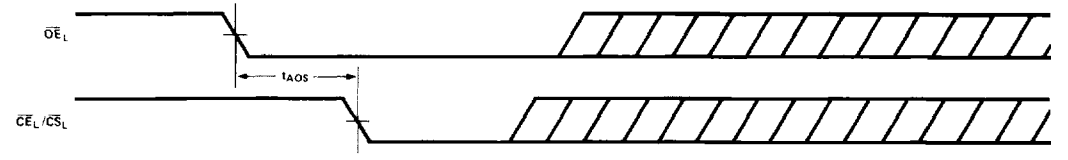


ADDRESSR VALID FIRST

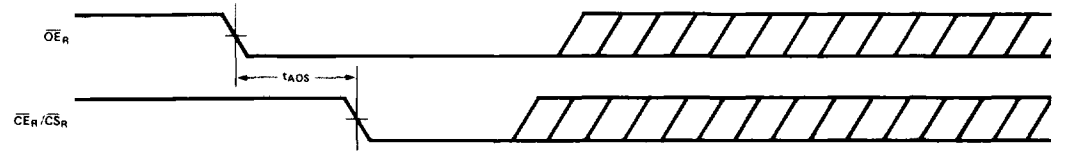


CONTENTION CYCLE NO. 3 CONTENTION OVERRIDE MODE, Note 9, Page 5-35

LEFT PORT CONTENTION IGNORED



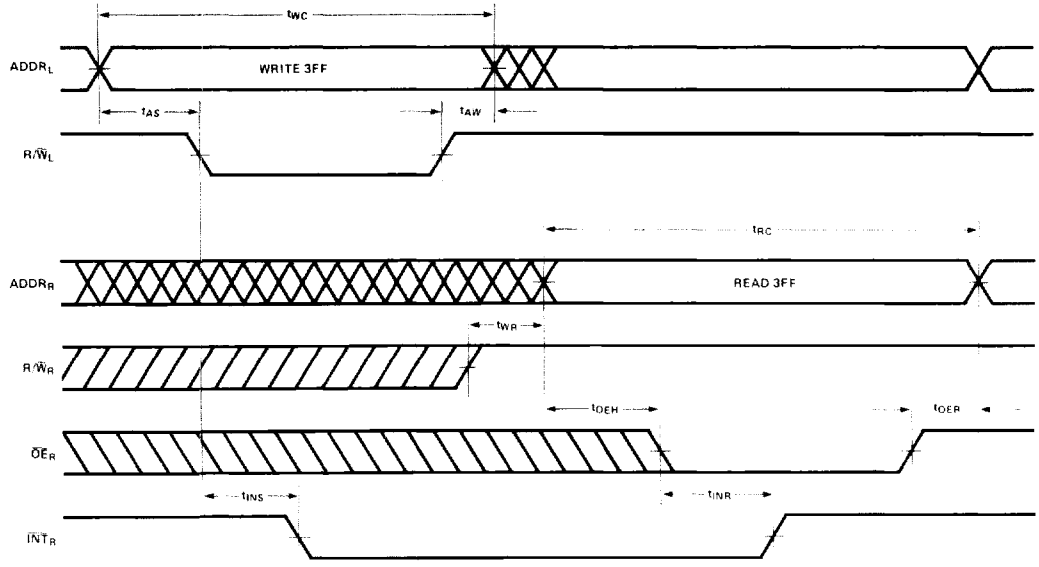
RIGHT PORT CONTENTION IGNORED



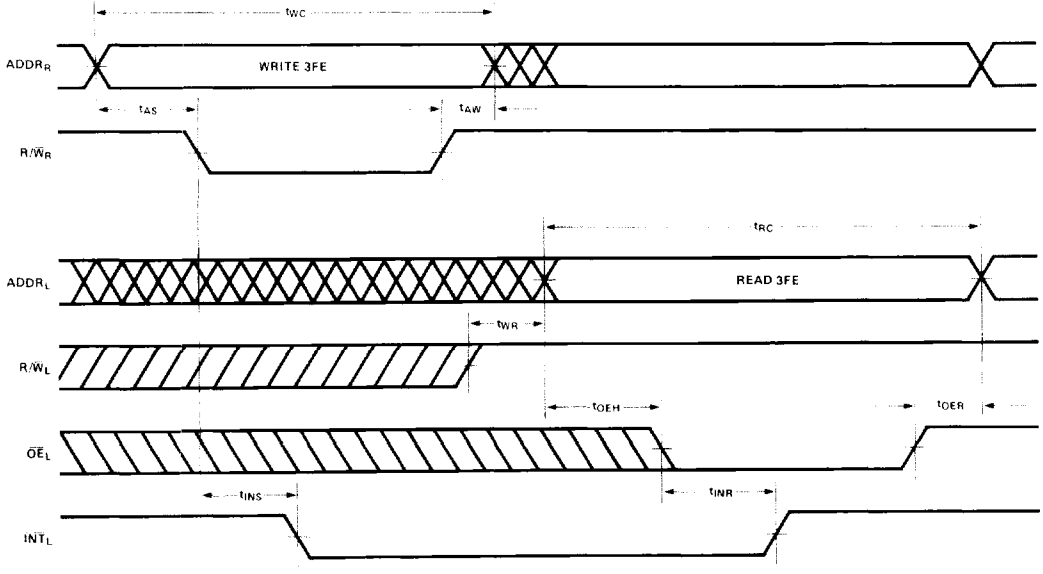
TIMING DIAGRAMS (Cont.)

INTERRUPT MODE, Note 8, Page 5-35

LEFT SIDE FLAGS RIGHT SIDE



RIGHT SIDE FLAGS LEFT SIDE



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FUNCTIONAL DESCRIPTION

The VT2130 and VT2131 are 1024-word by 8-bit dual port RAMs that feature two separate I/O ports. Each port allows independent access for read or write to any location in the memory.

The VT2130 features separate left and right port Chip Enable controls ($\overline{CEL}$ and $\overline{CER}$). Each Chip Enable activates its respective port when it goes LOW and controls automatic power-down circuitry that allows its respective side of the device to remain in a standby power mode as long as it remains HIGH. When a port is active, it is allowed access to the entire memory array.

The VT2131 features separate left and right port Chip Select controls ($\overline{CSL}$ and $\overline{CSR}$). Each Chip Select activates its respective port when it goes LOW and allows its respective side of the device to remain selected as long as it remains HIGH. When a port is active, it is allowed access to the entire memory array.

Each port has an Output Enable control ($\overline{OEL}$ and $\overline{OER}$) that keeps its respective output in a high impedance mode when HIGH. When a port's $\overline{OE}$ is LOW, that port's output drivers are turned on, providing its R/$\overline{W}$ control is HIGH.

Separate Read/Write Enable inputs (R/$\overline{WL}$ and R/$\overline{WR}$) control writing of new data into any location in the RAM from either port. When R/$\overline{WL}$ is LOW, new data is written into the location selected by the left address field. Likewise, when R/$\overline{WR}$ is LOW, new data is written into the location selected by the right address field. When a port's Read/Write Enable is HIGH, data can be read from that port if its respective $\overline{OE}$ is LOW. When R/$\overline{WL}$ is HIGH and $\overline{OEL}$ is LOW, data is read from the location selected by the left address field. When R/$\overline{WR}$ is HIGH and $\overline{OER}$ is LOW, data is read from the location selected by the right address field.

There is one situation where contention can occur. It is when both left and right ports are active and both addresses match. Two modes of operation are provided for this situation: (a) on-chip control logic arbitrates the situation; or (b) contention is ignored and both ports are given access to that memory location. $\overline{OE}$ controls the mode of operation.

If $\overline{CE}$ or $\overline{CS}$ is LOW before $\overline{OE}$ goes LOW when both addresses match, then on-chip control logic arbitrates the situation. Priority is given to the port whose $\overline{CE}$ or $\overline{CS}$ became valid first; the other port will not be allowed access to the memory core until that port's operation is completed.

If both ports' $\overline{CE}$ or $\overline{CS}$ controls become valid at the same time when their $\overline{OE}$s are HIGH, then the left port is given priority. If both $\overline{CE}$ or $\overline{CS}$ pins are valid before their respective $\overline{OE}$ controls and an address change causes an address match while $\overline{OE}$ is HIGH, then priority is given to the port whose address became valid first; the other port is not allowed access to the memory until that port's operation is completed. If both addresses became valid at the same time and match, and $\overline{OE}$ is HIGH, then the left port is given priority.

In the other mode, contention is ignored and one or both ports have access to the memory core at all times. This is accomplished by having $\overline{OE}$ LOW when the contention occurs. That is, the RAM core is accessible from a port even if the on-chip control logic would have delayed its access provided: (a) the port's $\overline{OE}$ is LOW when its $\overline{CE}$ or $\overline{CS}$ goes LOW during an address match; or (b) both ports are active and its $\overline{OE}$ is LOW when an address change causes an address match. Therefore, it is possible for both ports to have access to the same memory location at the same time, even in a WRITEL-WRITER situation.

Separate Busy Flags ($\overline{BUSYL}$ and $\overline{BUSYR}$) are provided to signal when a port's access to the memory core has been delayed. When both ports try to access the same memory location, the on-chip arbitration logic causes the Busy Flag to go LOW on the side that is delayed. These flags are provided to allow the user to stop the processor if desired. $\overline{BUSY}$ is driven out fast enough for the processor's address and data to be preserved if desired. The Busy Flags are operational even when the device is operating in the mode when contention is ignored and function the same as described for contention mode operation. This permits their use to signal that contention has occurred and data may have been changed.

Interrupt logic is included on-chip to provide a means for two processors to communicate with one another. If the left port writes to memory location 3FF, then the right port Interrupt Flag ($\overline{INTR}$) is latched LOW until the right port reads data from that same location. If the right port writes to location 3FE, then the left port Interrupt Flag ($\overline{INTL}$) is latched low until the left port reads data from that location. If both ports are enabled and contention occurs, the Busy circuitry will disable the address decoder from setting or resetting the Interrupt Flags.

TABLE 1: NON-CONTENTION READ/WRITE CONTROL

Left Port Inputs				Right Port Inputs				Left Flags		Right Flags		
R/$\overline{W}$L	$\overline{CE}$L/$\overline{CS}$L	$\overline{OE}$L	A0L-A9L	R/$\overline{W}$R	$\overline{CE}$R/$\overline{CS}$R	$\overline{OE}$R	A0R-A9R	$\overline{BUSY}$L	$\overline{INT}$L	$\overline{BUSY}$R	$\overline{INT}$R	Function
X	H	X	X	X	X	X	X	H	X	H	X	Left Port in Power Down Mode
X	X	X	X	X	H	X	X	H	X	H	X	Right Port in Power Down Mode
L	L	X	X	X	X	X	X	H	X	H	X	Data on Left Port Written to Memory Location A0L-A9L
H	L	L	X	X	X	X	X	H	X	H	X	Data in Memory Location A0L-A9L Output on Left Port
X	X	X	X	L	L	X	X	H	X	H	X	Data on Right Port Written to Memory Location A0R-A9R
X	X	X	X	H	L	L	X	H	X	H	X	Data in Memory Location A0R-A9R Output on Right Port
L	L	X	3FF	X	X	X	X	H	X	H	L	Left Side Flags Right Side to Read Memory Location 3FF
X	X	X	X	L	L	X	3FE	H	L	H	X	Right Side Flags Left Side to Read Memory Location 3FE

H = HIGH L = LOW X = Don't Care

TABLE 2: $\overline{CE}/\overline{CS}$ AND $\overline{OE}$ ARBITRATION

Left Port Inputs			Right Port Inputs			Left Flags		Right Flags		
R/$\overline{W}$L	$\overline{CE}$L/$\overline{CS}$L	$\overline{OE}$L	R/$\overline{W}$R	$\overline{CE}$R/$\overline{CS}$R	$\overline{OE}$R	$\overline{BUSY}$L	$\overline{INT}$L	$\overline{BUSY}$R	$\overline{INT}$R	Function
X	L1	X	X	L	LAC	H	X	L	X	Left Operation Allowed RAM Inaccessible from Right
X	L	LAC	X	L1	X	L	X	H	X	Right Operation Allowed RAM Inaccessible from Left
X	Both	X	X	Both	LAC	H	X	L	X	Left Operation Allowed RAM Inaccessible from Right
X	L1	X	X	L	LBC	H	X	L	X	Left Operation Allowed RAM Accessible from Right, Note 1
X	L	LBC	X	L1	X	L	X	H	X	Right Operation Allowed RAM Accessible from Left, Note 1
X	Both	X	X	Both	LBC	H	X	L	X	Left Operation Allowed RAM Accessible from Right, Note 1

L1 = Pin active before equivalent pin on other port.
LAC = LOW after Chip Enable.
LBC = LOW before Chip Enable.
Both = Equivalent pins on both ports become active at the same time.

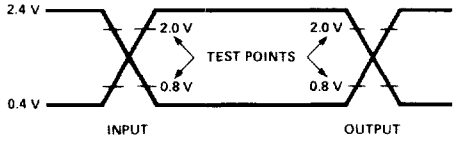
TABLE 3: ADDRESS AND $\overline{OE}$ ARBITRATION

Left Port Inputs				Right Port Inputs				Left Flags		Right Flags		Function
R/$\overline{W}$L	$\overline{CE}$L/$\overline{CS}$L	$\overline{OE}$L	A0L-A9L	R/$\overline{W}$R	$\overline{CE}$R/$\overline{CS}$R	$\overline{OE}$R	A0R-A9R	$\overline{BUSY}$L	$\overline{INT}$L	$\overline{BUSY}$R	$\overline{INT}$R	
X	L	X	Match 1	X	L	X	Match	H	X	L	X	Left Operation Allowed, Note 2
X	L	X	Match	X	L	X	Match 1	L	X	H	X	Right Operation Allowed, Note 2
X	L	X	Both	X	L	X	Both	H	X	L	X	Left Operation Allowed, Note 2

Match = Addresses on left and right ports are identical.
Match 1 = Address valid on the port before becoming valid on opposite port.
Both = Addresses match and become valid on both ports at the same time.

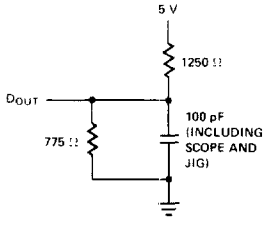
Notes:
1. See Contention Override Mode Timing on page 7.
2. RAM is inaccessible from other port unless that port's $\overline{OE}$ was LOW when the match occurred.

AC TESTING INPUT, OUTPUT WAVEFORM

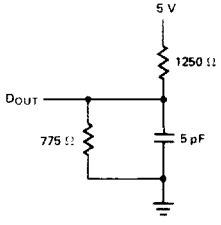


AC TESTING: INPUTS ARE DRIVEN AT 2.4 V FOR A LOGIC 1 AND 0.4 V FOR A LOGIC 0. TIMING MEASUREMENTS ARE MADE AT 2.0 V FOR A LOGIC 1 AND 0.8 V FOR A LOGIC 0 INPUT PULSE RISE AND FALL TIMES ARE 5 ns

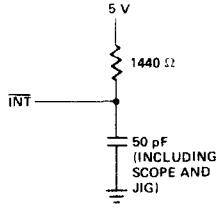
AC TESTING LOAD CIRCUITS



LOAD A



LOAD B



LOAD C